McIDAS

Man computer Interactive Data Access System

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WORKSTATION HARDWARE DESCRIPTION

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PREFACE

This manual was prepared by the Space Science and Engineering Center (SSEC), University of Wisconsin-Madison, to assist you with hardware maintenance of the Man-Computer Interactive Data Access System (McIDAS) Workstation. The manual is intended for McIDAS owners whose workstations use DATARAM Corporation's memory storage system.

In each workstation, some units are off-the-shelf devices, while others are modified or designed and developed by SSEC. This manual is designed to complement off-the-shelf unit documentation, to supplement modified-unit documentation, and to provide primary documentation for SSEC-developed units. Therefore, an important part of this manual is a list of reference manuals you should have received with your McIDAS. Appendix A is a typical McIDAS reference manual list.

A brief system overview and detailed workstation overview are followed by unit or circuit board documentation. Each unit or circuit board section includes an introduction, a functional description, and either applicable references for off-the-shelf units, modification descriptions for modified off-the-shelf units, or detailed circuit descriptions for custom units.

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McIDAS WORKSTATION OVERVIEW

INTRODUCTION

The McIDAS workstation is the link between the user and the McIDAS. It provides the animated display of satellite imagery and weather data. A CRT terminal allows the user to issue commands to the workstation and the host, and receive alpha-numeric information from the host. A large memory system stores image and graphics data; a color monitor is used to view this data, and a pair of joysticks is used to position the cursor on the data display. Optionally, a printer is connected to the workstation to produce a hardcopy of the alpha-numeric information. A graphics tablet can also be included; it executes pre-programmed strings of commands when the user points to specific regions of the tablet.

A brief description of SSEC's version of the McIDAS is provided to describe how the workstation fits into the total system. Users' systems range from single McIDAS workstations, linked remotely to SSEC's McIDAS, to complete systems like the SSEC McIDAS, to more elaborate systems, similar to SSEC's McIDAS, but with more or different components. The McIDAS workstation description follows the McIDAS system description.

McIDAS SYSTEM DESCRIPTION

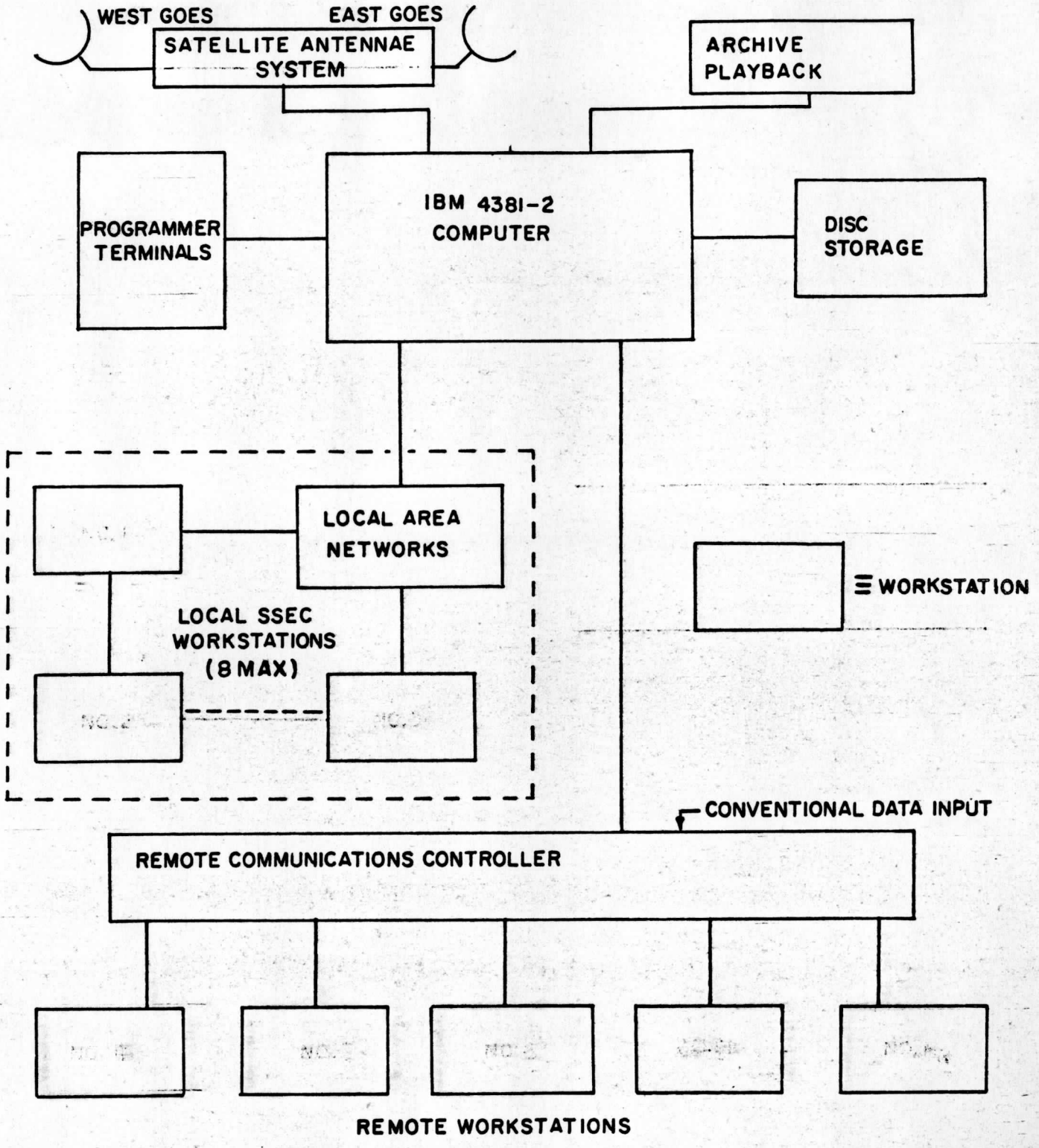
Figure 1 is a block diagram of the SSEC McIDAS. Each block or group of blocks is reviewed in terms of its function within the system.

EAST AND WEST GOES ANTENNAS

The GOES (Geosynchronous Operational Environmental Satellite) antennas receive visible and infrared digitally-encoded images from the East and West GOES satellites.

ARCHIVE/PLAYBACK

The raw GOES data are stored digitally on videocassette cartridges. The playback unit allows GOES raw data to be read into the system, at any time, for user analysis.



MCIDAS SYSTEM BLOCK DIAGRAM

FIGURE-1

IBM COMPUTER (4381-2)

The IBM mainframe computer receives imagery data from the GOES antenna group or from archived tapes. The computer contains the operating system, application programs, and subroutines; it functions as a data processor, data base management system, and data analyzer.

DISK STORAGE

Currently, the SSEC McIDAS has a storage capacity of 1Ø.9 gigabytes (10.9 billion bytes). The disk storage is divided into 6999 digital areas in which several data bases reside. The following are three of the major data bases:

- Image Files
- Meteorological Data (MD Files)
- Grid Files

An Image File (area) contains digitized satellite visual data or infrared sensor data.

A Meteorological Data File is a generic file for single location observations (non-image), designed to accommodate many types of data under one generalized structure.

A Grid File contains fields analyzed at regularly-spaced latitude and longitude locations (grids) from observational data.

PROGRAMMER TERMINALS

The programmer terminals are used for ongoing development of system software.

LOCAL AREA NETWORK

The local area network (LAN) provides a high-speed (10 Mbits/sec) data link between McIDAS workstations and the IBM computer. McIDAS uses an "off-the-shelf" local area network system, called proNET™, manufactured by Proteon, Inc.

REMOTE COMMUNICATIONS CONTROLLER

The Remote Communications Controller performs the same functions as the LAN but serves remote users. Workstations are usually connected to the Remote Communications Controller by dedicated data lines maintained by commercial firms such as AT&T. The data speeds (baud rates) are generally

much lower (9600 bits/sec or less) than those of the LAN. The terms "Local" and "Remote," as applied to workstations in Figure 1, refer to the data link type rather than geographical location. SSEC may have both local and remote workstations within a single room.

CONVENTIONAL DATA INPUT

The McIDAS can ingest a wide variety of conventional weather data. This conventional data input is referred to as "point source" data and is used to maintain the Meteorological Data (MD) data base. Sources for conventional data include radiosondes, rocketsondes, ship reports, aircraft, and radar.

McIDAS WORKSTATIONS

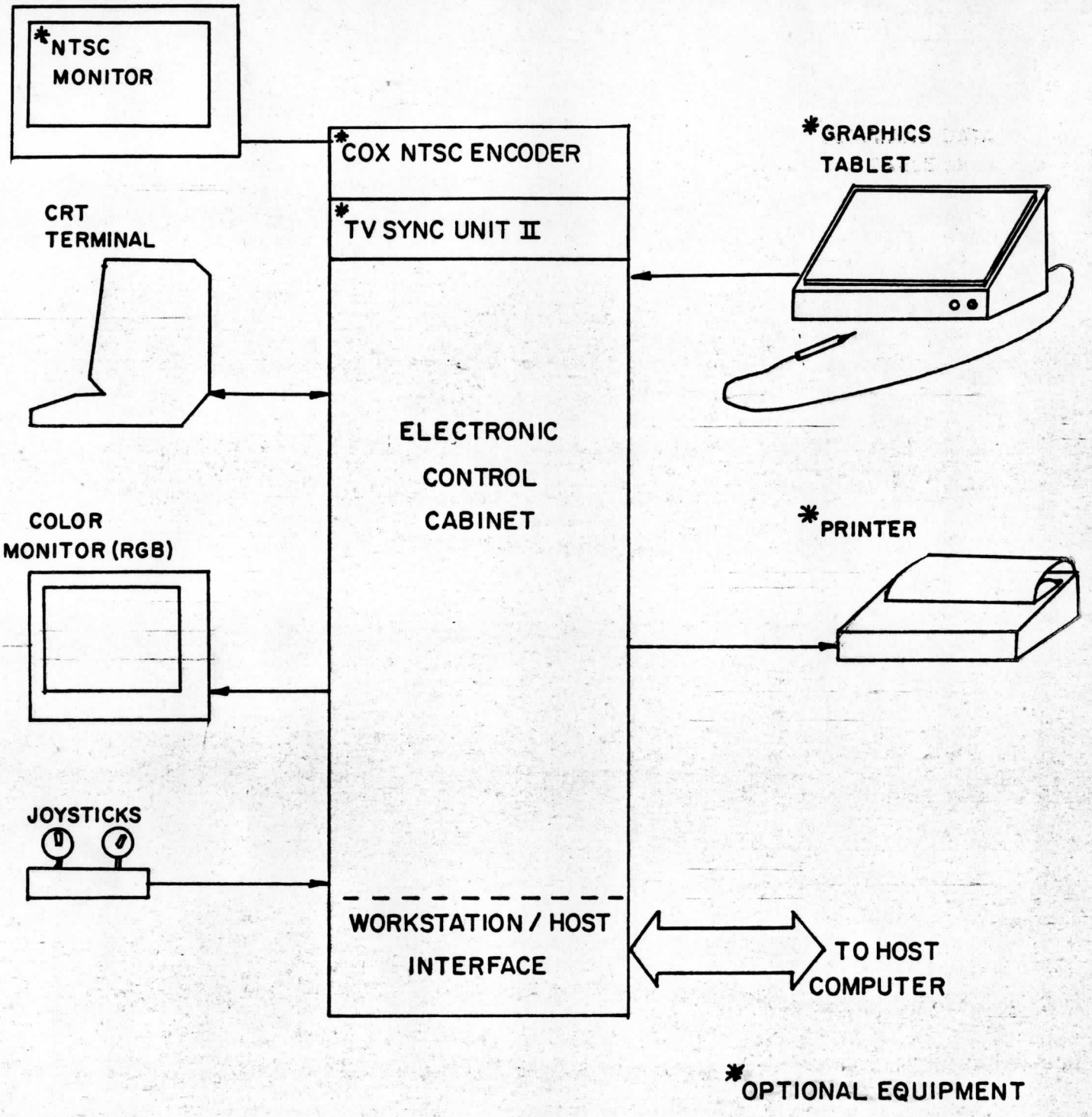
The McIDAS workstation is designed for animated display of satellite imagery and weather data. The following features are included in the workstation:

- real-time access to image and conventional data
- graphics overlays of images without image destruction
- animated displays of image or graphics frames at user-selectable looping rates of up to 15 frames/sec
- pseudo coloring of imagery
- user-selected graphics colors
- manual graphics drawing with joysticks
- satellite image combinations, forming 3-dimensional, color-enhanced images

Note that workstation features are not a function of a local or remote data link environment. Rather, workstation functions are determined by hardware configurations. (Local workstations perform most functions faster than remote workstations.)

McIDAS WORKSTATION DESCRIPTION

The Figure 2 block diagram shows the components that constitute a complete workstation. Blocks containing an asterisk (*) may be omitted in some workstations, with a corresponding reduction in workstation capability and flexibility.



McIDAS WORKSTATION-BLOCK DIAGRAM

FIGURE-2

WORKSTATION COMPONENTS

The blocks (components) in Figure 2 are individually addressed according to their functions within the workstation. Some components are standard "off-the-shelf" items and may be substituted with components of similar specifications. When these components are described, component specifications are included because make and model descriptions are more likely to change frequently.

CRT TERMINAL

The CRT Terminal provides user access to the host system. Presently, a Televideo 924 CRT terminal transmits and receives alpha-numeric characters to and from the Electronic Control Cabinet. The CRT terminal's inputs/outputs are standard eight-bit ASCII, 96ØØ baud with no parity. Operation is full duplex. The Televideo 924 is commercial equipment, documented by the manufacturer.

COLOR MONITOR (RGB)

The CONRAC 7211 is a standard RGB (red, green, blue) color monitor, used to display color and monochrome images and graphics. The inputs to the monitor are red, green, and blue drive signals and composite sync signals from the electronic control cabinet. The monitor is driven to a resolution of 64Ø picture elements (pixels) by 48Ø scan lines. The CONRAC 7211 is commercial equipment, documented by the manufacturer.

PRINTER

The printer produces hard copy maps, tables, or listings. The printer is not essential for workstation operation and therefore may be eliminated. The electronic equipment printer interface can easily be configured to accept any standard baud rate printer (from 11Ø baud to 19.2K baud) and can operate with printers both capable and incapable of keeping track of top-of-form. The printer is a serial RS-232 device. The OKIDATA Microline 93 is a standard commercial printer, documented by the manufacturer.

COMMAND DATA TABLET[1]

The data tablet is optional commercial equipment which simplifies the execution of frequently-used, complicated functions. The tablet is an X-Y coordinate device. When a user contacts the surface of the tablet with the tablet pen, the tablet generates and transmits a serial data stream containing the X and Y coordinates of the pen tip. The coordinates of the tablet are divided into areas by the host computer. Each area can be defined by the user to represent keystrokes or strings of keystrokes. When used in this manner, with an appropriate graphics tablet overlay, frequently-used, complicated functions can be executed by touching the appropriate tablet area with the pen. The tablet transmits seven-bit ASCII character coordinate data to the Electronic Control Cabinet at a rate of 19,2ØØ baud. The characters have even parity and two stop bits. The tablet presently used with the McIDAS is a "SummaGraphics Bit Pad One." Refer to the manufacturer's literature for more information.

JOYSTICKS

The Joystick module positions the cursor on the monitor. The module consists of two joystick potentiometers which supply analog position information to the Electronics Board. The Electronics Board transforms the analog input data to digital data and serially transmits this data to the Electronic Control Cabinet. Typically, the right joystick provides coarse position control while the left provides vernier (fine) control. The data is transmitted as eight-bit ASCII, with two stop bits, parity, and one start bits. The parity bit is always transmitted as a logic "one". It is not tested for even or odd parity by the receiving electronics. It is simply a filler bit.

ELECTRONIC CONTROL CABINET OVERVIEW

Figure 3 is a block diagram of the workstation, showing the Electronic Control Cabinet and external components. Except for the memory storage,

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[1]Command Data Tablet, Graphics Tablet, Data Tablet, and Tablet are used interchangeably throughout this text.

the 8Ø/24 microprocessor board, and the optional Cox NTSC Encoder, all control cabinet blocks are designed and built by SSEC.

MICROPROCESSOR

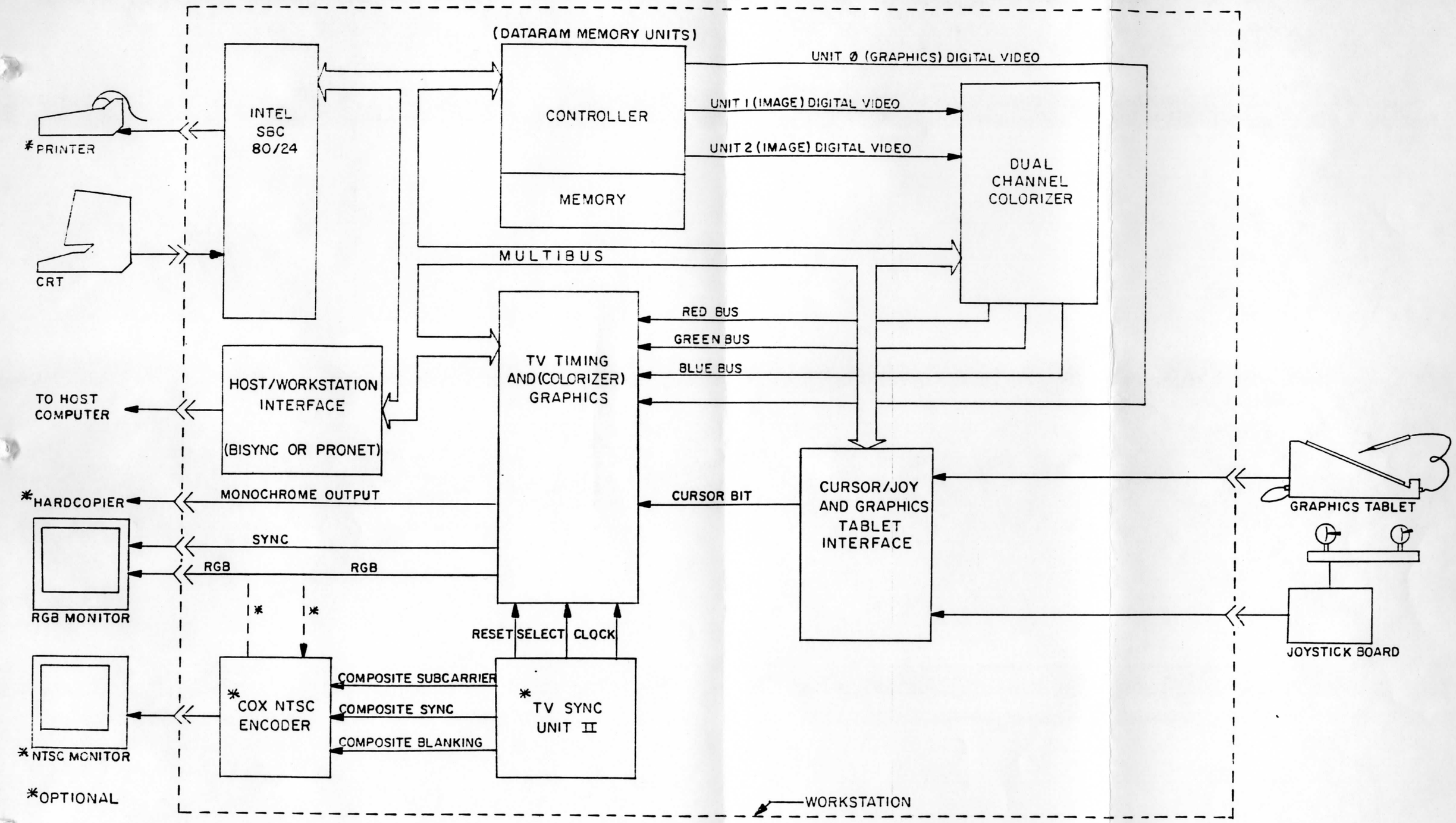
The microprocessor controls the data flow between the various boards and components in the workstation. It also controls communications between the host and workstation. The microprocessor accepts incoming alpha-numeric data from the CRT terminal, assembles the data into "packets," and initiates the "packet" transmission to the host. The microprocessor also accepts message command or data "packets" from the host, decodes the command or destination-device-address, and executes the command or data transfer.

The microprocessor is an Intel iSBC 8Ø/24 single board computer. The board is equipped with an optional RAM (Random Access Memory) module (Intel iSBC 3Ø1), providing a total 8K bytes of memory. The board supports a maximum of 32K bytes of EPROM (Erasable Programmable Read Only Memory). Three of the available four EPROM chips contain the microprocessor's instructions, constants, and most tables. The fourth EPROM chip contains only a video image compression table. (Refer to the Dual Channel Colorizer overview.) The board can directly support one serial I/O (Input/Output) device via the J3 jack and a second serial I/O device via an optional piggy-back I/O expander module (Intel iSBX 351). The J3 jack is connected to the CRT terminal while the expansion module is connected to the printer. The 8Ø/24 board uses an Intel 8Ø85A eight-bit microprocessor for the central processor unit; it performs on-board processing as well as on- and off-board control.

CABINET/CHASSIS

The Electronic Control Cabinet is a standard 19-inch electronics rack. The rack has an overall height of 56 inches, including the casters. The cabinet has an overall depth and width of 3Ø inches and 24 inches respectively. The rack has a front opening of 44 inches by 19 inches and houses the following six 19-inch modular electronic units:

- Cox NTSC Encoder (optional)
- NTSC (National Television Standards Committee) TV sync generator (optional)



FUNCTIONAL BLOCK DIAGRAM
ELECTRONIC CONTROL CABINET

FIGURE – 3

- Multibus chassis
- DATARAM memory storage (units Ø, 1, and 2)

Each module contains its own DC power supply which plugs into a switched convenience AC outlet panel, located near the bottom rear of the cabinet.

The NTSC Sync Generator and the Cox NTSC Encoder are located at the top of the cabinet (when installed) and enable the workstation to produce NTSC composite color video. The composite color video can be used to drive an optional NTSC Color Monitor and modulate a commercial TV transmitter. The NTSC TV Sync Generator is designed and manufactured by SSEC and is documented in Section 12 of this manual.

There are two versions of the Multibus chassis. Both versions consist of an enclosure containing DC power supplies and a card cage. Electronics Solutions Incorporated (ESI) built the older style enclosure, which may be seven or nine slots (MC757 or MC609 respectively). SSEC extensively modified this ESI chassis version. The boards are installed and removed from the rear of this older style Multibus Chassis. The newer version of the Multibus chassis was designed and is fabricated by SSEC. Boards are accessed through the front of these SSEC enclosures.

All boards within the card cage are interconnected by the card cage backplane, through a bus structure called Multibus^{R}. Multibus is registered trademark of Intel Corporation and has become an industry standard. The standard is now controlled by IEEE (IEEE 796). The P1-bus consists of 16 address lines, 8 data lines, control lines, interrupt lines, and bus exchange lines.

All SSEC boards, housed in the card cage, are designed to be Multibus-compatible with the P1 connector. SSEC also uses the P2 connector for various McIDAS-specific timing and video signals.

The DATARAM memory storage units are located below the Multibus chassis. A DATARAM control board, built by SSEC, is located in each of the memory storage units. The DATARAM control board connects the Multibus to the memory storage system. Additional information on the Memory Storage Unit is found in the next section of the Overview (Memory Storage System).

MEMORY STORAGE SYSTEM

The Memory Storage System consists of three separate memory storage units. One unit stores graphic overlay data while the other two units store

compressed image data. Each unit can be populated with from one to four storage array boards. Each array board provides storage for 16 frames of video data. Increasing with the number of array boards, the memory storage unit can store 16, 32, 48, or 64 graphic frames and 32, 64, 96, or 128 image frames.

In response to the significant amount of memory required for video storage, SSEC developed a memory control board that allows the microprocessor to store images and graphics in the Memory Storage Units. These data are automatically retrieved when the microprocessor addresses the unit via a frame number for read operations. Video data is stored one pixel at a time by addressing the frame number, video line number (Ø-511) and pixel position within that line (Ø-639). Video data is read sequentially beginning with the starting address and ending with the last pixel address of the frame. The read process is repeated until the user selects a different frame number. During the read process, data is read sequentially by the Control board and output to the Dual Channel Colorizer (image data) or the TV Timing and Colorizer (graphics), at TV pixel painting rates. See the manufacturer's literature for more information on the memory storage modules.

DUAL CHANNEL COLORIZER

The Dual Channel Colorizer board expands (decompresses) the two 3-bit video image channels into two 6-bit channels. The 6-bit channels are used as address inputs to an enhancement table. The table is user-programmable via the host computer. The 15 binary output bits from the table are divided into three 5-bit buses which represent magnitudes of red, green and blue (RGB) drive signals. The table provides a means to assign color drive intensities (pseudo color) as a function of the 6-bit image channel inputs, individually or in combination with each other.

TV TIMING AND COLORIZER

The RGB bus signal outputs from the Dual Channel Colorizer board are inputs to the TV Timing and Colorizer board. The 3-bit graphics bus and the cursor bit are also inputs to this board. This board does the following:

- generates all TV timing signals
- multiplexes image, graphics and cursor data

- converts the digital video into analog video, suitable for driving a standard RGB monitor
- assigns color to the graphics and cursor data

The TV timing signals are horizontal and vertical drive signals, used by frame-processing logic; PXLCK (pixel clock), used for timing and synchronization of all digital video signals; and composite sync, used by the RGB monitor.

Each pixel, as seen on the RGB monitor screen, is either an image pixel, a graphics pixel or a cursor pixel. The TV Timing and Colorizer board assigns priority to the pixel type, from highest to lowest, as follows:

- cursor
- graphics
- image

Graphics bits are processed by a color enhancement table, similar to the process by which image color enhancement is performed on the Dual Channel Colorizer board. For each cursor bit value ("Ø" or "1"), eight colors can be loaded into the table; the 15 RGB outputs of the lookup table result in 32,768 possible colors and brightness levels to choose from.

The digital RGB video data is applied to the digital-to-analog (D-to-A) converters, combined with composite sync and output to the RGB monitor. The TV Timing and Colorizer board also provides a monochrome output to drive hard copiers.

CURSOR/JOYBOARD AND GRAPHICS TABLET INTERFACE

The Cursor/Joyboard and Graphics Tablet Interface combines three unrelated functions. This board generates the cursor symbol, and interfaces the serial input joystick data and optional graphics tablet data to the microprocessor.

When the user positions the joysticks, the Joystick Board generates a serial output data stream containing cursor position information. The Joystick Interface section of this board converts the serial data stream to parallel data; parallel data is transmitted via the Multibus to the microprocessor.

The microprocessor updates its stored cursor position registers and transmits the updated values back to the Cursor Generator portion of the

board. The microprocessor also transmits cursor symbol size and shape information. The Cursor Generator uses these input parameters and TV timing signals to determine if the pixel (on the RGB monitor) about to be painted is a cursor pixel. If the pixel is a cursor pixel, a flag (cursor bit) is sent to the TV Timing and Colorizer board. The Cursor Bit is used by the TV Timing and Colorizer board to turn off the image and graphic channels during the painting of a cursor pixel.

HOST/WORKSTATION INTERFACE

The workstation is linked to the host computer either by a Bisynchronous Communications Interface (Bisync) or by proNET™.

proNET, a proprietary Local Area Network (LAN) designed and manufactured by Proteon Associates Inc., can link several workstations within a limited physical area. The "Wire Center" is a component of the proNET system. The Wire Center typically connects as many as eight workstations.

The Bisync system typically utilizes analog modem links, DDS® (AT&T Dataphone Digital Service) links or limited distance modems as part of the terrestrial link.

Differences in data transmission rates and link lengths are the primary trade-offs between the two systems. proNET is generally a local system that can transmit and receive data at rates of 1Ø Mbits per second. The Bisync system can be thousands of miles long but is generally restricted to lower data rates (96ØØ bits per second or less).

Regardless of interface type, bisynchronous or proNET, serial ASCII data is transmitted and received. Workstations using the proNET system have an additional SSEC fabricated interface component called a proNET Terminal Interface (PTI). The PTI re-formats received proNET packets to the Bisync protocol for incoming messages and vice versa for outgoing messages. Thus, the workstation's Intel 8Ø/24 firmware remains the same regardless of the communication scheme.

Host-to-workstation message transmissions consist primarily of:

- ASCII text to the CRT
- ASCII text to the printer
- graphics plotting parameters (starting points, line lengths, and directions)
- pseudo coloring table loading data
- TV image data

- cursor size, shape, and position
- image looping parameters
- graphic and cursor color palette loading data
- workstation ID number
- TV frame numbers

Workstation-to-host message transmissions consist primarily of:

- CRT keystroke characters
- workstation ID, including number of image and graphic frames available (generally ignored by the IBM host)
- TV image and graphics display status--frame number shown and upper and lower loop bounds
- raw joystick position data
- raw data tablet coordinate data

WORKSTATION SUMMARY

The workstation is best summarized by tracing a user's command through the system. For this example, assume the user wants to transfer an image frame to the workstation. Refer to Figure 4. The user types the proper sequence of characters at the CRT terminal to request the desired image from the host. (The input data format is located in the McIDAS APPLICATIONS GUIDE.) The alpha-numeric command enters the 8Ø/24 Microprocessor board on J3. The microprocessor formats the command into a message packet and transfers the packet to the Host/Workstation Interface. Assuming a Bisync interface system, the packet is loaded into a "transmit buffer." Now, the microprocessor initiates the transmission by issuing a command word to the Bisync board. Once initiated, the Bisync board automatically transmits each character in the "transmit buffer." The host deciphers the received packet, determines that the workstation has requested an image frame, and transmits the image, line by line.

The host forms each image line into a 642-byte packet, consisting of a two-byte image line number and 64Ø six-bit pixel data values. The host transmits the packets to the workstation's receive buffer, located in the Host/Workstation Interface. Periodically, the microprocessor reads the status of the Bisync board and, upon detection of a "message received" status, transfers the message packet from the "receive buffer" to the 8Ø/24 board. The microprocessor strips the "image line number" from the message packet and transfers this data to the appropriate Memory Storage

Unit's DATARAM control board. The DATARAM control board loads the image line number into the pixel address generation section of the DATARAM control board. Now, the microprocessor processes each of the 64Ø six-bit pixel data values in a compression algorithm. The algorithm reduces the 6-bit pixel data to 3-bit pixel data, thereby reducing the memory storage requirements by 5Ø%. After each pixel is processed, it is transferred to the DATARAM control board which loads the pixel into memory and increments the pixel address counter. This process continues until each of the 64Ø pixels have been processed and stored. For each image frame, a total of about 49Ø packets (as described above) are transferred from the host and processed and stored by the workstation.

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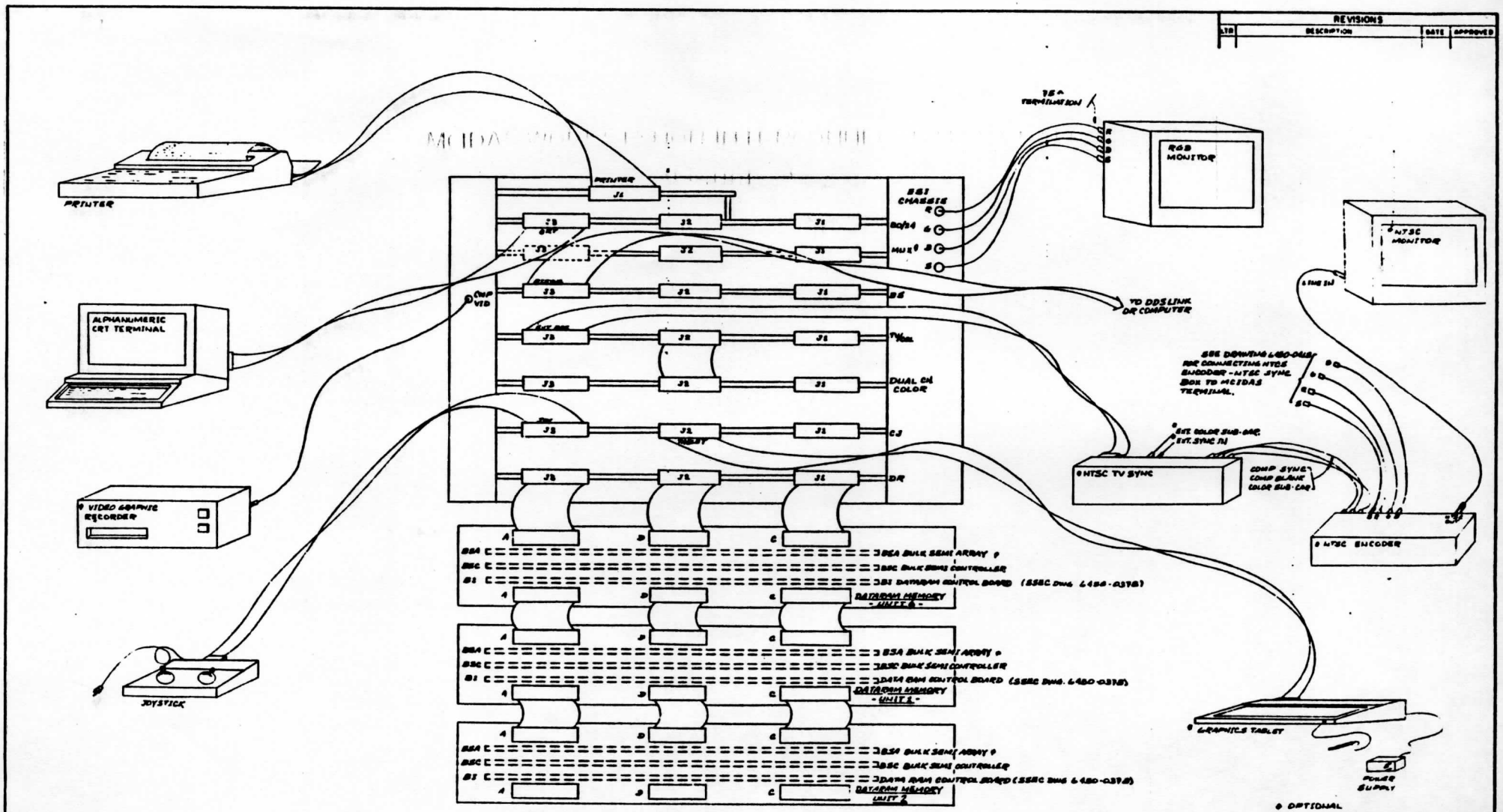

McIDAS WORKSTATION INTERCONNECTION DIAGRAM

FIGURE - 4

SECTION 2
SINGLE BOARD COMPUTER
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SINGLE BOARD COMPUTER

INTRODUCTION

The Single Board Computer consists of an Intel® iSBC 8Ø/24™ single board microcomputer and an iSBX 351™ serial I/O expansion board. This document provides only a functional overview of the Single Board Computer. For complete hardware documentation of the iSBC 8Ø/24™, see Intel®'s iSBC 8Ø/24™ SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL (Manual order number 142648-ØØ1). The iSBX 351™ is documented in Intel®'s iSBX 351™ SERIAL MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL (Manual order number 98Ø319Ø-Ø2). Note: Intel, iSBC, iSBX, Multibus and Multimodule are registered trademarks of Intel Corporation.

For a more complete understanding of the McIDAS workstation and system, it is necessary to understand the workstation/host interface protocol, the workstation operational firmware[1] and the diagnostic firmware. The workstation/host interface protocol is described in the SSEC document, HOST TO TERMINAL - TERMINAL TO HOST SYSTEM PROTOCOL DESCRIPTION, dated 11 September 1984.

The operational and diagnostic firmware is documented in the McIDAS WORKSTATION FIRMWARE DESCRIPTION.[2]

HARDWARE FUNCTIONAL DESCRIPTION

The 8Ø/24 and 351 provide the processing power necessary to oversee all workstation processes and maintain a communications link between the host computer and the workstation. These boards receive data from the host's control processing unit (CPU), steer it to the proper workstation

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[1]The term "firmware" describes programs stored in non-volatile EPROM that may be altered by the user.

[2]This document is not yet completed. It will be forwarded to you upon completion.

device, and collect status information and data from that device, packing it into a message for transmission to the host.

The 8Ø/24 board is built around the Intel 8Ø85A microprocessor chip. The address, data, and control lines of the microprocessor are not only connected to other on-board chips, they are connected to most other electronic control cabinet boards via the Multibus and Multibus interface logic. Note: For additional information on the Multibus, refer to Intel's MULTIBUS® DATA BOOK (Order number 21Ø893-ØØ3).

The iSBC 8Ø/24™ board (referred to as the "8Ø/24") is a Multibus- and Multimodule-compatible computer system. The board contains 8K bytes of RAM (4K bytes of on-board RAM plus 4K bytes from optional RAM iSBC 3Ø1 RAM) and 32K bytes of erasable-programmable-read-only-memory (EPROM). The board has six 8-bit I/O ports and one programmable serial communications channel. In the McIDAS, a second programmable serial communications channel is provided by plugging a Multimodule iSBX 351 board (referred to as the "351") into the 8Ø/24.

Figure 1 is a functional block diagram of the iSBC 8Ø/24, including the iSBC 3Ø1 RAM expansion module and the iSBX 351 I/O expansion module.

MICROPROCESSOR

The microprocessor executes the commands of the workstation firmware package. The microprocessor goes to the EPROM memory block, retrieves the instruction to be executed, and carries out the assigned task. The 8Ø85A microprocessor deciphers the instructions and initiates their execution.

MEMORY AND I/O MAPPING

All controllable devices external to the microprocessor are assigned a memory address or an I/O address. The Memory and I/O Mapping block in Figure 1 generates the device-enabling signals by processing the microprocessor's address bus output and IO/M/ control signal. This control signal is high when the microprocessor performs an I/O read or write operation and is low when it performs a memory read or write operation. I/O read and write operations (also known as port read and write) consist of eight binary bits which represent port addresses of ØØH-FFH

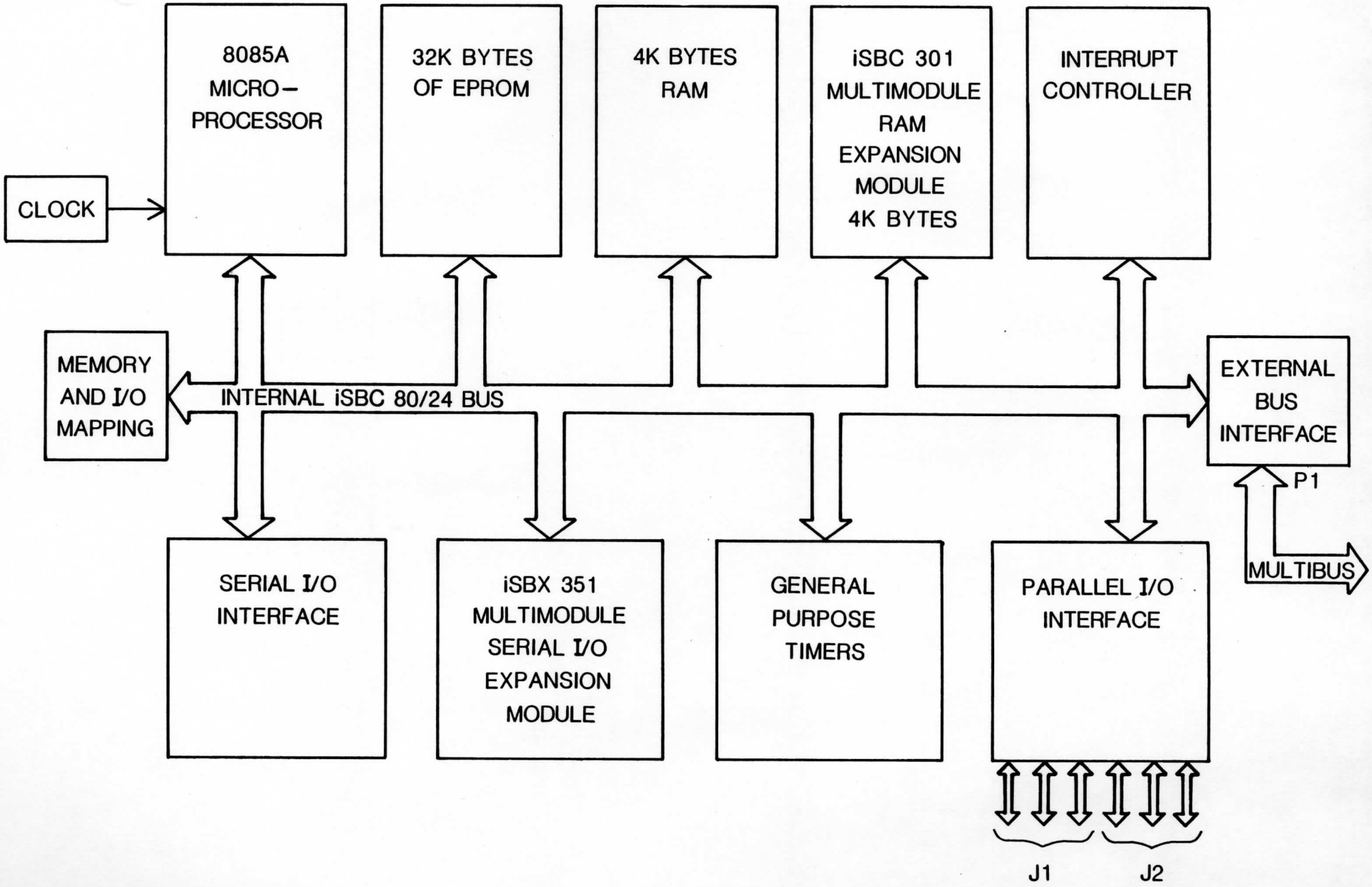


FIGURE 1. MICROPROCESSOR BOARD FUNCTIONAL BLOCK DIAGRAM

(hexadecimal). Memory read and write operations use all 16 address bus lines (ØØØØH-FFFFH). The memory and I/O mapping block only provides address deciphering for on-board memory and I/O devices. Each device external to the 8Ø/24 board (off-board) that is addressable by the microprocessor (via the Multibus) must provide its own memory or I/O mapping logic. The External Bus Interface provides the Multibus with all address and control lines necessary to perform memory and I/O mapping.

The iSBC 8Ø/24, iSBC 3Ø1, iSBX 351, and all other workstation boards and devices are memory and I/O mapped, as shown in Table 1 below.

ADDRESS/PORT	I/O-MEMORY	FUNCTION
ØØØØH - 5FFFH	Memory (EPROM)	Instruction code (8Ø/24)
6ØØØH - 7FFFH	Memory (EPROM)	Video compression (8Ø24)
8ØØØH - 9FFFH	(not used)	
AØØØH - BFFFH	Memory (RAM)	General (8Ø/24)
CØØØH - EFFFH	Memory	Dual channel colorizer enhancement tables
FØØØH - F7FFH	Memory	Bisync communications buffers
F8ØØH - FBFFH	(not used)	
FCØØH - FC29	Memory	DATARAM control addresses
FC2A - FEFFH	(not used)	
FFØØH - FF3F	Memory	Graphics enhancement palette
FF4Ø - FF7F	Memory	Cursor enhancement palette
FF8Ø - FFFF	(not used)	
7ØH	I/O (Input)	Cursor/Joy and Data Tablet Interface Data Tablet MSBs Vertical Position
71H	I/O (Input)	Cursor/Joy and Data Tablet Interface Data Tablet LSBs Vertical Position
71H	I/O (Output)	Dual Channel Colorizer - Graphics Enable
72H	I/O (Input)	Cursor/Joy and Data Tablet Interface Data Tablet MSBs Horizontal Position
72H	I/O (Output)	Dual Channel Colorizer - Cursor Enable

73H	I/O (Input)	Cursor/Joy and Data Tablet Interface Data Tablet LSBs Horizontal Position
74H	I/O Input	Cursor/Joy and Data Tablet Interface Data Tablet Pen Status
75H		TV Timing and Colorizer Vertical Interval
76H	Not used	
77H	I/O (Input/Output)	Bisync Control
78H - 7FH	I/O (Output)	Cursor/Joy and Data Tablet Interface Cursor Size and Control
78H - 7FH	I/O (Input)	Cursor/Joy and Data Tablet Interface Joystick Position Data
8ØH - AFH	(not used)	
BØH	I/O (Output)	Dual Channel Colorizer - Unit 1 and 2 LSBs of Unit 2 Select Mask
B1H	I/O (Output)	Dual Channel Colorizer - 4 MSBs of unit 2 Select Mask and Control
B2H	I/O (Output)	Dual Channel Colorizer - Unit 1 and 2 LSBs of Unit 2 Invert/Normal Control Mask
B3H	I/O (Output)	Dual Channel Colorizer - Unit 2, 4 MSBs of Invert/Normal Control Mask
B4H	I/O (Output)	Dual Channel Colorizer - Not used
B5H - DBH	I/O	(Not used)
DCH	I/O (Input/Output)	8Ø/24 - Timer #Ø Read/Load
DDH	I/O (Input/Output)	8Ø/24 - Timer #1 Read/Load
DEH	I/O (Input/Output)	8Ø/24 - Timer #2 Read/Load
DFH	I/O (Output)	8Ø/24 - Timer Mode Control
E4H	I/O (Input)	8Ø/24 - iSBX 351 Baud Rate Select (Line Printer)
E5H	I/O (Input)	8Ø/24 - Number of Image Frames
E6H	I/O (Input)	8Ø/24 - Number of Graphics Frames
E7H	I/O	(Not used)
E8H	I/O (Input)	8Ø/24 - Workstation ID Number

ECH	I/O (Input/Output)	8Ø/24 - USART Data (CRT)
EDH	I/O (Input/Output)	8Ø/24 - USART Command/Status
EEH-EFH	I/O	(Not used)
FØ1H	I/O (Input/Output)	8Ø//24 - iSBX 351 USART Command/Status
F1H	I/O (Input/Output)	8Ø//24 - iSBX 351 USART Data (Line Printer)
FA	I/O (Input/Output)	8Ø/24 iSBC 351 Timer #2 Control
FB	I/O (Output)	8Ø/24 iSBC 351 Timer Mode Control

Table 1. Memory and I/O Mapping

EPROM

The first 24,576 (ØØØØH - 5FFFH) bytes of EPROM are used by the microprocessor for non-volatile instruction storage. Included in this block are tables and constants. The last 8192 bytes of storage (addresses 6ØØØ - 7FFF) make up a special table used to compress the image data from six bits per pixel to three bits per pixel. The compression process reduces image storage requirements by half.

RAM and iSBC 3Ø1

Together, the RAM block and the iSBC 3Ø1 block constitute an 8192-byte static RAM. The RAM stores variables, system configuration, status and other scratch pad data.

SERIAL I/O INTERFACE

The Serial I/O Interface block provides a serial RS-232C communications link to an external device. In the McIDAS, the external device is the CRT terminal. The baud rate is software-programmable via the on-board timer (see the General Purpose Timer description below).

GENERAL PURPOSE TIMER

The general-purpose Timer block contains three independent timers. The timers are software-programmable and may be configured as frequency generators, interval timers, and real-time interrupt generators. One of the timers is the baud rate clock for the Serial I/O Interface.

iSBX 351 MULTIMODULE SERIAL I/O EXPANSION MODULE

The iSBX 351 module plugs into one of the two expansion connectors (J6) on the 8Ø/24 board. The module provides an additional serial I/O interface channel very similar to the on-board Serial I/O Interface block described above. Baud rates, data formats, and interrupts are jumper- and program-selectable on the Multimodule board. The iSBX 351 has its own on-board timer for baud rate, frequency, and timing functions. The timer has three independent channels. Only one timer is required for the iSBX 351 on-board timing functions, leaving the remaining two for general purpose use. In McIDAS, timer #2 is used while timer #1 is an unused spare (timer #Ø is used by the iSBX 351).

PARALLEL I/O INTERFACE

The Parallel I/O Interface block provides six general-purpose 8-bit parallel I/O ports. In McIDAS, only five ports are used. All ports are configured as inputs ports only. Ports E4, E5, and E6 are connected to jack J1 while E8, E9, and EA are connected to jack J2. Programming plugs, connected to J1 and J2, are used to program the selected port input pins. During initialization, performed by the microprocessor immediately after a power turn-on or system reset, the microprocessor reads ports E4, E5, E6, E8 and E9 to determine the following:

- number of video frames
- number of graphics frames
- graphics tablet presence and size
- printer baud rate
- system AC power frequency (5Ø hz or 6Ø hz)
- workstation ID number

INTERRUPT CONTROLLER

The microprocessor can directly control four interrupt sources. In McIDAS, all four direct sources are grounded (disabled). The Interrupt Controller block can control eight additional interrupt sources (indirectly). The Interrupt Controller contains an integral priority scheme which arbitrates contention among interrupts. Jumpers connect system interrupts to the selected interrupt priorities. In the McIDAS, three interrupt sources are controlled by the Interrupt Controller. The

Vertical Interval on the TV Timing and Colorizer board generates a rate of 3Ø interrupts per second (INTØ/). These interrupts have the highest priority. The CRT Terminal input data is the second highest priority interrupt rate source. Timer #Ø generates the programmable interrupt rate with the lowest priority.

The only Multibus-transported interrupt signal used by the 8Ø/24 is INTØ/, generated on the TV Timing and Colorizer board. The 8Ø/24 board is shipped from the factory with default jumpers installed. As shipped, INT2/ is the only Multibus-transported active interrupt. The proNET Terminal Interface (PTI) card acts as a bus master, using INT2/ as an interrupt from the proNET HSBM board. In McIDAS workstation applications (using proNET), the INT2/ activation jumper must be removed and the jumper which activates INTØ/ must be installed, so that both boards do not use the same interrupt signal. The proNET system does not use INTØ/. After the INTØ/ jumper is installed on the 8Ø/24 board, an interrupt from the proNET system will have no effect outside that system. Similarly, a Vertical Interval interrupt (INTØ/) affects only the 8Ø/24 board.

For complete configuration of the iSBC 8Ø24 and the iSBX 351 refer to the McIDAS DESIGN NOTE INTEL 8Ø24 and iSBX Board Configuration. The design note is part of your original documentation package.

SECTION 3
DUAL CHANNEL COLORIZER
TABLE OF CONTENTS

DUAL CHANNEL COLORIZER
(SSEC DRAWING 35Ø4-ØØ5, MODIFICATION B, DATED 5/3/84)

INTRODUCTION

The Dual Channel Colorizer performs the following three major functions on the compressed data from the two image storage units in the DATARAM:

- data decompression
- user interaction with image data processing
- user interaction with color enhancement processes

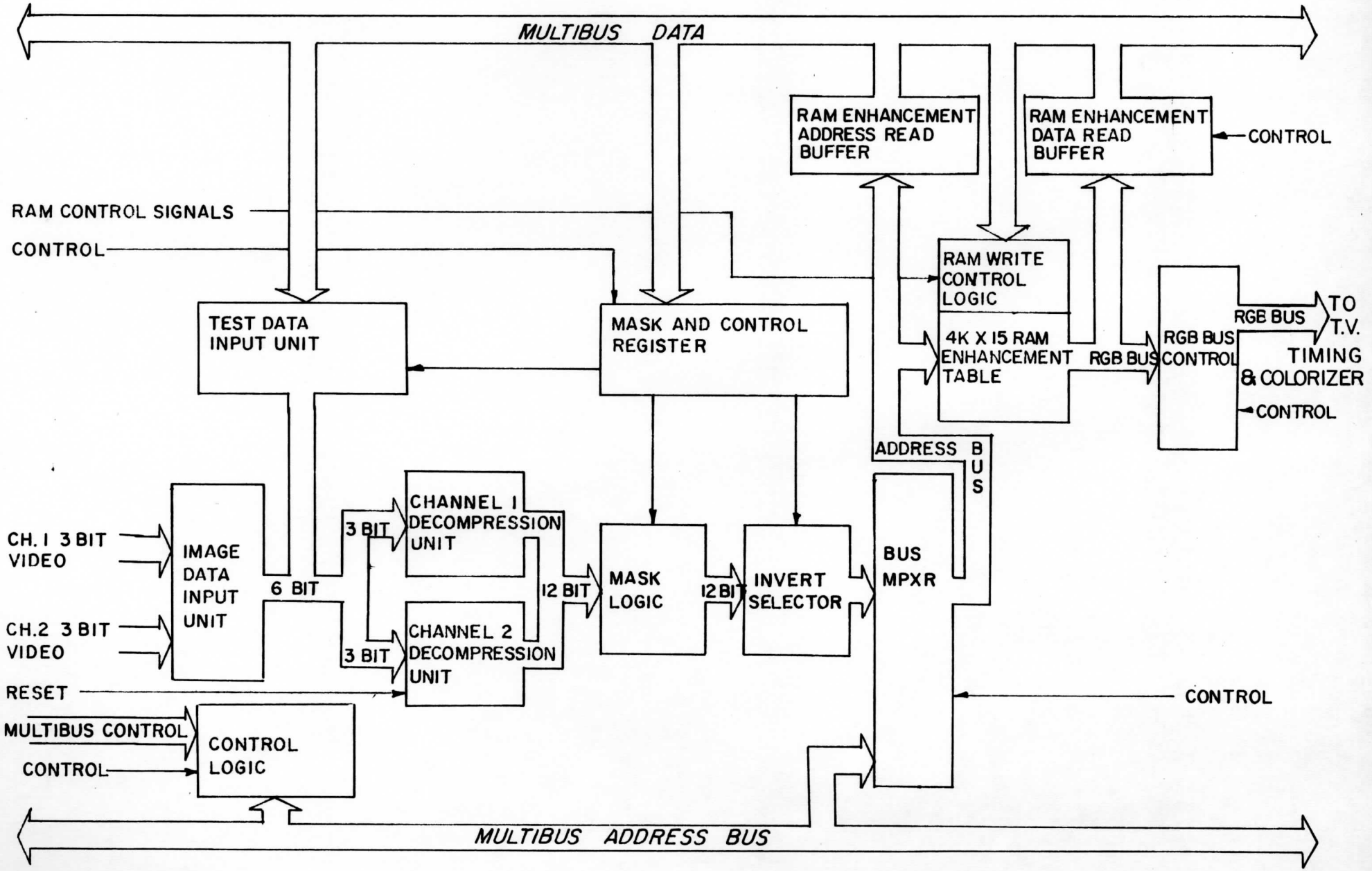
An image picture contains approximately 313,600 pixels, each of which originally is represented by a six-bit binary code (64 brightness levels). If this format is used, over two million bits of storage are required to store each image picture. To reduce storage requirements by half, the six-bit real data values are compressed into three-bit "partitions." The microprocessor executes the compression algorithm when it moves the data from the communications buffer to the DATARAM storage unit. The three-bit partition values are stored in the workstation, reducing the memory requirement by half. Data decompression is the process of reconstituting the six-bit digital image data from a compressed three-bit partition code.

Pixel-by-pixel decompression is performed simultaneously on two pictures. Through user interaction, either or both picture(s) can be selected, masked according to video intensity, combined or processed by combinations of the above actions.

The last major function of the Dual Channel Colorizer is color enhancement of the dual channel video data. The user can define a "gray scale level" to "color hue and brightness" relationship for each video channel individually and for two combined video channels. This function allows a greater volume of image data with more rapid analysis than is possible with a monochrome image.

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the Dual Channel Colorizer.



DUAL CHANNEL COLORIZER FUNCTIONAL BLOCK DIAGRAM

FIGURE 1

(3504-005)

The inputs to the Image Data Input Unit are the compressed three-bit/channel (six bits total) image data from the two DATARAM image storage units. The output of the Image Data Input Unit shares a common bus with the Test Data Input Unit. The Image Data Input Unit converts the dual channel input data to TTL logic levels and outputs the data onto the six-bit multiplexed bus. The Test Data Input Unit is not implemented in firmware. It was designed to allow a user or technician to inject known values into the Decompression Units for verification of proper operation. However, a gray scale diagnostic accomplishes the same thing.

Two identical state machines are used to decompress the two 3-bit channels into two six-bit channels. The only input to the state machines, other than the input data, is internal feedback of the previous output data (the previous pixel brightness level).

The six-bit decompressed data are passed to the Mask Logic block, which can turn off any of the decompressed input data lines via the Mask and Control Register block. The output from the Mask Logic block is applied to the Invert Selector block.

The Invert Selector block can invert the data on any data input lines, as commanded by the Mask and Control Register block. However, this hardware feature is not implemented in firmware. Note, this is a "useless" function in the sense that data can (in some diagnostics) be inverted by the enhancement table.

The Mask and Control Register receives data from the Multibus and latching signals from the Control Logic Unit. The Mask and Control Register can store (latch) up to 25 mask and control bits; 12 are used by the Mask Logic Unit, 12 are used by the Invert Selector Unit and one controls the Test Data Input Unit. Currently, the Mask and Control Register is used as a channel selector, enabling or disabling all data bits of each channel.

The 12-bit output from the Invert Selector Unit is applied to one input of a Bus Multiplexer. The other Bus Multiplexer input is driven by the Multibus address bus. The Multiplexer output is an address bus for the RAM Enhancement Table. When driven by the Multibus, the multiplexed address bus selects a RAM Enhancement Table cell to be written into. The data to be written into the table cell come from the Multibus data bus. When driven by the Invert Selector, the multiplexed address bus selects a cell in the Enhancement Table from which data are read.

The Enhancement Table is a 4K by 15 static RAM and functions as a programmable look-up table. The output of the table is the origin of the RGB (Red, Green, and Blue) bus. The Invert Selector output (12-bit, dual-channel decompressed video) represents video intensity and is applied as an address to the Enhancement Table via the Multiplexer. Note, in single channel operation, six bits are masked off. The 4Ø96 possible combinations of video intensities can address 4Ø96 different 15-bit locations. In each location, five bits are used for each of the three color drives. When the user pre-programs the intensities of these colors, each video intensity input corresponds to a particular RGB output.

The RGB Bus Control is a tri-state latch. The latch is controlled by a signal from the TV Timing and Colorizer Board (SSEC 35Ø4-ØØ7 sheet 2 of 4). The RGB Bus Control allows the TV Timing and Colorizer board to turn off the RGB bus during the painting of graphics or cursor pixels, thereby assigning the Dual Channel Colorizer image data the lowest priority of the three video data types (image, graphics and cursor).

The RAM Enhancement Read Buffer allows the user or technician to examine the 15-bit digital output (RGB) from the RAM Enhancement Table. This feature normally is used while injecting known inputs into the Test Data Input Unit and observing the outputs from the RAM Enhancement Data Read Buffer.

The Control Logic block contains line drivers and receivers, memory and I/O mapping and associated logic circuits that generate the control and gating signals for most of the board.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the Dual Channel Colorizer is shown on SSEC drawing #35Ø4-ØØ5 (Modification B, dated 5/3/84). The schematic circuit analysis is accomplished by analyzing groups of components, represented by a single block in Figure 1 above.

SCHEMATIC CONVENTIONS

When reference is made to the schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and the section letter designator. The symbol ID number alone is used to refer to single section ICs.

CONTROL LOGIC

Most of the Control Logic is found on sheet 3 of the schematic diagrams. Most circuits on the Dual Channel Colorizer board are either memory or I/O mapped. Therefore, the primary objective of the Control Logic analysis is to determine which outputs are memory mapped, which are I/O mapped, and which addresses activate each signal.

All control signals are derived from four Multibus control signals and the Multibus address bus. The following are control signals:

- MRDC/ (Memory Read Command inverted)
- MWTC/ (Memory Write Command inverted)
- IORC/ (I/O Read Command inverted)
- IOWC/ (I/O Write Command inverted)

The upper eight bits of the address bus are buffered and inverted by Octal tri-state buffer L33 and applied to mapping PROM R33. A list of the three outputs from R33, their addresses and their primary uses follows:

- MW, CØØØH-DFFFH, Enhancement Table (read and write)
- OW, ports BØH-B3H, Mask and Control Read Buffer (read)
  Mask and Control Register load (write)
- TSTPRT, port B4H, Test Data Input Buffer (write)

MW, OW, and TSTPRT are combined, by a 3-to-8 line decoder and several gates, with the four Multibus control signals to form 12 different control signals, used throughout the board.

Each of the Multibus control signals pass through inverting buffers (E35-A, -B, -C, and -D) before they are applied to the control logic. For the following analysis, the control and mapping signals are replaced by single letters (and converted back when necessary). Therefore, let:

- MWTC = A
- MRDC = B
- IOWC = C
- IORC = D
- TSTPRT = E
- MW = F
- OW = G

With the above substitutions, the output from E27-A is FA and the output from E27-B is CG. FA and CG are inputs to NOR gate C35-C and yield an output of FA+CG/. To derive the output from E19-A, we must determine

the composition of STRBEN. STRBEN is the output from NOR gate C35-D, which is driven by E19-D (MEMRD) and inverter C27-A. The output of E19-D is BF while the output of C27-A comprises D, G, C, and E as follows: C11-A output is DG and C11-B output is CE. This results in an output from C35-B of DG+CE/. Therefore, the output from inverter C27-A is DG+CE/. DG+CE is NORed with BF by NOR gate C35-D, thus STRBEN = DG+CE+BF/. STRBEN is ANDed with FA+CG by AND gate E19-A to produce (DG+CE+BF/)(FA+CG/). The output from E19-A is inverted by inverter C27-E to produce DG+CE+BF+FA+CG.

** IMPORTANT **

C27-E has an active high output during all valid memory or I/O commands to this board. Translating the term DG+CE+BF+FA+CG back to real commands yields the following:

- DG = I/O reads to ports BØH-B3H
- CE = I/O writes to port B4H
- BF = Memory reads to addresses CØØØH-DFFFH
- FA = Memory writes to addresses CØØØH-DFFFH
- CG = I/O writes to ports BØH-B3H

C19-A, -B and A19-A form a cascaded three-stage D-latch register. The output from C27-E drives the input of C19-A as well as the clear (CLR) inputs of C19-A and C19-B. Because the latches are clocked by PXLCK, a high output from C27-E appears at the following points:

- C19-A output after one PXLCK clock pulse
- C19-B output after two PXLCK clock pulses
- A19-A output after three PXLCK clock pulses

When C27-E returns to a low output, C19-A and -B clear immediately and A19-A clears on the next PXLCK clock pulse. The latches provide input timing signals to three circuits: the AMC/ generator, the XACK/ generator and 3-to-8 line decoder J3. AMC/ is the control signal that controls the enhancement table Address Multiplexer. When AMC/ is high (inactive), the bus is driven by the Invert Selector; when AMC/ is low (active), the bus is driven by the Multibus address bus. AMC/ is active low if either of its inputs are high. Pin 3 of C35-A (MEMRD) is high during a memory read to addresses CØØØH-DFFFH. During this time, either RE_1/ or RE_2/ are enabled, enabling the RAM Enhancement Read Buffers, thus allowing RAM Enhancement Table data onto the Multibus data bus. Pin 2 input to C35-A

is driven by C11-C. Pins 9 and 1Ø of C11-C are qualified high for two PXLCK periods during all valid inputs to this board. DG+CE+BF+FA+CG is the logic expression at the output of C27-E that causes pins 9 and 1Ø to be a logic high simultaneously. C11-C pin 11 is driven by NOR gate C35-B. This gate generates a logic "zero" for the terms DG and CE. If we extract these terms from DG+CE+BF+FA+CG, the logic expression that generated a high at C11-C pins 9 and 1Ø, we have BF+FA+CG. Translated back to real terms, AMC/ is active low during memory reads and writes to addresses CØØØH-DFFFH or I/O writes to port addresses BØ-B3H.

A second output of the latches goes to the XACK/ generator. NAND gate A27-C goes active low on the third pixel clock following an active high on C27-E. The output of OR gate C3-D goes low when A27-C goes low and there is an IORC, IOWC, MRDC or MRWC control signal active. When C3-D goes low, G35-F pulls the XACK/ line down, informing the CPU that the command was completed.

The third output from the latches enables 3-to-8 line decoder J33. J33 is enabled by driving pins 4 and 5 low while driving pin 6 high. Pins 4 and 5 are normally low and remain low until the third pixel clock following a high at C27-E output. AND gate E19-B is qualified on the second pixel clock after C27-E goes high, when STRBEN is high. Thus, J33 is qualified between the rising edge of pixel clock pulse two and the rising edge of pixel clock pulse three, when STRBEN is high. STRBEN (C35-D output) is produced by NORing C27-A output with MEMRD (DG+CE+BF). The output of C27-E is DG+CE+BF+FA+CG, so the only signals which qualify C27-E and therefore J33 pins 4 and 5, without driving E19-B (STRBEN input) low, are FA and CG. Translated, FA is Memory write to addresses CØØØH-DFFFH and CG is I/O write to port addresses BØH-B3H. It is only during these times that J33 can be qualified and then only during the time between pixel clock two and pixel clock three, following a high at E27-E.

J33, the 3-to-8 line decoder, produces two memory-mapped and four I/O-mapped outputs. The A and B inputs (pins 1 and 2 respectively) are driven by buffered Multibus address lines ADRØ and ADR1 respectively. The C input (pin 3) is driven by E27-A and is active high for memory writes to addresses CØØØH-DFFFH. The table below shows the inputs and outputs of J33.

Memory Write

CØØØH-CFFFH	ADR1	ADRØ	Output (Active low)
Ø	Ø	Ø	$Y_Ø$ (Port BØ)
Ø	Ø	1	Y_1 (Port B1)
Ø	1	Ø	Y_2 (Port B2)
Ø	1	1	Y_3 (Port B3)
1	Ø	Ø	Y_4 (CØØØH)
1	Ø	1	Y_5 (CØØ1H)
1	1	Ø	Y_6 (CØØ2H)
1	1	1	Y_7 (CØØ3H)

AND gate E27-C ORs the active low outputs from Y_5 and Y_7 (all memory write odd addresses from CØØ1H-DFFFH) while AND gate E27-D does the same with Y_4 and Y_6 (all even memory write addresses from CØØØH-DFFEH). The outputs from the two gates are the active low memory write enable signals used by the RAM Enhancement Table. Because the table is organized as a 4K by 15-bit RAM and the Multibus can only supply eight data bits to the RAM at one time, each memory location must be programmed in two write operations. WE1/ loads the Red magnitude and two MSBs of the Green magnitude while WE2/ loads the three LSBs of the Green and all of the Blue magnitude.

The $Y_Ø$-Y_3 outputs from J33 can only occur during I/O write operations to port addresses BØH-B3H. During this time, the C input to J33 is "zero" and ADRØ-ADR1 determine the specific output, as indicated in the table above. All four outputs are control signals used by the Mask and Control Register.

The four control signals which have not been discussed yet are RE_1/, RE_2/, B1RD and BØRD. RE_1/ and RE_2/ are memory reads to addresses CØØØH-DFFFH and are control signals used by the RAM Enhancement Data Read Buffer.

Two control signals are required for the same reason that two memory write signals are required. In fact, RE_1/ reads the same half of memory that WE1/ can write to, and the same is true for RE_2/ and WE2/. RE_1 is generated by NANDing MEMRD with ADRØ (A27-A), thus producing an active low on

memory reads to all odd addresses, CØØ1H-DFFFH. NAND gate A27-B combines MEMRD with ADRØ/ to generate the even address control signal RE_2/. B1RD and BØRD are control signals used by the RAM Enhancement Address Read Buffer. C11-A produces an active high during I/O reads to port addresses BØH-B3H. NAND gates E11-A and E11-B combine the C11-A output with ADRØ and ADRØ/ respectively to produce odd address and even address I/O reads, as RE_1/ and RE_2/ do above.

IMAGE DATA INPUT UNIT

Refer to sheet 4. Image data enters the board from the two image data storage units via the P2 bus. Channel 1 supplies three bits to quad line receiver AK33 while channel 2 supplies its three bits to quad line receiver AM33. The line receivers convert the input signals to TTL levels and output them onto a six-bit multiplexed bus. This line receiver (AM26LS33) has a tri-state output and requires a high level on pin 4 (EN) and a low level on pin 12 (EN/) to activate its output. X2, the test data input unit and also a tri-state device, provides a test data injection capability at the multiplexed bus. The control signal TSTEN controls both tri-state devices, by disabling X2 and enabling AK33 and AM33 when TSTEN is low (TSTEN/ is high) and doing the converse when TSTEN is high.

TEST DATA INPUT UNIT (not implemented in Firmware)

This unit (X2) is connected to the buffered data bus (BDØ-BD7) and latches the Multibus data on the rising edge of the clock input (pin 11). The clock input is driven by TDL (Control Section-see sheet 3 of the schematic, bottom center) which is active during I/O writes to port address B4H. The latched data in X2 is available at the output only while the tri-state control (OC, pin 1) is low. This pin is driven by TESTEN/. TESTEN/ is an inverted output (inverted by NAND gate E11-C) from the Mask and Control Register. For more information on the generation of TSTEN, refer to the circuit description of the Mask and Control Register section.

DECOMPRESSION UNIT

The Decompression Units are shown on sheet 4 of the schematics. The two identical decompression state machines share a data input D-latch (AM22); each contains two PROMS and a feedback D-latch. Channel 1 consists of PROMS AM3 (generates the four LSBs) and AP3 (generates the two

MSBs) and latch AK3. The channel 2 counterparts are AM12, AP12 and AK12. These state machines outputs form all but the three least significant address inputs for the next data input. The three address LSBs are driven by the compressed data partitions stored in the DATARAM. The two PROMS in each state machine function as a single six-bit by 512 RAM look-up table PROM. Note that D-latches AK3 and AK12 are clocked by PXLCK, thus the present PROM outputs become address inputs after the next PXLCK.

The state machine must always start in a known state. The input data stream consists of horizontal scan lines of video, thus the state machine must always be reset to state Ø before starting a new horizontal line. Currently, the state machines are reset to "zero" simply by supplying several pixel partitions of "zero" to each state machine at the end of each horizontal scan line. The states within the state machine are designed so that a maximum of five consecutive "zero" value partitions always cause a return to state "zero". In the present configuration, the output of AD33 is always low, enabling latches AK3 and AK12 continuously.

The output from each state machine is decompressed image data, a six-bit number; it designates the current state of the state machine. This current state (fed back as the six MSB address inputs after the next PXLCK), together with the next partition (the three LSB address inputs), form the new address to the PROMS and advances the machine into a new state. Table 1 is the composite PROM state table which, for discussion, has been converted from hexidecimal to decimal. As an example, assume that the state machine currently has an output of 17 and the next two incoming partitions are six and five. By reading down the "Gray Value" row to 17 (current output) and then across to the partition 6 column, the result is an output of 26. The 26 is not only an output, it also selects the next "Gray Value" row, 26. When the next partition comes in (five), read down the partition 5 column to row 26 to find the next output, 3Ø. Thus, with an initial output of 17 and partitions of six and five as inputs, the next two outputs are 26 and 3Ø.

With this much information about the decompression process, we can actually infer the compression algorithm without reading any of the code. Compression is a process of determining which partition yields the closest value on a given "Gray Value" line (refer to Table 1). When a value is determined by the algorithm, that value determines the "Gray Value" line

Gray Value	Partition 0	1	2	3	4	5	6	7
0	0	1	4	15	27	39	51	63
1	0	1	2	5	10	33	56	61
2	1	1	3	6	11	34	57	62
3	2	3	4	7	12	35	58	63
4	0	3	4	5	8	13	36	59
5	1	4	5	6	9	14	37	60
6	2	5	6	7	10	15	38	61
7	3	6	7	8	11	16	39	62
8	4	7	8	9	12	17	40	63
9	0	5	8	9	10	13	18	41
10	1	6	9	10	11	14	19	42
11	2	7	10	11	12	15	20	43
12	3	8	11	12	13	16	21	44
13	4	9	12	13	14	17	22	45
14	5	10	13	14	15	18	23	46
15	6	11	14	15	16	19	24	47
16	7	12	15	16	17	20	25	48
17	8	13	16	17	18	21	26	49
18	9	14	17	18	19	22	27	50
19	10	15	18	19	20	23	28	51
20	11	16	19	20	21	24	29	52
21	12	17	20	21	22	25	30	53
22	13	18	21	22	23	26	31	54
23	14	19	22	23	24	27	32	55
24	15	20	23	24	25	28	33	56
25	16	21	24	25	26	29	34	57
26	17	22	25	26	27	30	35	58
27	18	23	26	27	28	31	36	59
28	19	24	27	28	29	32	37	60
29	20	25	28	29	30	33	38	61
30	21	26	29	30	31	34	39	62
31	22	27	30	31	32	35	40	63
32	0	23	28	31	32	33	36	41
33	1	24	29	32	33	34	37	42
34	2	25	30	33	34	35	38	43
35	3	26	31	34	35	36	39	44
36	4	27	32	35	36	37	40	45
37	5	28	33	36	37	38	41	46
38	6	29	34	37	38	39	42	47
39	7	30	35	38	39	40	43	48
40	8	31	36	39	40	41	44	49
41	9	32	37	40	41	42	45	50
42	10	33	38	41	42	43	46	51
43	11	34	39	42	43	44	47	52
44	12	35	40	43	44	45	48	53
45	13	36	41	44	45	46	49	54
46	14	37	42	45	46	47	50	55
47	15	38	43	46	47	48	51	56
48	16	39	44	47	48	49	52	57
49	17	40	45	48	49	50	53	58
50	18	41	46	49	50	51	54	59
51	19	42	47	50	51	52	55	60
52	20	43	48	51	52	53	56	61
53	21	44	49	52	53	54	57	62
54	22	45	50	53	54	55	58	63
55	0	23	46	51	54	55	56	59
56	1	24	47	52	55	56	57	60
57	2	25	48	53	56	57	58	61
58	3	26	49	54	57	58	59	62
59	4	27	50	55	58	59	60	63
60	0	5	28	51	56	59	60	61
61	1	6	29	52	57	60	61	62
62	2	7	30	53	58	61	62	63
63	0	12	24	36	48	59	62	63

Table 1. Composite PROM table with traces showing the compression and decompression of the real data values 34, 42, 28, 30 and 31.

for the next data input compression cycle. The partition number is stored in the DATARAM. The following is an example of the compression process. As stated earlier, the state machine always starts at zero at the beginning of each horizontal scan. Therefore, for our example, assume that we are starting at zero, and the following set of image data is applied to the compression algorithm: 34, 42, 29, 31 and 32. Refer to Table 1 during this example analysis. Start at "zero" ("Gray Value" line Ø). The first uncompressed data input is 34; 39 is selected because it is the closest value in line Ø to the original input value of 34. A partition value of 5 is stored and a new "Gray Value" of 39 is determined. Now, at "Gray Value" line 39, the next input value is 42. A partition value of 6 yields a 43, the closest value to 42, which leads to "Gray Value" line 43 for the next input and stores a partition value of 6. Next, an input of 29 results in a partition value of 1 and a new "Gray Value" line of 34. Now, an input of 31 results in a partition of 2 and a "Gray Value" line of 3Ø. Finally, an input value of 32 at "Gray Value" line 3Ø stores a partition value of 4 and yields "Gray Value" line 31.

In summary, the input values of 34, 42, 29, 31, and 32 result in partition values of 5, 6, 1, 2, and 4. When these partition values are decompressed, the data outputs are 39, 43, 34, 3Ø, and 31. Table 2, below, shows the inputs, partitions, outputs and error magnitudes.

Table 2

Partition	Image Input	Image Output	Error
5	34	39	5
6	42	43	1
1	29	34	5
2	31	3Ø	1
4	32	31	1

The error, while usually small and generally insignificant (especially when input data changes are small), is the consequence of reducing the memory storage requirements by 50%.

MASK LOGIC UNIT

Twelve dual-input AND gates constitute the Mask Logic Unit. The circuitry consists of quad AND gates AF3, AF11 and AF19. Each of the data bits from the output of the dual decompressors (12 bits total) is applied to a separate AND gate in the Mask Logic Unit. The other input to each gate is a control bit (12 total) from the Mask and Control Register. If a particular control bit is a "one", the corresponding AND gate passes its data from the decompressor to the Invert selector. Thus, the Mask Logic Unit is simply a 12-section, single-pole-single-throw electronic switch. Currently, this unit is used as a channel selector. The following are four possible states of operation:

- channel one and channel two disabled
- channel one enabled, channel two disabled
- channel one disabled, channel two enabled
- both channels enabled

INVERT SELECTOR UNIT

The Invert Selector Unit consists of quad Exclusive-OR gates AD3, AD11 and AD19 (see sheet 1). This unit receives inputs from the output of the Mask Logic Unit and can either invert or non-invert each data bit.

Like the Mask Logic Unit, the Invert Selector Unit receives 12 control bits from the Mask and Control Register. Each control bit is applied to a separate EX-OR gate along with a data bit. If the control bit is a "one", the gate effectively inverts the data bit; if the control bit is a "zero", the gate passes the data uninverted. The output of the Invert Selector is passed on to AB11 and AB22 (tri-state latches), the Bus Multiplexer. Note: Currently, the control bits are always "zero" (data is uninverted).

MASK AND CONTROL REGISTER

The Mask and Control Register consists of tri-state octal D-latches V33, X33 and Z33 and quad D-latch AB33. Each of the tri-state octal latches is connected to the buffered Multibus data bus (BDØ=BD7), while the quad latch is driven by BDØ-BD3. The outputs from V33 are used as mask control bits for the least significant eight bits of the Mask Logic Unit. V33 is clocked by MAL/ from the Control Logic Unit. MAL/ is an I/O

mapped control signal, addressed by the CPU as port BØH. Thus, when addressing port BØH, the data (mask data) present on the Multibus data bus is latched into V33. In a similar manner, X33 is used to latch the four MSB mask control bits and is addressed as port B1H.

Only two of the four MSB outputs from X33 are used, Q6 (QFM) and Q7 (TSTEN). TSTEN is the control signal used by the Test Data Input Unit; its complement, TSTEN/, enables the Image Data Input Unit. Therefore, when TSTEN is a "one", the Test Data Input Unit passes Multibus data into the Decompression Units and shuts off the Image Data Input Unit. Conversely, when TSTEN is set to "zero", the Decompression Units are fed by the Image Data Input Unit. The signal QFM (Quarter Frame Mode) was used in an earlier version of the workstation. In the present version, QFM is always set to "one", resulting in a continuous logic low at pin 7 of AD33 (see sheet 4, lower right corner).

BUS MULTIPLEXER

The Bus Multiplexer is shown on sheet 1 of the schematics and consists of octal tri-state D-latches AB22 and AB11 and non-inverting tri-state buffers Z22 and Z11. The D-latch outputs are enabled by AMC while the buffer outputs are enabled by AMC/ (refer to the Control Logic Section for information on the generation of AMC/). As stated earlier, AMC/ is active low during memory reads and writes to addresses CØØØH-DFFFH, and during I/O port writes to BØH-B3H. Therefore, during these times, Z22 and Z11 are enabled, allowing the Multibus address bus to address the RAM Enhancement Table.

RAM Enhancement Table

The RAM Enhancement Table is shown on sheet 2 of the schematics. The RAM consists of sixteen 4K by 1-bit static RAM chips organized as a 4K by 16-bit static RAM. Of the 16 output bits, only 15 are used (G13 was used in earlier versions of the workstation). These RAMS feature separate data input and output pins, allowing the input pins to be connected directly to the buffered Multibus data lines (BDØ-BD7). To write data into the table, WE1/ or WE2/ is brought low by performing a memory write to addresses CØØØH-DFFFH.

Because the RAM address bus lines (RAØ-RA11) are driven by buffered Multibus address lines AD1-AD12 respectively, the CPU makes two consecutive memory writes to program one address in the table (ADØ effectively toggles the write enables while AD1-AD12 select the address). The output of the RAM chips forms the RGB bus and is applied to the RGB Bus Controller and the RAM Enhancement Read Buffer.

RAM Enhancement Data Read Buffer

The RAM Enhancement Data Read Buffer is shown on sheet 2 of the schematic and consists of tri-state buffers R2 and N2. These buffers are enabled by RE_1/ and RE_2/ respectively (see Control Logic Section for generation of these signals). When R2 is enabled (odd addresses), the Red bus and the two Green bus MSBs are placed on the Multibus data bus. When N2 (even addresses) is enabled, the three Green bus LSBs and the Blue bus data bits are placed on the Multibus.

RGB Bus Controller

The bus controller consists of V2 and T2, located on sheet 2 of the schematics. These tri-state latches are clocked by PXLCK and enabled by a control signal from the TV Timing and Colorizer board via J2 pin 4. Thus the RGB data generated by the Dual Channel Colorizer can be disabled (during cursor and/or graphics pixel painting) by the TV Timing and Colorizer.

SECTION 4
TV TIMING AND COLORIZER BOARD
TABLE OF CONTENTS

TV TIMING AND COLORIZER BOARD
(SSEC DRAWING 35Ø4-ØØ7, MODIFICATION AD, DATED 2/4/85)

INTRODUCTION

The TV Timing and Colorizer board includes two units, the TV Timing Unit and the Graphics/Cursor Colorizer Unit. Although some timing signals from the TV Timing Unit are used by the Colorizer Unit, the units are distinct.

The TV Timing Unit generates all synchronizing, timing, and control signals required to display the picture on the monitor. In addition, it produces many of the memory management signals required by the DATARAM Control board.

The Graphics/Cursor Colorizer Unit assigns priority ratings to the image, graphics, and cursor data and generates graphics and cursor color signals, pixel by pixel, under control of the microprocessor.

FUNCTIONAL DESCRIPTION

TV TIMING UNIT

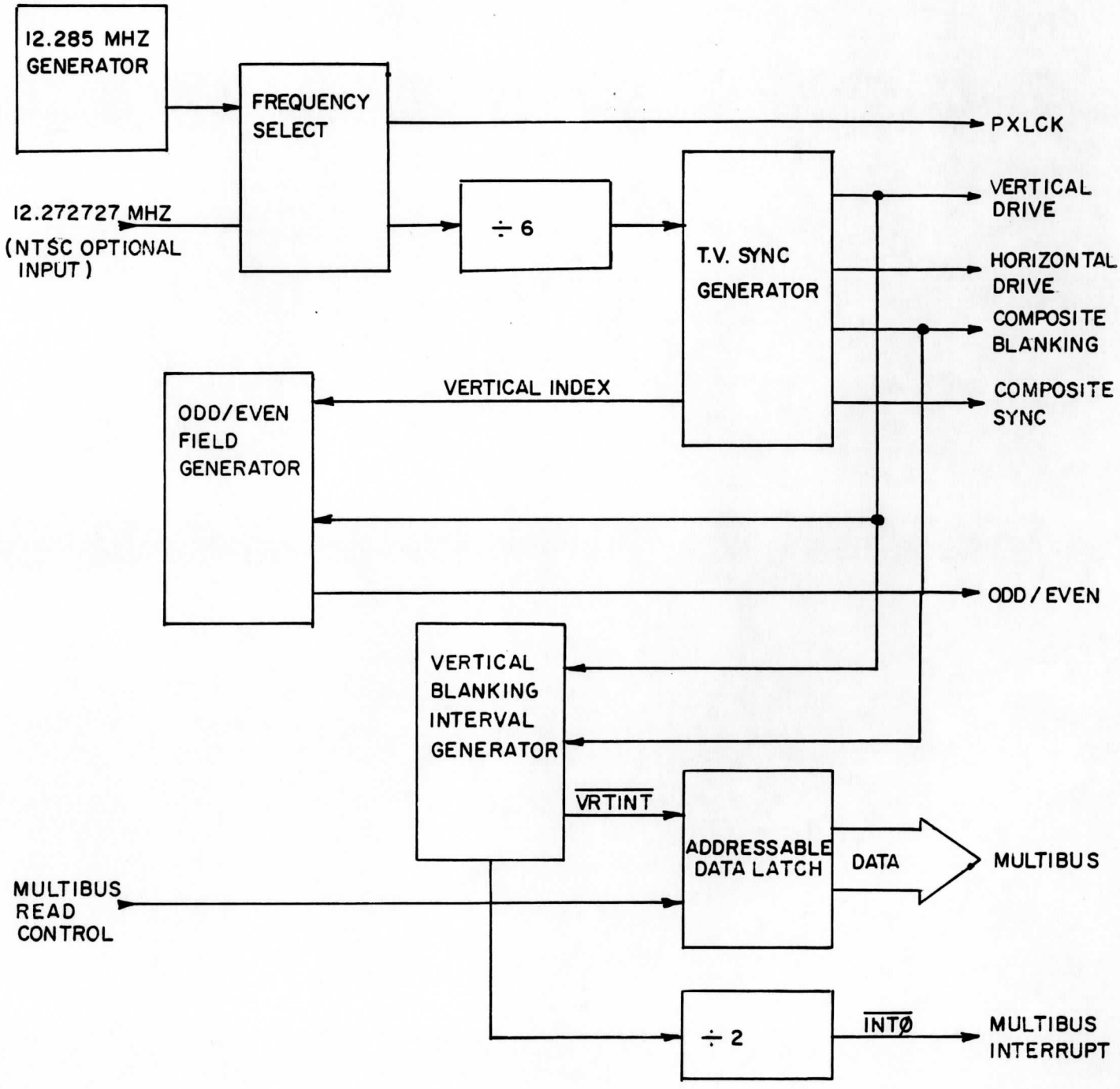
Figure 1 is a functional block diagram of the TV Timing Unit. The unit produces the following six output waveforms:

- PXLCK (picture element clock ≅ 12.3 Mhz)
- VRDRV (vertical drive - 6Ø hz)
- HORDRV (horizontal drive - 15.75 Khz)
- BLNK (composite blanking)
- SYNC (composite synchronization)
- OE (odd/even field identification - 3Ø hz)

PXLCK, VRDRV, HORDRV, and OE are exported, via the P2 bus, to one or more of the following boards:

- DATARAM/Multibus Interface
- DATARAM Control
- Dual Channel Colorizer
- Cursor Generator and Graphics Tablet Interface

BLNK and SYNC are used by only the Graphics/Cursor Colorizer unit.



FUNCTIONAL BLOCK DIAGRAM OF THE T.V. TIMING GENERATOR

FIGURE 1

(3504-007)

All TV timing signals originate with either the on-board 12.285-Mhz generator or the 12.272727-Mhz optional generator from NTSC (National Television Standards Conference). The on-board generator output is applied to the "Frequency Select" block, essentially an electronic switch. The NTSC generator provides a 12.272727-Mhz reference frequency input to the Frequency Select block and provides control signals. The Frequency Select block automatically switches to the NTSC generator reference if it is available.

The output of the Frequency Select block is used as PXLCK and is the source for the divide-by-six block. The divide-by-six block produces the 2.Ø475-Mhz or 2.Ø454545-Mhz (NTSC) reference input to the TV Sync Generator block, a single IC chip that produces all of the standard TV signals.

The vertical drive is interlaced. That is, the TV scans the 262½ odd lines, retraces to the top of the screen and scans the 262½ even lines in each complete picture. Therefore, there are 6Ø vertical sync pulses/sec but only 3Ø complete pictures. The DATARAM Control board must know which field is being scanned (odd or even). As an aid, the TV Sync Generator provides a short duration pulse (vertical index) at the beginning of each picture (3Ø-hz rate). The "Odd/Even Generator" uses the Vertical Index and the Vertical Drive as inputs to generate a 3Ø-hz symmetrical square wave. The waveform is a logic "one" (high) during the odd field and a logic "zero" during the even field.

Because many McIDAS processes are based on frames of information (image and graphics data storage and retrieval, for example), the CPU must know when each field starts and which field is being scanned. The Vertical Blanking Generator block extracts the vertical blanking signal from the composite blanking (BLNK) to produce VRTINT/ (vertical interval). VRTINT/ is available to the Multibus via the "Data Latch" and is a logic "zero" during vertical blanking (retrace). An interrupt, (INTØ/), to inform the CPU that a vertical blanking time has begun, is generated by applying VRTINT to a divide-by-two circuit. The output of the divide-by-two circuit is a symmetrical square wave. The negative-going edge of INTØ/ interrupts the CPU. The CPU uses INTØ/ and VRTINT to define a time window during which the cursor and graphics palettes can be loaded transparently. This window occurs only once during each complete picture, though it may occur at the beginning of either frame (odd or even).

GRAPHICS/CURSOR COLORIZER UNIT

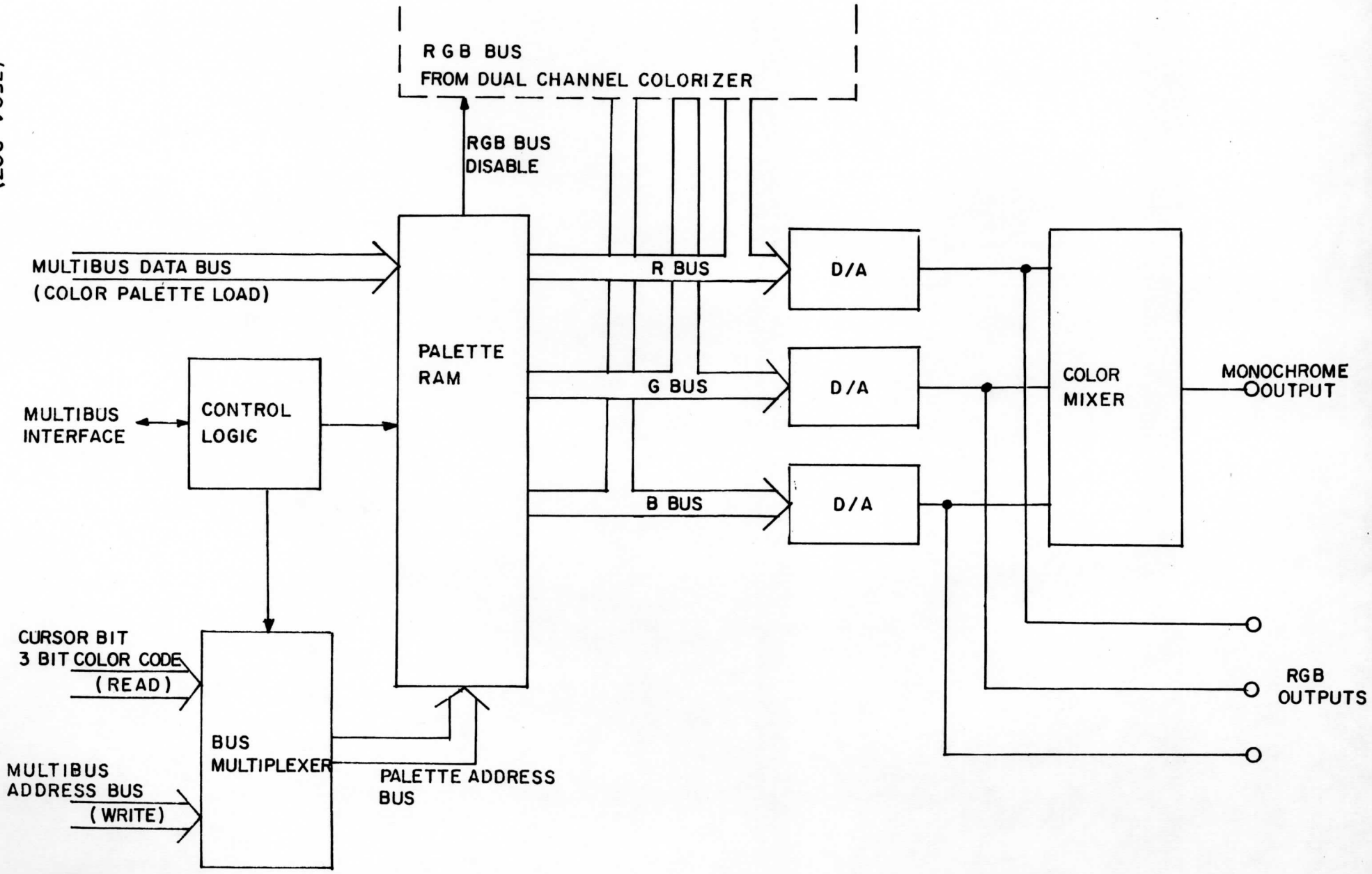
Figure 2 is a functional block diagram of the Graphics/Cursor Colorizer unit. Image data is presented to this unit by the Dual Channel Colorizer board, via the RGB (red, green, blue) bus. The Palette RAM output connects directly to the RGB bus. Only one data source for the RGB bus is permitted at one time, either the Dual Channel Colorizer (image data) or the Palette RAM (graphic/cursor data). Because it is able to disconnect the Dual Channel Colorizer (via the RGB Bus Disable signal) during graphics and/or cursor pixel times, the Palette RAM has a higher priority.

Temporarily disregard the Palette RAM inputs, they are discussed in the next paragraph. The digital image data is converted to analog data by three digital-to-analog converters, one for the each of the three primary colors. The outputs from the converters go to a color mixer and off board, via the P2 bus, to the rear of the chassis. The P2 bus outputs are the RGB monitor video signals. The "Color mixer" block sums 30% of the red drive with 59% of the green drive and 11% of the blue drive to produce a monochrome output for monochrome monitors or hard copiers. These percentages are NTSC standard and represent the brightness amplitude output from a monochrome camera if it scans red, green, and blue objects of equal brightness.

The Palette RAM has 64 possible data storage addresses. The first 32 addresses (0-31) are the graphics color storage area (palette) while addresses 32-63 are reserved for cursor color storage. More precisely, the graphics palette consists of addresses 1-7 while the cursor palette consists of addresses 32-39. Address 0 is selected only during the painting of image pixels (no graphics and no cursor); it connects the RGB bus to the Dual Channel Colorizer board and turns off the Palette RAM output. Graphics Palette addresses 8-31 and cursor palette addresses 38-63 are not used.

The user can preload up to seven graphics colors (addresses 1-7) and up to eight cursor colors (addresses 32-39) into the Palette RAM via the CPU and the Multibus (there are over 32,000 possible color and brightness combinations to choose from).

During the painting process, color data is read from the Palette RAM under command of the Palette address bus. The bus is driven by three



FUNCTIONAL BLOCK DIAGRAM OF THE GRAPHICS/CURSOR COLORIZER

FIGURE 2

color selector bits and the cursor bit (from the Cursor/Joyboard and Graphics Tablet Interface board). Each palette occupies exactly half of the RAM and the desired palette is determined by the state of the most significant RAM address bit. The cursor bit drives this bit and therefore selects the palette. When the cursor bit is "zero", the graphics palette is selected and when the cursor bit is "one", the cursor palette is selected. The color in each palette is selected by the same three color-selector bits.

During the Palette RAM loading process, the palette address bus is connected to the Multibus address bus by the "Bus Multiplexer." The palette data is supplied by the Multibus data bus. The palette "read," "write," and "Bus Multiplexer" controls are directed by the "Control Logic" block.

DETAILED CIRCUIT DESCRIPTION

TV TIMING UNIT

The TV Timing Unit is shown on sheet 1 of 4 of SSEC drawing #3504-007, Modification AD, dated 5/31/84 (TV Timing and Colorizer).

12.285-Mhz Generator

This circuit is J13, a 24.57-Mhz temperature-compensated crystal oscillator. The oscillator output is buffered by inverter J1-A and applied to the clock input of D flip-flop J21-B. J21-B is configured as a divide-by-two circuit by connecting the Q output to the D input. The output frequency of J21-B is 12.285 Mhz and is applied to L5, the Frequency Select circuit.

Frequency Select Circuit

The Frequency Select circuit consists of data selector L5 and line receivers N1-A, -B and -C. Functionally, L5 is a double-pole, double-throw switch. The output of N1-B determines the position of the switch. If N1-B pin 5 is high, pin 3 of L5(1B) is connected to pin 4(1Y) and pin 6(2B) is connected to pin 7(2Y). When pin 5 of N1-B is low, pin 2(1A) of L5 is connected to pin 4(1Y) and pin 5(2A) is connected to pin 7(2Y). Line receivers N1-A and N1-C convert the bipolar NTSC generator inputs (12.272727 Mhz and Sync Reset respectively) into TTL logic levels. The

"section 1" portion of L5 selects the frequency source while the "section 2" portion of L5 selects the Sync Reset source. Note that if the NTSC generator is not connected to J3, all three line receivers have floating inputs. AM26LS33 line receivers are guaranteed by the manufacturer to have a high output when their inputs are floating. Therefore, N1-B, the control line receiver, will have a high output when the NTSC generator is not connected. This connects the on-board 12.285-Mhz frequency source to L5-4 and connects the pin 7 output (RST) to a pull-up. One of the functions, therefore, of the NTSC generator is to force pin 5 of N1-B low, connecting its other two outputs (12.272727 Mhz and Sync Reset) to the outputs of L5. The purpose of the Sync Reset is covered in detail in the TV Sync Generator description. The output of L5 pin 4 becomes PXLCK after it is buffered by J36-B.

Divide-by-Six Circuit

The divide-by-six circuit is 4-bit binary counter L17 and Z11-C. The counter is pre-loaded with a count of 1 by NAND gate Z11-C. Z11-C is qualified by a counter output of Ø11ØB(6), since the Q_B and Q_C counter outputs are used. It takes five counts to qualify the output of Z11-C, but the counter (74LS163) has a synchronous load feature so it does not pre-load until the next clock pulse input. The output frequency of the divide-by-six circuit is 2.Ø475 Mhz or optionally 2.Ø454545 Mhz. The output frequency is applied to the TV Sync Generator and to inverting buffer J36-A.

TV Sync Generator

The TV Sync Generator is TV camera sync generator chip N9. This chip provides all of the basic sync functions for either color or monochrome 525-line/6Ø-Hz interlaced camera and video recorder applications.

The chip divides the reference frequency by 13Ø to produce the horizontal sync frequency of 15,75Ø hz or 15,734.3 hz (NTSC). The vertical sync frequency is generated by dividing the horizontal frequency by 262.5. Therefore, the vertical drive frequency is 6Ø.ØØ hz or 59.94 hz (NTSC). All output signals from this chip are composites of these two frequencies. For further information on this device, refer to a National Semiconductor reference manual. If PXLCK is divided by six to produce the

reference frequency and the reference frequency is divided by 13Ø to produce the horizontal frequency, the PXLCK frequency is 78Ø times the horizontal frequency. Thus, there are 78Ø pixels per horizontal line. However, approximately 132 pixels are lost due to the horizontal blanking time for retrace. This leaves approximately 648 active pixels per horizontal line (in the McIDAS, a few additional pixels are blanked by the CPU and DATARAM).

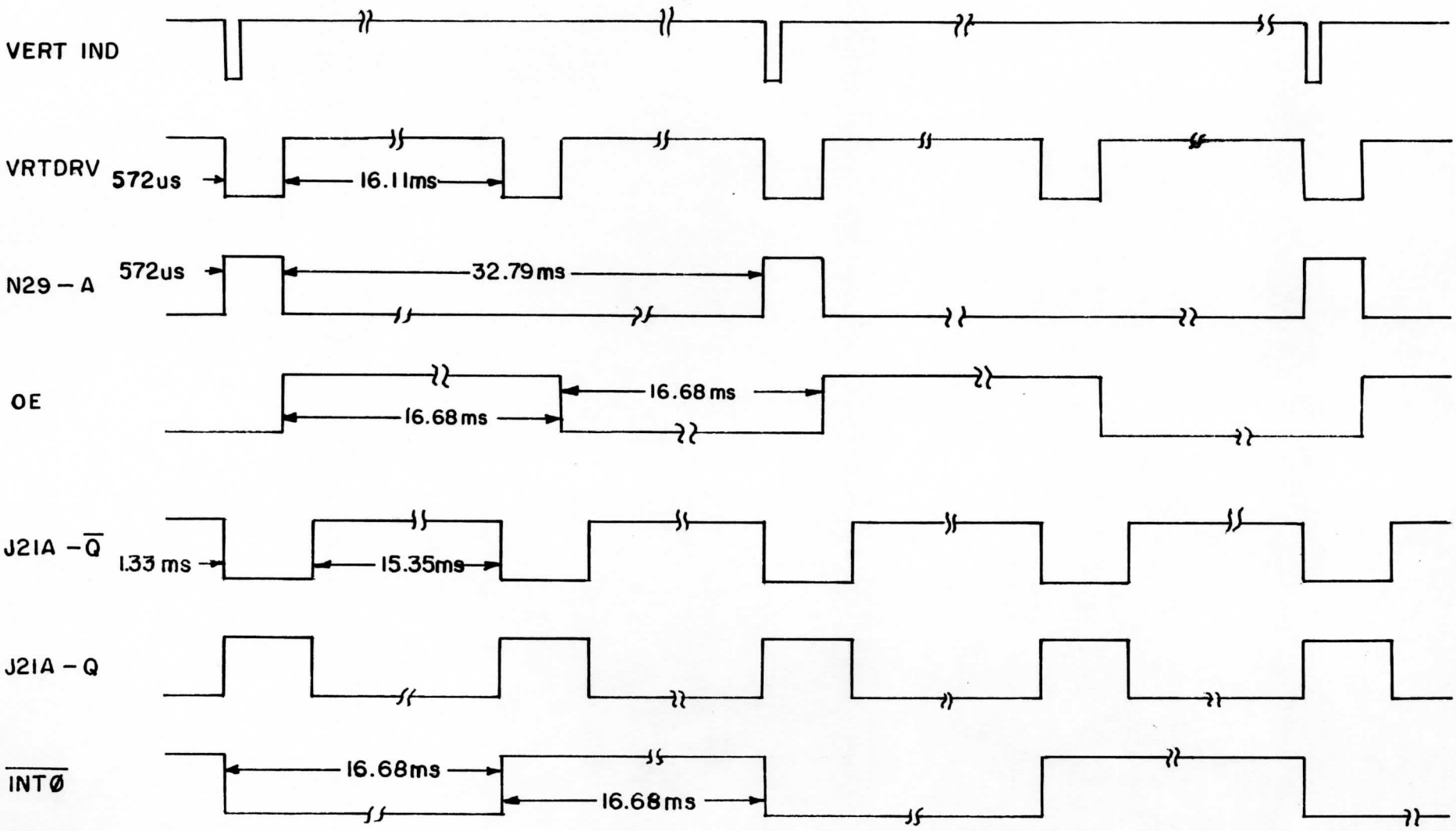
When an NTSC generator is used, it produces its own sync signals for use by an NTSC monitor and the standard RGB monitor (the NTSC generator has a chip very similar to N9). The NTSC generator sync signals and the N9 sync signals must be locked together because the N9 signals are used by the DATARAM control board for reading image and graphics data from memory. If the two sets of sync signals are not locked together, the images appear to drift or float across the screen, because they are produced under control of one set of sync signals and displayed under control of the other.

N9 is designed to be synchronized by an external sync generator. This feature is used when N9 operates with an optional NTSC generator. The generator provides a sync reset input to line receiver N1-C. The reset signal is coupled from pin 5(2A) to pin 7(2Y) of L5, where it becomes the horizontal and vertical reset input to N9.

Horizontal drive (pin 15), vertical drive (pin 11), composite blanking (pin 14), and composite sync (pin 16) outputs from N9 are resynced to PXLCK by quad-D latches N18 and L28. N18 resyncs the outputs to the 2.Ø4-Mhz reference and L28 resyncs the outputs of N18 with PXLCK. VRDRV (L28 pin 2), HORDRV (L28 pin 7), and PXLCK (J36-B pin 4) are exported from this board by line drivers L37-B, -C and -A respectively. In addition, PXLCK, composite blanking, and composite sync are routed to the Graphics and Cursor Colorizer unit (sheets 2, 3 and 4 of the schematic).

Odd/Even Field Generator

The Odd/Even Generator consists of N29-A and -B and inverter/buffer J1-E. The vertical index output pulse from N9 (pin 9) is a 488-nsec active low pulse occurring at a 3Ø-hz rate. The pulse signals the beginning of a new picture. (Remember, a picture consists of two frames, the odd and the even.) The active low pulse is inverted and buffered by J1-E and applied to the clock input of N29-A. Refer to Timing Diagram 1.



TIMING DIAGRAM I

TV TIMING AND COLORIZER BOARD
(3504-007 SHT. 1)

The output of N29-A follows the D input (pin 2) on the rising edge of the inverted vertical index clock input. The D input is always a logic "one" when the clock pulse arrives. After the clock pulse arrives, the output of N29-A is also a logic "one". The N29-A output is also the N29-B input. N29-B is clocked by VRDRV (positive-going edge). As a result, N29-B Q output (pin 9) goes to a logic "one" on the trailing positive-going edge of VRDRV (about 572 µsec after the vertical index). This produces a logic "zero" output from N29-B Q/, which asynchronously clears N29-A. Therefore, N29-A has a 572-µsec active high output pulse every 33.3 µsec. When N29-A returns to a logic "zero" output, it provides a "zero" input to N29-B. Therefore, N29-B also goes to a logic "zero" output at pin 9 but not until the next trailing edge of VRDRV arrives. When N29-B pin 9 goes to a logic "zero", the Q1 (pin 8) returns to a logic "one". This prepares N29-A for the next vertical index input. This produces a symmetrical waveform at the Q output of N29-B; the waveform changes state on the trailing edge of each vertical drive (VRDRV) pulse. This waveform is called OE (odd/ even). OE is always active high during the odd (first) field and active low during the even field. These waveforms are shown in Timing Diagram 1.

Vertical Blanking Interval Generator

The Vertical Blanking Interval Generator provides vertical blanking status to the CPU via the Multibus. To accomplish this, the circuit provides two outputs to the Multibus, an interrupt (INTØ/) and a vertical blanking interval waveform (VRTINT/). INTØ/ interrupts the computer at the beginning of the vertical blanking period, while VRTINT is active low during the vertical blanking period (1.33 msec). The CPU uses these two waveforms to perform transparent operations (processes which disrupt the monitor display if performed during the pixel painting process, such as graphics or cursor color palette RAM loading).

The Vertical Blanking Interval Generator is D flip-flop J21-A. J21-A is preset 6Ø times/sec by the vertical drive signal (VRDRV) and is clocked by composite blanking. VRDRV presets the Q output (pin 5) to a logic "one." The first rising edge of composite blanking following the preset causes the Q output to return to the low state, because the D input (pin 2) is grounded. This results in a 6Ø-hz waveform with an active low period of 1.33 msec (VRTINT/) at pin 6 (Q/) of J21-A.

The Q output of J21-A (pin 5) is applied to a divide-by-two counter, C37. The Q_A output of C37 (pin 14) is a symmetrical 3Ø-hz square wave and is applied to open collector NAND Gate E38-A. The output of E38-A is INTØ/.

VRTINT/ is applied to the D1 (pin 3) input of tri-state octal latch T35. D2 - D7 of T35 are grounded and the eight output lines are connected to the Multibus data bus. Therefore, when the CPU is interrupted by INTØ/, the CPU polls (reads) the status of VRTINT/ by enabling T35. T35 is enabled by driving pin 1 (OE/) low. Due to inverter T25-C, the clock input goes high at the same time pin 1 goes low. This device latches on the rising edge of the clock. NAND gate T25-B drives pin 1 and T25-C, and is qualified when IORC/ is active low (I/O read command) and signal TIMEN is active high. TIMEN is an output of memory mapping PROM X27 (on sheet 2 of the schematic). TIMEN is active high during port address 75. T25-B is qualified, as is T35, during a port read to I/O port 75.

GRAPHICS/CURSOR COLORIZER UNIT

The digital portion of the Graphics/Cursor Colorizer is described first and is found on sheet 2 of 4, SSEC #35Ø4-ØØ7. The digital-to-analog conversion portion (sheet 3) is covered next, followed by the composite video section (sheet 4).

Palette RAM

The Palette RAM consists of two Fairchild F93419 RAM chips (AF14 and AL14). Most of the circuitry on sheet 2 of the schematic is involved with board control and reading or writing data to or from the Palette RAM. As a result, the RAM is analyzed in terms of the following:

- electrical characteristics and configuration
- read/write controls
- addressing inputs
- RGB bus control
- output function

Electrical Characteristics and Configuration

Two RAM chips (AF14 and AL14) are organized as 64 by 9-bit static random-access, open-collector memories. The chips feature separate data

input ($D_{\emptyset}$ - D_8) and data output ($O_{\emptyset}$ - O_8) ports and a common address port ($A_{\emptyset}$ - A_5). Note that $D_{\emptyset}$ of both chips is grounded (not used) and output bit $O_{\emptyset}$ of both chips is not used. The address and data input ports are parallel connected and the data output ports drive separate RGB bus lines, thus the two RAMS function as a 64 by 16-bit RAM.

Read/Write Control

The CS/ (active low Chip Select) is grounded and functions as a read enable. Because pin 15 is grounded, the output is always enabled. Even though the output of the Palette RAM is always enabled, it can give up control of the RGB bus, as explained in the RGB Bus Control section.

The WE/ (active low Write Enable) allows data bus input data to be stored in the address specified by the address port input. Each chip has its own WE/ that originates from a separate output of T13. The generation of these signals is explained in the Control Logic Description.

Addressing Inputs

The address ports ($A_{\emptyset}$ - A_5) are connected in parallel and receive inputs from tri-state buffer AD16 during read operations and from the Multibus address bus, via tri-state bus driver V11, during write operations. In this way, the Palette RAM address bus is multiplexed.

RGB Bus Control

O_2 - O_6 of AF14 are connected to R_4 - $R_{\emptyset}$ of the Red bus respectively, O_7 - O_8 of AF14 and O_1 - O_3 of AL14 are connected to G_4 - $G_{\emptyset}$ of the Green bus respectively, and O_4 - O_8 of AL14 are connected to B_4 - $B_{\emptyset}$ of the Blue bus respectively.

The resistor networks, AJ1 and AK1, are the collector load resistors for the RAM open collector outputs. The two data sources for the RGB bus are the Palette RAM and the Dual Channel Colorizer. The Dual Channel Colorizer board provides graphics and image data to the RGB bus via two 745374 tri-state buffers (V2 and T2 on sheet 2, SSEC #35Ø4 - ØØ5). The Output Enable (OE) of these chips is driven by inverting input OR gate Z11-D (on sheet 2, SSEC #35Ø4 - ØØ7). When the output of Z11-D is a "one", the Dual Channel Colorizer output buffers are in a high impedance condition (outputs disabled). During this time, the Palette RAM is the

source of RGB data. The output of Z11-D is a "one" any time at least one of its two inputs is a "zero". The two inputs to Z11-D are O_1 (AF14) and PALEN/. PALEN/ is a "one" during normal operation and is explained in detail in the Control Logic section. The output of Z11-D is the inverted output of O_1 (AF14) during normal operation. When O_1 (AF14) is a "zero", the Palette RAM is the RGB data source and when O_1 (AF14) is a "one", the Dual Channel Colorizer is the RGB data source.

As stated in the Read/Write Control section, the RAM output is always enabled. The Palette RAM must output all "one"s to give up control of the RGB bus during non-cursor and non-graphic pixels. This action, causing the output transistors in the Palette RAM to turn off, would normally allow all bus lines to go to a logic high. If the Dual Channel Colorizer (DCC) is enabled by Z11-D, the output buffers on the DCC override the logic "one"s (on those RGB lines that the DCC is attempting to pull down to a logic "zero") during the painting of an image pixel. Address ØØH in the Palette RAM is loaded with FFH (all binary "one"s) and is dedicated to image pixel processing.

Output Function

The RGB bus consists of five lines for each of the three colors. The binary value on each set of lines ranges from ØØØØØB (OFF) to 11111B (full brightness). There are 32 distinct levels for each set of five lines (each color).

Address Bus Multiplexer

The Palette RAM Address Bus Multiplexer consists of non-inverting tri-state buffer AD16 and inverting tri-state buffer V11. V11 is enabled for data loading of the Palette RAM by bringing pins IG/ and 2G/ (pins 1 and 19) low. With VII enabled, the Multibus address lines ADR1/ - ADR6/ are inverted and connected to A_0 - A_5 of the Palette RAM, selecting the address that will be loaded with the data present on the input data bus. AD16 is enabled during Palette RAM read operations by bringing pins 1 and 19 on AD16 low. The only four active input lines to AD16 are D2, D5, D6, and D7.

The P2 bus is the source of the active inputs to AD16. The cursor bit signal (CURS) from the Cursor/Joyboard and Graphics Tablet Interface

enters the board from P2-18 and P2-20. Signals VID2, VID1, and VIDØ, from the DATARAM Control board, enter the board on P2-12 and P2-1Ø, P2-8 and P2-6, and P2-4 and P2-2 respectively. All four signals (the three video signals and the cursor signal) are converted to TTL by quad line receiver AB3. VIDØ, VID1, and VID2 form a three-bit binary color selector address with VIDØ functioning as the LSB. The color selector bits and the cursor bit are applied to the inputs of AD16 via AND gates AD6-A, -B, -C, and -D. These AND gates allow the operator the opportunity to inhibit one or more of the four bits. Operation of this feature is explained in more detail in the Control Logic Section. Normally, all bits are gated through.

With AD16 pins D1, D3 and D4 grounded, the following are the possible addresses and their functions:

Binary Address	Function
ØØØØØ	Image Pixel Processing
ØØØØ1	Graphics Color #1
ØØØ1Ø	" " #2
ØØØ11	" " #3
ØØ1ØØ	" " #4
ØØ1Ø1	" " #5
ØØ11Ø	" " #6
ØØ111	" " #7
1ØØØØ	Cursor Color #1
1ØØØ1	" " #2
1ØØ1Ø	" " #3
1ØØ11	" " #4
1Ø1ØØ	" " #5
1Ø1Ø1	" " #6
1Ø11Ø	" " #7
1Ø111	" " #8

Control Logic Section

The Control Logic consists of PROM X27, shift register X19, 3-to-8 line decoder T13, quad D flip-flops X1 and AF1, and associated gates, buffers, inverters, line drivers, and receivers.

PROM X27 provides four mapping outputs (O_1 - O_4) which are either memory mapped or I/O mapped by external gates. IOWC/ (I/O write command)

enters this board from P1-22 and is inverted by buffer J36-F. IOWC is applied to NAND gate Z11-B along with the O_4 output from the PROM. This output is active high for PROM address inputs 72ØØH-727FH (I/O port address 72). Therefore, the output of Z11-B is active low for I/O write commands to port address 72. The output of Z11-B is applied to quad D flip-flop AF1 as a clock. The D input to AF1 (pin 4) is driven by DØ/ (buffered Multibus data bit Ø - DATØ). Therefore, an I/O write to port 72 with a LSB data bit equal to "zero" produces a "one" at AF1-pin 4 (remember, the address bus bits are inverted) and an output from AF1 (pin 3) of "zero". Conversely, a "data write" to port 72, with the data LSB equal to "one", produces a "one" output from AF1 pin 3. When AF1 pin 3 is a "zero", AND gate AD6 is turned off and the cursor is disabled (turned off).

The operation of NAND gate Z11-A, quad D flip-flop X1 and AND gates AD6-A, -B, and -C is nearly identical to the process just described in the preceding paragraph. Note, however, that DØ/, D1/, and D2/ are applied to the D inputs (1D, 2D, and 3D respectively), and the 1Q/, 2Q/, and 3Q/ outputs are applied to NAND gates AD6-A, -B, and -C respectively. The PROM O_3 output is active for addresses 71ØØH-717FH and is I/O mapped by Z11-A. An I/O write to port address 71, with any of the three LSBs equal to "zero", turns off the corresponding color selector bit.

PROM output O_1 is active for address inputs of FFØØH-FF7FH and is applied to AND gate V3-C, along with the output of OR gate R8-A. OR gate R8-A has inputs MRDC (Memory Read Command) and MWTC (Memory Write Command) to pins 2 and 1 respectively. The output of V3-C is active for memory read or write to addresses FFØØH-FF7FH.

The output of V3-C is applied to both data inputs (A and B, pins 1 and 2 respectively) and the CLR input (pin 9) of X19. When the output of V3-C is "zero", the X19 outputs are all "zero" (Q_A, Q_B, Q_C, and Q_D). When the output of V3-C is a "one", a stream of "one"s is clocked by PXLCK, through X19. That is, after the first clock pulse, Q_A is a "one", and Q_B -Q_D are "zero". After the second clock pulse, Q_A and Q_B are "one" and Q_C and Q_D are "zero", and after the third clock pulse, Q_A, Q_B, and Q_C are "one", etc. Note that the Q_A output and the inverted Q_D (inverted by inverter V22-D) output are applied to AND gate V3-D. V3-D, therefore, is qualified from the rising edge of the first PXLCK until the rising edge of the fourth PXLCK, after a memory read or write to addresses FFØØH-FF7FH.

When V3-D is qualified, AND gate T5-B is qualified, producing GRFEN/ which enables tri-state buffer V11 and disables tri-state buffer AD16. In this way, the Palette RAM is addressed by the Multibus address bus.

Three-to-8 line decoder T13 is qualified when G2 (pin 6) is "one", and G2A and G2B are "zero". The Q_B output of X19 is applied directly to G2 of T13, qualifying this input on the second PXLCK clock rising edge, following a memory read or write to address FFØØ-FF7FH. If the request is a "memory write," the output of inverter V22-A is a "one", not a qualifying input to V3-A. However, the Q_C output of X19 does qualify V3-A, until its output goes to a logic "one" on the rising edge of the third clock pulse after X19 is enabled. Therefore, during a "memory write," T13 is enabled from the rising edge of the second PXLCK to the rising edge of the third PXLCK, following the qualification of X19. During a "memory write," the C input (pin 3) of T13 is "zero" due to the inversion of the inactive high MRDC/ by inverter J36-D. The B input of T13 is "one" due to the inversion of the active low MWTC/ by inverter V22A. The A input of T13 is ADRØ and can be either "one" or "zero". When ADRØ is "zero", Y_2 of T13 is active low, enabling RAM AL14. When ADRØ is "one", Y_3 of T13 is active low, enabling RAM AF14. The table below summarizes the memory write operation to addresses FFØØH-FF7FH.

ADDRESS	RAM	REMARKS
FFØØH	AL14	Image pixel processing. Inverted data must be all "one"s.
FFØ1H	AF14	Image pixel processing. Inverted data must be all "one"s.
FFØ2H	AL14	G2-GØ and B_4-$B_Ø$ RGB data load. Graphics Color #1
FFØ3H	AF14	R_4-$R_Ø$ and G_4-G_3 RGB data load. DATØ is equal to "zero". Graphics Color #1
FFØ4H	AL14	Same as address FFØ2H but Graphics Color #2
FFØ5H	AF14	Same as address FFØ3H but Graphics Color #2
FFØ6H-FFØEH (even)	AL14	Same as address FFØ2H but Graphics Colors 3-7
FFØ7H-FFØFH (odd)	AF14	Same as address FFØ3H but Graphics Colors 3-7
FF1ØH-FF3FH		Not used.

FF4ØH	AL14	G_2-$G_Ø$ and B_4-B_3 RGB Data Load. Cursor Color #1
FF41H	AF14	R_4-$R_Ø$ and G_4-G_3 RGB Data Load. DATØ is equal to "zero". Cursor Color #1
FF42H-FF4EH (even)	AL14	Same as FF4OH, but Cursor Colors 2-8
FF43H-FF4FH (odd)	AF14	Same as FF41H, but Cursor Colors 2-8
FF5ØH-FF7FH		Not used

During a memory read to addresses FFØØH-FF7FH, GRFEN/ is produced just as it was during a memory write, enabling V11 and disabling AD16. Now, however, the G2-A and -B inputs are already qualified, because MWTC/ is a "one". T13 is enabled as soon as G2 goes high, on the second rising PXLCK following the enabling of X19. During a memory read, the C input is a "one" and the B input is a "zero". During a memory read, the outputs from T13 are Y_4 (ADRØ equal to zero) and Y_5 (ADRØ equal to "one"). Y_4 and Y_5 enable tri-state buffers AN2 and AL2 respectively, allowing the user to examine the contents of the Palette RAM. PALEN/ is formed by ORing Y_4 (GRFRD1/) and Y_5 (GRFRD2/) via gate V3-B. PALEN/ enables tri-state buffer V11 and disables tri-state buffer AD16, via gate T5-B. In summary, a memory read allows the Multibus address bus to address the Palette RAM and enables AL2 or AN2, allowing the specified Palette RAM contents onto the Multibus data bus for review by the user.

Gate T5-A combines the four signals (memory or I/O mapped) to enable tri-state buffer X10-A. Thus, XACK/ (Transfer Acknowledge) goes active low, informing the CPU that the off-board memory or I/O process has been completed.

Digital-To-Analog Converter Section

The output of the RGB bus is applied to the three D latches AB2Ø, AJ18, and AP18 (located on sheet 3 of the schematic). The latches resynchronize the RGB data to PXLCK and integrate the blanking function, by applying composite blanking to the clear (CLR) inputs (pins 1). In this way, they drive all color levels asynchronously to "zero" during horizontal and vertical retrace.

The five-bit output from each latch is applied to the most significant five-bit input of an eight-bit DAC (Digital-to-Analog Converter). The DACs (AA3Ø, AF3Ø, and AL3Ø) three LSBs are grounded. The DAC output section is functionally a +5.Ø-ma (Full scale) current source in parallel with a 400-ohm resistor. The 4ØØ-ohm shunt resistance is in parallel with a 1% precision 115Ø-ohm load resistor and the 4ØØK-ohm input impedance of the next circuit. Thus, the effective DAC shunt resistance is 297 ohm. The maximum current output (all five bits high) is 4.99 ma, because the lower three inputs are always "zero". Therefore, the maximum DAC output, and thus the maximum color amplitude, is +1.42 volts.

The analog output of each DAC is applied to a National LHØØØ2 current amplifier (AD39, AJ39, and AP39), for a nominal gain of Ø.96. Primarily, the current amplifiers convert the high impedance output of the DACs to an output impedance of approximately 6 ohm. The amplifier output voltage is in phase with the input and approximately 1.41V, peak to peak. The amplifier output voltages are output to the P2 bus, via 68-ohm series resistors, as the RGB monitor drive signals. The color drive input impedance of standard RGB monitors is 75 ohm, so the monitor input voltages are approximately Ø.7ØØ peak. This is an industry standard. Note that the composite sync is also supplied to the P2 bus, using an LHØØØ2 amplifier and 68-ohm series resistor.

Color Mixer Section

The RGB current amplifier output voltages are also applied to the composite video circuitry (on sheet 4 of the schematic). Operational amplifier E15 functions as a summing amplifier. The red, green and blue drive voltages are applied to 3.ØK-ohm, 1.5K-ohm, and 8.2K-ohm input resistors respectively. If +1.ØØV is simultaneously applied to the three input resistors, the red, green and blue input currents are 333 µa, 667 µa and 122 µa respectively. Because the amplifier input current is negligible, the total input current flowing through the 91Ø-ohm feedback resistor is 1.122 µa. Therefore, the output voltage is -1.Ø2V. In other words, the amplifier adds 59% of the green drive to 3Ø% of the red drive and 11% of the blue drive. The basis of these percentages was addressed in the Graphics/Cursor Colorizer Functional Description.

The output of F16 is a negative voltage, ranging from Ø.Ø volts (all RGB binary bits equal to "zero") to -1.4 volts (all RGB binary bits equal

"one"). This voltage is applied to another summing amplifier, E3Ø. E3Ø sums the RGB video (including composite blanking) with composite sync. The composite sync from the TV Timing unit is applied to inverting buffer J1-D, resulting in a positive 4.Ø-volt pulse input to the summing amplifier E3Ø. The summing amplifier inverts the RGB video (Ø to 1.4V) and inverts and multiplies the sync pulse by 4.7/3Ø to produce a sync pulse with an amplitude of -Ø.63V. Thus the output of E3Ø is a composite video having a peak-to-peak amplitude of 2.ØV. Current amplifier G39 reduces the output impedance to 74 ohm (6-ohm amplifier output impedance and the 68-ohm resistor). Therefore, to drive a 75-ohm monochrome monitor or hard copier, the input voltages to these devices are the industry standard 1.ØV peak to peak.

4/DB1/04

SECTION 5
CURSOR/JOYBOARD AND GRAPHICS TABLET INTERFACE
TABLE OF CONTENTS

CURSOR/JOYBOARD AND GRAPHICS TABLET INTERFACE
(SSEC DRAWING #35Ø4-Ø29, MOD I, DATED 4/26/85)

INTRODUCTION

The Cursor/Joyboard and Graphics Tablet Interface is a combination of three independent units: the Cursor Generator, the Joystick Support Interface, and the Graphics Tablet Interface. Except for sharing minimal address decoding and an internal data bus, the three units, though they reside on the same board, are physically, functionally, and logically distinct.

The Cursor Generator is a timing circuit that tells the TV Timing/Colorizer board whether or not the pixel about to be scanned is a cursor bit. The TV Timing/Colorizer board assigns brightness levels and color to cursor pixels. The Cursor Generator receives eight bytes of cursor parameter data from the microprocessor, via the Multibus, to determine cursor size, shape, and position, and therefore which pixels are cursor pixels. TV timing signals from the TV Timing/Colorizer board are used by the Cursor Generator for synchronization.

The Joystick Support Interface receives, decodes, and stores the serial RS-232 joystick position data output from the Kraft Digital (or Miniature) Joystick board. This position data is made available to the Multibus via addressable buffers and is used to determine the position of the cursor. Typically, the right joystick provides coarse position control while the left functions as a vernier (fine) control.

The Graphics Tablet Interface receives, decodes, and stores the serial RS-232 coordinate position data that is output by the Graphics Tablet. The coordinate data is available to the Multibus via addressable buffers. The coordinate points can be divided into "areas" by the host computer and defined by the user to represent CRT keystrokes or strings of keystrokes. When used in this way, with an appropriate graphics tablet overlay, frequently-used, complicated functions can be executed by touching the appropriate area with the pen.

FUNCTIONAL DESCRIPTION

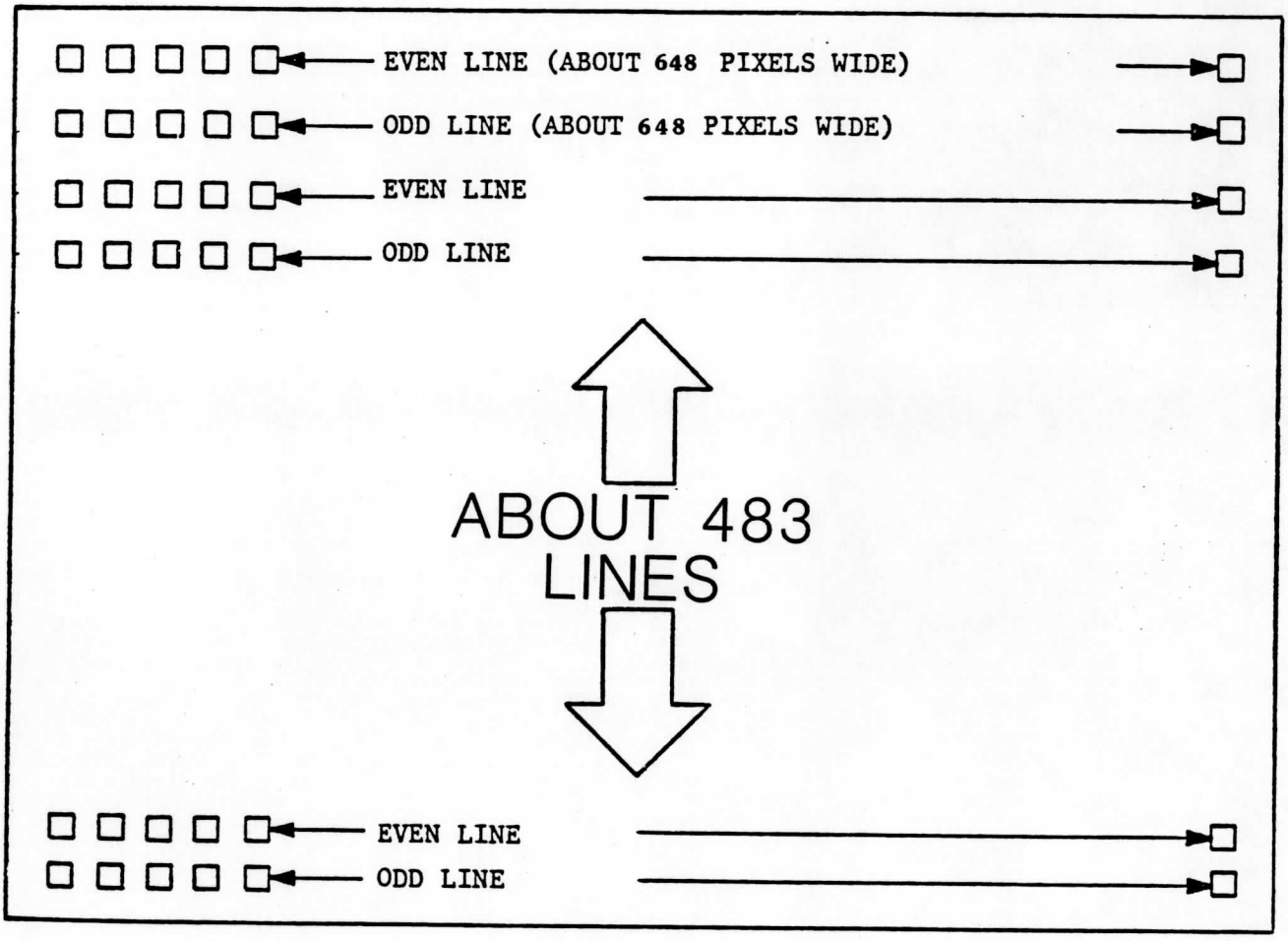
Each of the three units are described separately.

CURSOR GENERATOR FUNCTIONAL DESCRIPTION

The TV picture is composed of 525 horizontal lines, classified alternately as odd lines and even lines. Each horizontal line is subdivided into 78Ø picture elements (pixels). Forty-two of the horizontal lines are blanked during vertical retrace; 132 pixels are blanked during each horizontal retrace. Therefore, each picture is approximately 648 pixels by 483 pixels (see Figure 1). Each line is painted from left to right, one pixel at a time. First, all the even lines are painted and then, all the odd lines are painted, completing one picture. If the host computer requires that the cursor be displayed on pixel 3ØØ of line 251, then the cursor generator's output goes "on" when the TV sweep paints pixel 3ØØ of line 251 and the generator's output is "off" at all other times. That is, the output is off during the painting of all even lines and the output is off when the TV sweep paints the first line, the third line, and all other odd lines until it reaches line 251. The generator's output remains off for all the pixels in line 251 until the sweep reaches pixel 3ØØ. While the sweep paints pixel 3ØØ, the generator's output is on and the cursor is painted or displayed. For the rest of the pixels in line 251 and for the rest of the odd lines, the cursor generator's output is off. This cycle continues until the host computer changes the format of the cursor display. The cursor can be an outlined square, a solid square, a crosshair, or several other rectangular formats. The cursor generator must time its output ("cursor bit") to be on when the individual pixels that creak the location and design of the cursor are painted.

Any pixel on the color monitor is referenced by its XY coordinate pair. The vertical coordinate (Y) is a specified number of scan lines from the top of the screen, while the horizontal component consists of a specified number of pixels from the left of the screen. Therefore, the following three timing signals are required to drive the cursor generator:

- vertical timing pulses to locate the top of the screen
- horizontal timing pulses for vertical position (Y)
- pixel clock pulses for horizontal position (X)



TV PICTURE AS SEEN BY VIEWER

Each line is painted from left to right, one pixel at a time. First all the even lines are painted, and then all the odd lines, and then all the even lines, etc.

Figure 1. Composition of a Digital TV Picture
(3504-029)

Refer to Figure 2, the functional block diagram of the cursor generator. The eight-byte storage register receives eight bytes of cursor parameter data from the Multibus. The eight bytes are defined as follows:

- byte zero - least significant 8 bits of cursor width (pixels)
- byte one - least significant 8 bits of cursor center pixel
- byte two - lower nibble is most significant 4 bits of cursor center pixel
  - upper nibble is most significant 4 bits of cursor center line
- byte three - least significant 8 bits of cursor height (lines)
- byte four - least significant 8 bits of cursor center line
- byte five - lower nibble is most significant 4 bits of cursor width (pixels)
  - upper nibble is most significant 4 bits of cursor height (lines)
- byte six - cursor state assignments
- byte seven - cursor state assignments

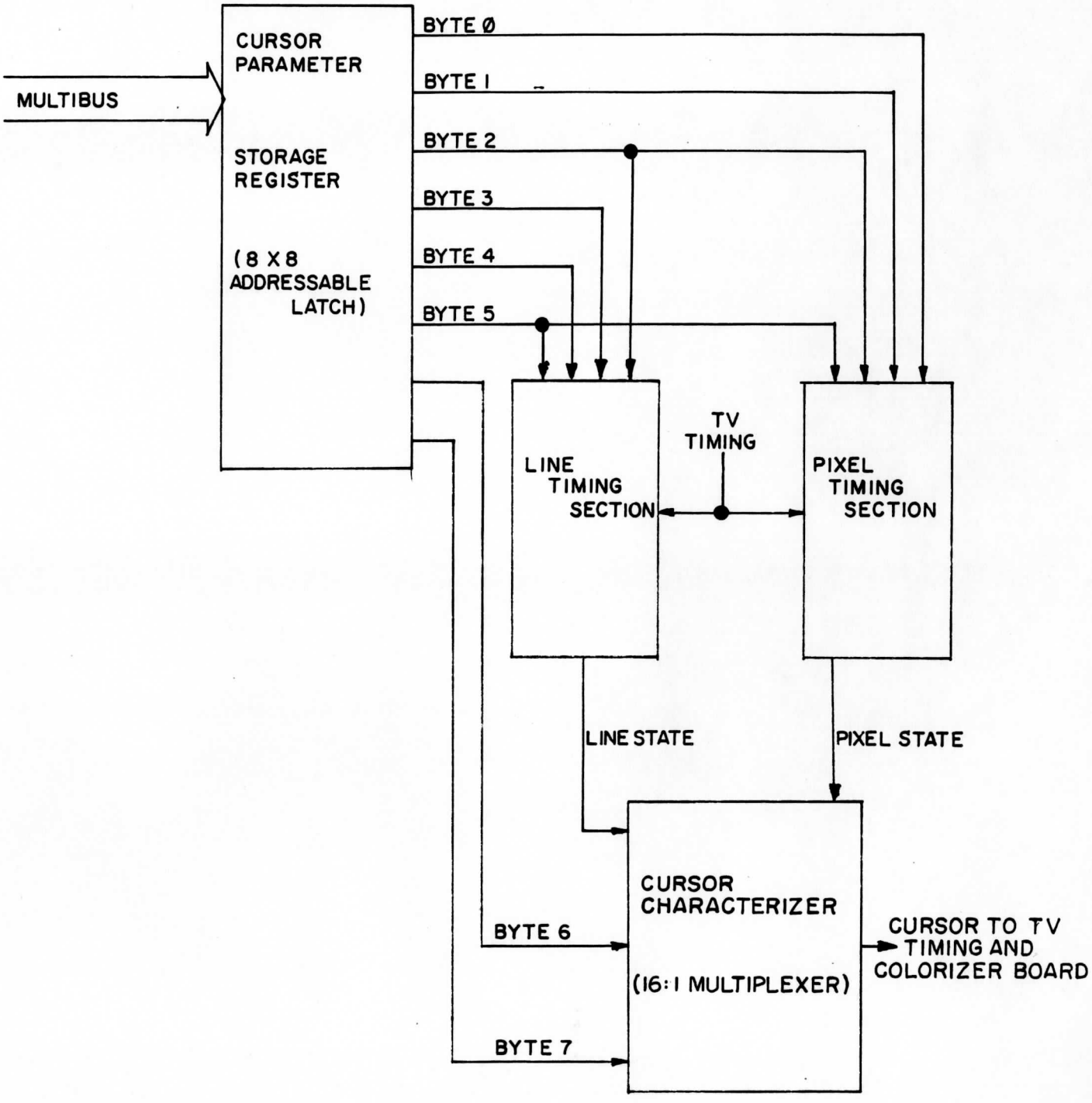
The eight-byte storage register is an addressable latch which continuously supplies parameter data to the other functional blocks, until it is changed by the microprocessor, under user control.

The generator is made up of two nearly identical blocks, the line and pixel timing blocks. The blocks compare desired cursor position and size data with present scan position and generate the following four output codes, called "states":

- non-cursor area (state Ø)
- cursor edge (state 1)
- cursor interior (state 2)
- cursor center (state 3)

Sixteen state combinations exist because there are four states in both the horizontal and vertical axis.

The four states in each logic block are combined to form two 2-bit words. The two words are applied as addresses to the Cursor Characterizer. The user assigns a "one" or "zero" to each of the 16 state inputs, via cursor parameter bytes 6 and 7. The characterizer gates one of these inputs, as determined by the two address words from the Cursor Line Timing



CURSOR GENERATOR FUNCTIONAL BLOCK DIAGRAM
(3504-029)

FIGURE 2

and Cursor Pixel Timing blocks to the output. The output of the Cursor Characterizer block is applied to the TV Timing/Colorizer board. The output for each pixel scanned is a single bit. If the cursor bit is on, the pixel is a cursor pixel, otherwise, it is either a graphics or image pixel.

JOYSTICK SUPPORT INTERFACE FUNCTIONAL DESCRIPTION

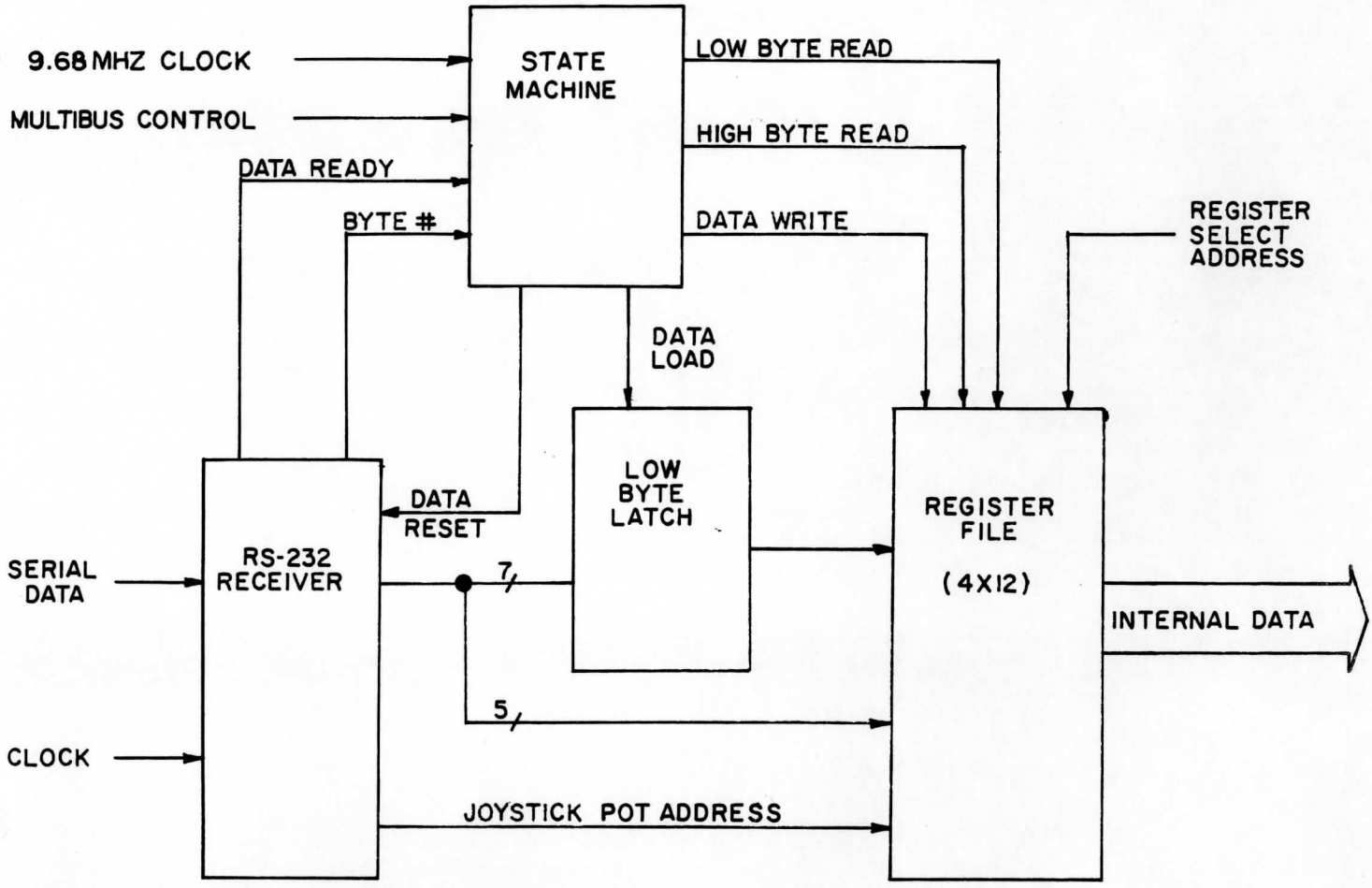
The Kraft Digital (or Miniature) Joystick board digitizes the four analog joystick potentiometer outputs and asynchronously transmits the data serially to the Joystick Support Interface unit. Eight bytes of data are transmitted to this unit, that is, two bytes for each of the four potentiometers (pots).

The Kraft Digital (or Miniature) Joystick board outputs 8ØØ characters per second to the Joystick Support Interface unit (4ØØ pairs). There are four pots, so each pot position is updated 1ØØ times per second. Essentially, this unit must do the following:

- organize the characters into pairs
- store the 12 data bits from each pair in a Register File
- output microprocessor-requested pot position data (via the Multibus)

Figure 3 is a functional block diagram of the Joystick Support Interface. All control logic for this unit is contained in the State Machine. Outputs from the State Machine control the RS-232 Receiver, Low Byte Latch, and Register File read and write operations. The RS-232 Receiver block converts the 96ØØ-baud serial data to parallel format. When the receiver detects the end of a character, a data ready (DR) command is sent to the State Machine. The receiver also sends the first data bit (this is the character ID, refer to the Kraft Digital (or Miniature) Joystick section) to the State Machine. If the ID bit is a "zero" (1st character), the State Machine enables the Low Byte Latch which temporarily stores the low seven data bits. If the ID bit is a "one" (2nd character), the State Machine enables the Register File Data Write line.

The Register File consists of four 12-bit buffers. Prior to writing data to the Register File, one of the four buffers must be selected. The joystick pot address data contained in the 2nd character is used as the Data File address. Therefore, each two-character pair contains its own



JOYSTICK SUPPORT INTERFACE FUNCTIONAL BLOCK DIAGRAM

(3504-029)

FIGURE 3

storage address. Each buffer in the Register File is updated (overwritten) 1ØØ times per second, making position information continuously available. The Register File allows data to be written to and read from simultaneously, from the same or different locations. Pot position data is output to the Multibus when requested by the microprocessor, via the Internal Data bus. Two data reads are required to transmit the 12 position bits. The Multibus read requests are processed by the State Machine.

GRAPHICS TABLET INTERFACE FUNCTIONAL DESCRIPTION

The Graphics Tablet Interface is functionally nearly identical to the Joystick Support Interface.

When the user contacts the pad surface of the Bit Pad One graphics tablet (by Summagraphics Corporation) with the pen, the pad outputs a group of five characters at a serial asynchronous baud rate of 19,2ØØ bits/sec. Each second, 135 groups are output. The first character of a group is a flag character, and is followed by two characters of X coordinate data and two characters of Y coordinate data. The serial data format is seven data bits, even parity, and two stop bits. The following table summarizes the format of each group.

Character	Content	Bit	7	6	5	4	3	2	1	Ø
1	FLAG		P	1	D	D	D	F	Ø	Ø
2	LSB X Coord		P	Ø	X_5	X_4	X_3	X_2	X_1	$X_Ø$
3	MSB X Coord		P	Ø	X_{11}	$X_{1Ø}$	X_9	X_8	X_7	X_6
4	LSB Y Coord		P	Ø	Y_5	Y_4	Y_3	Y_2	Y_1	$Y_Ø$
5	MSB Y Coord		P	Ø	Y_{11}	$Y_{1Ø}$	Y_9	Y_8	Y_7	Y_6

D = Don't Care

P = Parity

F = Flag

Note that only the flag character is allowed to have a "one" in bit position 6. The status of this bit separates flag character (1st character) processing from data processing (characters 2-5).

Two major processes are performed by the Graphics Tablet Interface unit. First, it receives the serial data, converts it to parallel and writes it into a Register File. Second, it outputs data, upon request, from a register file onto the Multibus.

Figure 4 is a functional block diagram of the Graphics Tablet Interface. The State Machine controls sequencing of this unit. The RS-232 Receiver block outputs a DR pulse (data received) and bit six (Data/Status) to the State Machine upon completion of a character. The State Machine uses these two inputs to determine if the character is status or data. If the character is a status character, the State Machine does the following:

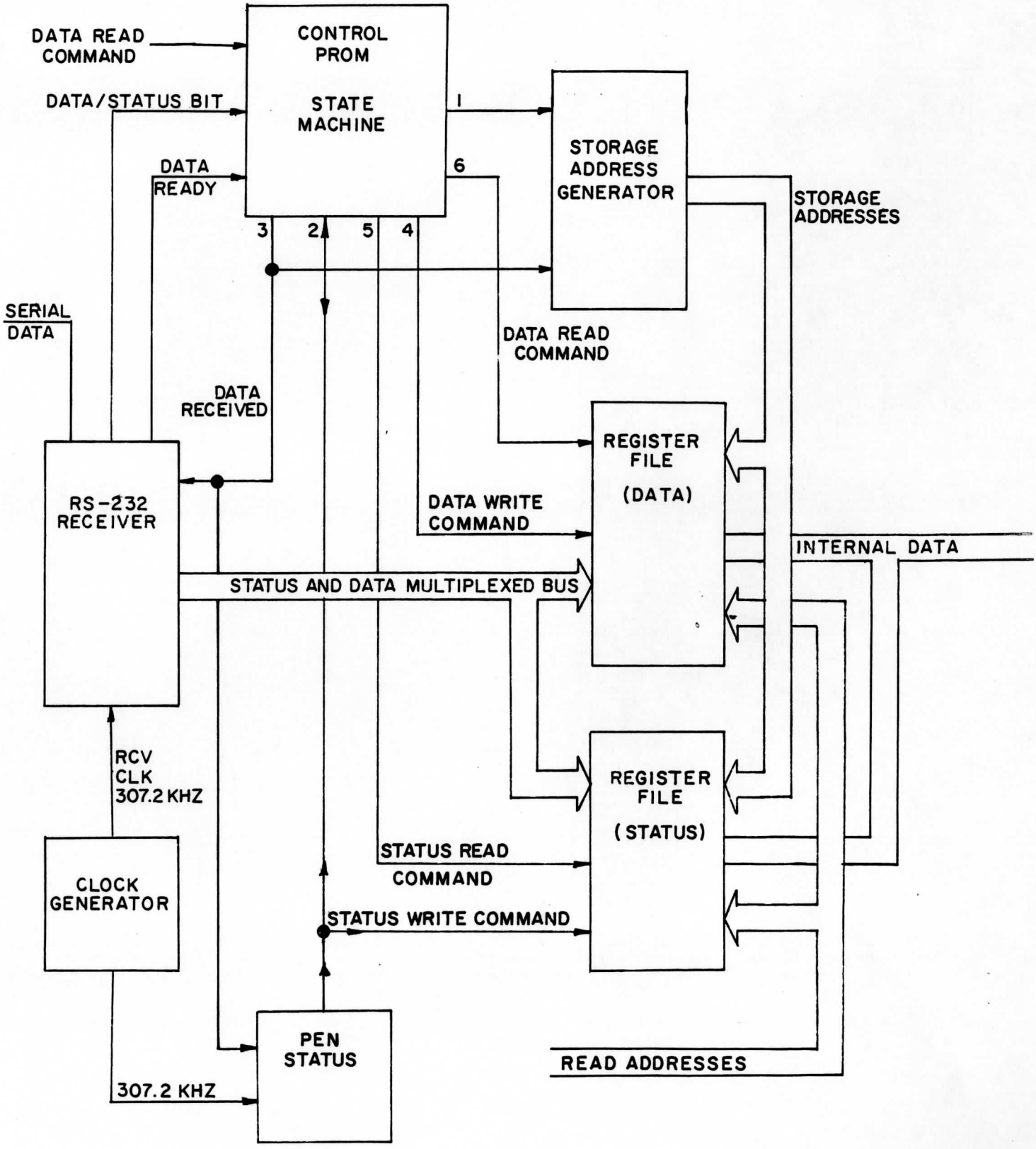
- Initializes the Storage Address Generator
- Writes the status into the Status Register File (Address zero)
- Outputs a "Data Received" command to the RS-232 receiver

If the character is a data character, the State Machine does the following:

- Decrements the Storage Address Generator
- Writes the data into the Data Register File at the address specified by the Address Generator (Address 3, 2, 1 or Ø)
- Outputs a "Data Received" command to the RS-232 receiver

The Pen Status and Clock Generator blocks have not been addressed yet. The Pen Status block is a timer that resets each time the State Machine generates a "Data Received" pulse. This occurs as long as the pen contacts the pad ("pen down"), but if the pen is up, no data is received, the counter is not reset and the Pen Status block generates a "Status Write Command" to the Status Register File. This cancels the "one" stored in bit position 6. In this way, the microprocessor can periodically and rapidly determine if the pad is being used by reading the status Register File and testing bit 6.

The Clock Generator is a crystal-controlled oscillator that produces the data read clock for the RS-232 Receiver. The clock frequency is 3Ø7.2 Khz (16 times the data rate). The block also supplies the Pen Status block with a time reference.



GRAPHICS TABLET INTERFACE FUNCTIONAL BLOCK DIAGRAM
FIGURE 4
(3504-029)

The Graphics Tablet Interface unit's data read sequence is very similar to that of the Joystick Support Interface unit. The State Machine generates two read commands based on its inputs, a Status Read Command and a Data Read Command. The two read commands, together with the Multibus address bus, can select any of the five buffers for output to the Multibus data bus, via the internal data bus.

DETAILED CIRCUIT DESCRIPTION

The schematic diagrams of the Cursor Generator and Graphics Tablet Interface are shown on SSEC drawing #35Ø4-Ø29 (Modification H dated 5/3/84) sheets 1-5. The schematic circuit analysis is accomplished by analyzing groups of components represented by single blocks on the respective functional block diagrams. The circuitry common to one or more units on this board is described before the individual units.

The SSEC circuit schematics are labelled by the column and row in which pin #1 of that chip resides. This is very helpful for troubleshooting, since the symbol ID is also the chip location; however, IC gates, flip-flops, buffers, and inverters usually have several identical logic circuits packaged on the same IC. Therefore, when reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and a section identification letter. The symbol ID number alone is used to refer to single function ICs.

SHARED CIRCUITS DESCRIPTION

The following circuits are shared by one or more units:

- Multibus interface circuits
- Internal bidirectional data bus
- IO (Input/Output) mapping logic

The Multibus interface circuits consist primarily of line drivers and line receivers; however, an important exception is the Multibus signal XACK (Transfer Acknowledge). From the perspective of the microprocessor, all units on this board function as I/O devices. The 8Ø/24 microprocessor board requires an external response (XACK) to any off-board I/O write or read requests. The microprocessor enters a wait state and ceases all other processing until XACK goes true (or microprocessor board time out

occurs), informing the CPU that the request has been carried out by the off-board hardware. There are three separate I/O units on this board; each must provide an acknowledge input to the XACK generator.

The Joystick Support Interface Unit and the Graphic Tablet Interface unit are both I/O read-only devices and generate the acknowledge signals JACK and PACK respectively. These signals are ORed together by OR gate AB3-A (on page 1 of the schematic). The output of AB3-A is ANDed with IORC by gate A32-D to form READ. READ, therefore, goes active high if either the Joystick or Graphics Tablet unit acknowledge a CPU I/O read request. READ is used to control the Internal data bus, as explained later, and is combined with WRITE by OR gate AB3-B. WRITE is an acknowledge signal generated by the Cursor Generator unit. The output of AB3-B is inverted by E12-F and applied to the enable input of tri-state line driver T32-F. When enabled, the line driver's output (XACK) is pulled low, providing the required acknowledge to the 8Ø/24 board.

The internal bidirectional data bus is connected to the Multibus data lines (DATØ-DAT7) by two bidirectional four-bit bus drivers (V32 and X32 on page 1). The enable pins (1 and 13) of both drivers are driven by READ (true during I/O read operations to the graphic tablet or joystick units), allowing data onto the Multibus only during READ time. At all other times, the bus drivers allow incoming data to go from the Multibus to the internal bus. The internal data bus goes to all three units on the board.

The I/O mapping logic is G32, a 512 by 4-bit PROM. The #54A program in the PROM allows a high on pin 11 ("Y") if the address on the inverted address lines is 78H-7FH. This eight-address block addresses the Cursor Generator unit during "write" operations and addresses the Joystick Support Interface unit during "read" operations. The other PROM output is from pin 1Ø (RPEN). RPEN is active high if the address on the inverted address lines is 7ØH-74H and is used during I/O read operations to the Graphics Tablet unit.

CURSOR GENERATOR CIRCUIT DESCRIPTION

The Cursor Generator is located on sheets 1-3 on the SSEC #35Ø4-Ø29 drawing. The Cursor Parameter Storage Register, as previously shown in Figure 2, consists of eight 8-bit addressable latches (N3, N12, N23, N32,

R3, R12, R23, and R32). Each latch stores one bit in one of eight output latches, determined by the three input address lines: A, B, and C (pins 1, 2, and 3 respectively).

The data inputs to the eight latch ICs are the eight data lines of the Internal bus. The Internal data bus is connected to the Multibus data lines at all times except during an I/O read to the joystick or graphics units. The latch address lines (A, B and C) are all connected in parallel, as are the enable inputs (pin 14). If a latch is enabled on one chip, the corresponding latches on all eight chips are enabled. Because all address lines are parallel-connected, all chips load data into the same corresponding latch. As an example, assume that the data on DATØ/-DAT7/ are Ø11Ø11ØØ respectively and BAØ-BA2 are Ø11 (binary representation of 3). After the latches are enabled (pin 14 goes low), the Q3 output of the eight latches is ØØ11Ø11Ø (left to right). The outputs from these devices do not change unless the CPU writes over the data. During turn-on or reset, INIT goes active low, setting all outputs to zero.

Addressing the latches is accomplished by applying the lower three address lines (BAØ, BA1, and BA2) to the A, B, and C inputs respectively and driving the enable pins low (pin 14). Gate A32-A ANDs the "Y" output from the PROM (active high for addresses 78H-7FH) with IOWC to produce WRITE. WRITE is inverted by E12-D to produce the addressable latch-enable signal.

The outputs from the addressable latches are wired such that the eight $Q_Ø$ outputs of all eight latches form "byte Ø," Q1 outputs form "byte 1," . . . and Q7 outputs form "byte 7." These outputs remain static until changed by the CPU or initialized to zero during turn-on or reset.

Line Counter Section

The schematic diagram for the Line Counter Section of the Cursor Generation Functional Block Diagram (Figure 2), is shown on SSEC drawing #35Ø4-Ø29, sheet 2 of 5.

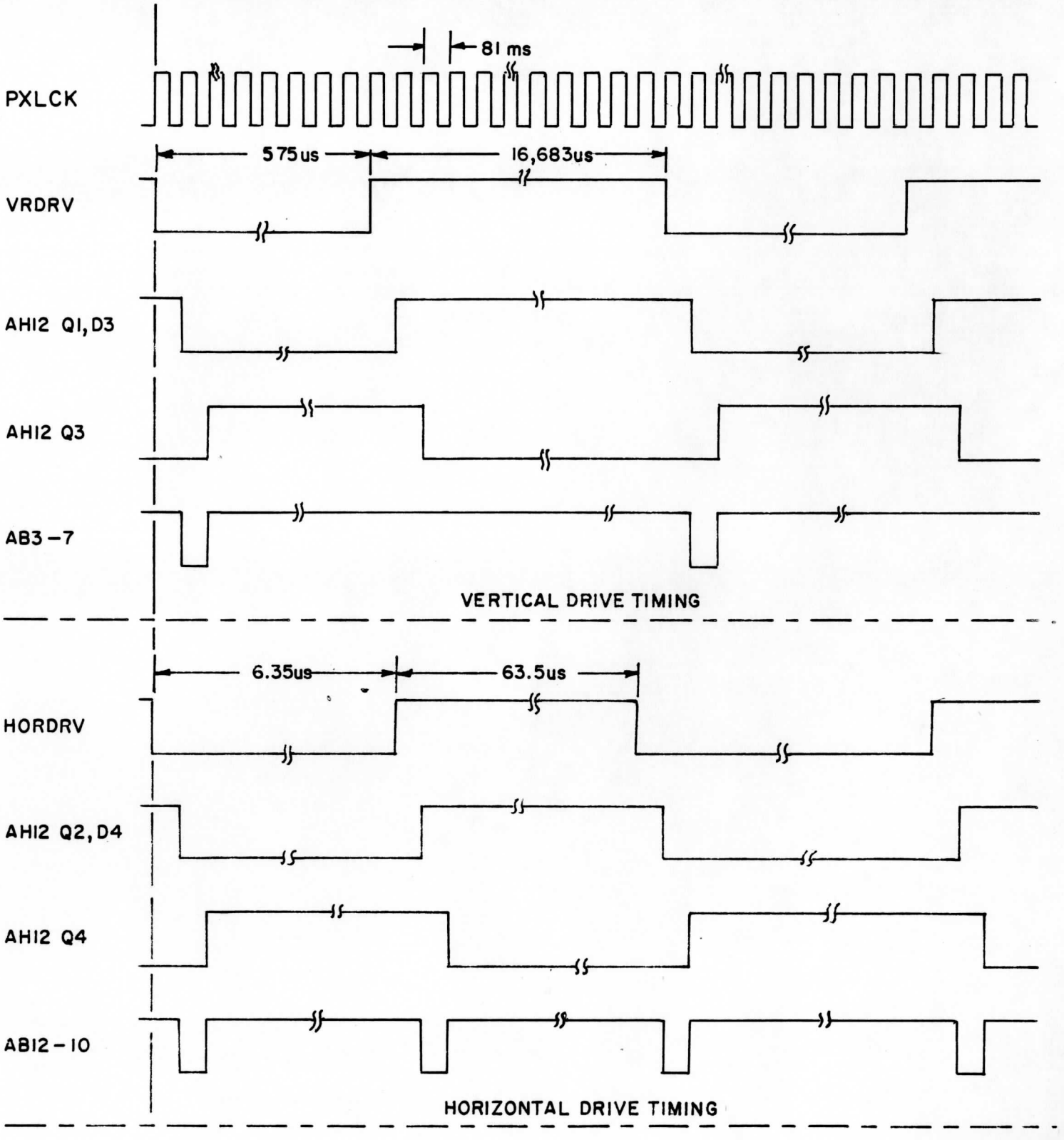
Three timing signals, VRDRV, HORDRV, and PXLCK (vertical drive, horizontal drive, and pixel clock respectively), are applied to this section from the P2 bus via line receivers AP32-A, AP32-B, and AP32-D respectively. The 12.285-Mhz PXLCK (12.272727 Mhz if equipped with the optional NTSC generator) synchronously clocks all D latches and counters in this section.

The horizontal and vertical drive signals (see Timing Diagram 1) are applied to quad D-latch AH12. Two sections of AH12 (#1 and #3) are used by VRDRV while the other two sections (#2 and #4) are used by HORDRV. The latch is wired so that the output of the first section of each pair follows its respective drive signal (VRDRV or HORDV) but delayed one PXLCK period; the output of the second section of each pair is the complement of the respective drive signal and delayed two PXLCK periods. In both sections, the delay between the drive and its complement is one PXLCK period (81 nsec). The vertical drive and its delayed complement are applied to OR gate AB3-C to produce an active low 81-nanosecond pulse at the beginning of each vertical field. The horizontal drive and its delayed complement are applied to Exclusive OR gate AB12-C to produce two active low pulses separated by 6.35 μsec (see Horizontal Drive Timing in Timing Diagram 1). The requirement for two horizontal pulses is explained shortly.

As explained earlier in the Cursor Generator Functional Description, any pixel (or cursor position) can be described by its X,Y coordinates. However, the 525 horizontal lines which make a complete picture are scanned in two alternate groups or fields, containing 262.5 lines per field. During the odd field scan, only the odd lines are scanned; during the even field scan, only the even lines are scanned. Therefore, there is a vertical drive pulse every 262.5 horizontal lines. To properly locate the cursor vertically, the line counter must count both even and odd lines during a field. Therefore, two horizontal pulses per line scan must be sent to the line counter.

The line counter consists of three Up/Down binary counters connected in cascade (V3, V12, and V23). Data inputs from the Addressable Latch (see sheet 1) are applied to the preset inputs of the counters.

The preset data represents the desired distance from the top of the screen to the horizontal center of the cursor. The active low vertical drive pulse output from AB3-C is the preload pulse for the counter. Note that the vertical drive pulse is also applied to the clear input of Z23 (quad D-Latch), resulting in a low level at the output of OR gate X23-D. The output of X23-D drives the Up/Down input on the line counters. Upon receiving a vertical drive pulse, the counters are preloaded to the center line of the cursor and the counter is in a count-down mode.



TIMING DIAGRAM I

CURSOR DRIVE SIGNAL GENERATION

(3504-029 SHT.2)

The only additional inputs to the counters are the Horizontal Drive pulse and pixel clock. The horizontal drive enables the counters for one pixel period twice each horizontal scan, resulting in a double decrement.

The outputs from the counters are applied to AND gate X12 and to a 12-bit comparator consisting of three 4-bit magnitude comparators connected in cascade (T3, T12, and T23). The Addressable Latch supplies cursor range data to the comparator. Refer to Figure 5. The range (vertical width) is the number of horizontal lines above and below the cursor center line. As the counter decrements, it eventually matches the Addressable Latch inputs. When this occurs, the "=" pin (pin 6) of T23 goes active high, indicating that the two sets of inputs to the comparator are equal. This signal indicates the edge of the cursor (top or bottom) and is applied to the D1 input of Z23 via OR gate X23-A. After the next counter decrement, the counter input to the comparator is smaller than the Addressable Latch inputs, causing the "=" pin to return to its inactive low state and the "<" pin (pin 7) to go high. The "<" signal is applied to the D2 input of Z23 via OR gate X23-B; it indicates that this line is an interior cursor line (state 2). The counter continues to count down until it reaches "zero". On the next line, the counter underflows to all binary "one"s, qualifying NAND gate X12. NAND gate X12 is the center detector. The output of the NAND gate is inverted by buffer Z12-A and applied to the D4 input of Z23 via OR gate X23-D. The latched output from Q4 of Z23 is applied to OR gate X23-D. The resulting high output from the OR gate (X23-D) causes the counter to count up through the remainder of the field. The counter continues to count up and the comparator continues to indicate interior cursor lines until the counter and Addressable Latch inputs to the comparator again match, indicating the bottom edge of the cursor (see Figure 5).

The "=", "<", and Center Detector outputs are combined by OR gates X23-A, X23-B, and X23-D and latched by Z23 to form a two-bit binary code. The code is defined as follows:

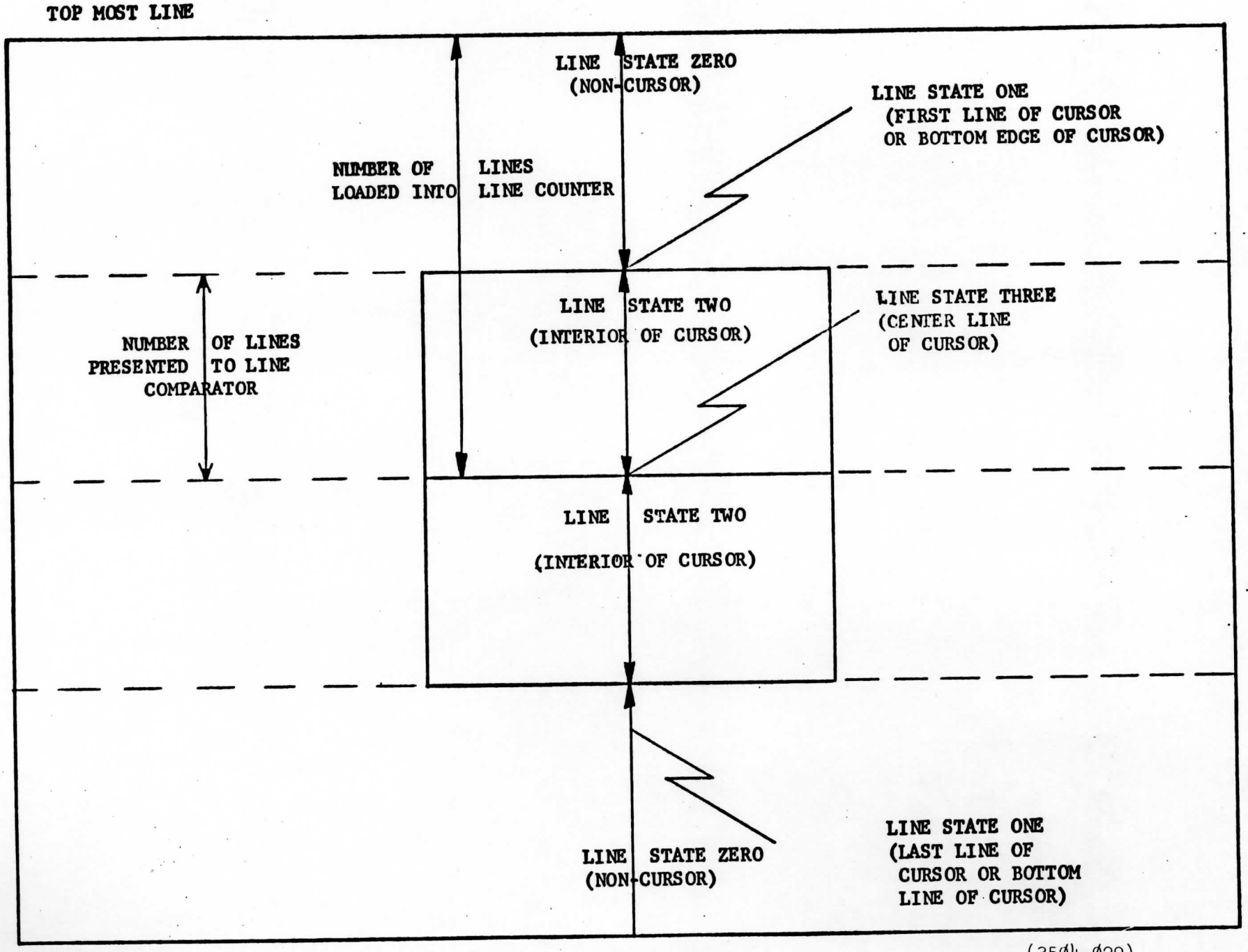


Figure 5. Line Cursor States (Vertical)

State	Q_2	Q_1	Function (Line State)
Ø	Ø	Ø	Non-cursor lines
1	Ø	1	Top or Bottom Edge
2	1	Ø	Interior Cursor Lines
3	1	1	Center Cursor Line

The two-bit binary code, covered after the Pixel Counter Section, is applied to the Cursor Characterizer. The "State" is the decimal equivalent of the two-bit binary code.

Pixel Counter Section

The Pixel Counter Section is shown on SSEC drawing #3504-029, sheet 3 of 5. This section, describing the horizontal position of the cursor, is nearly identical to the line counter section. Only the differences will be discussed here.

Horizontal position is determined by counting pixels from the left edge of the screen. The 12-bit counter (J3, J12, and J23) is pre-loaded with the desired number of pixels, measured from the left of the screen to the vertical center axis of the cursor (refer to Figure 6). During pre-load, the horizontal drive pulse is applied to the load pin of the three counter chips. The counters count down or up at the pixel clock rate (PXLCK). The 12-bit comparator (L3, L12 and L23) compares the input from the counter with the input from the Addressable Latch. The input from the Addressable Latch is the desired cursor width (vertical range) from the edge of the cursor (left or right edge) to the cursor's vertical center line (see figure 6).

The edge-, interior-, and center-detection processes are identical to those in the Line Counter Section. The Q2 and Q3 outputs of latch E23 function as a two-bit binary code and are defined as follows:

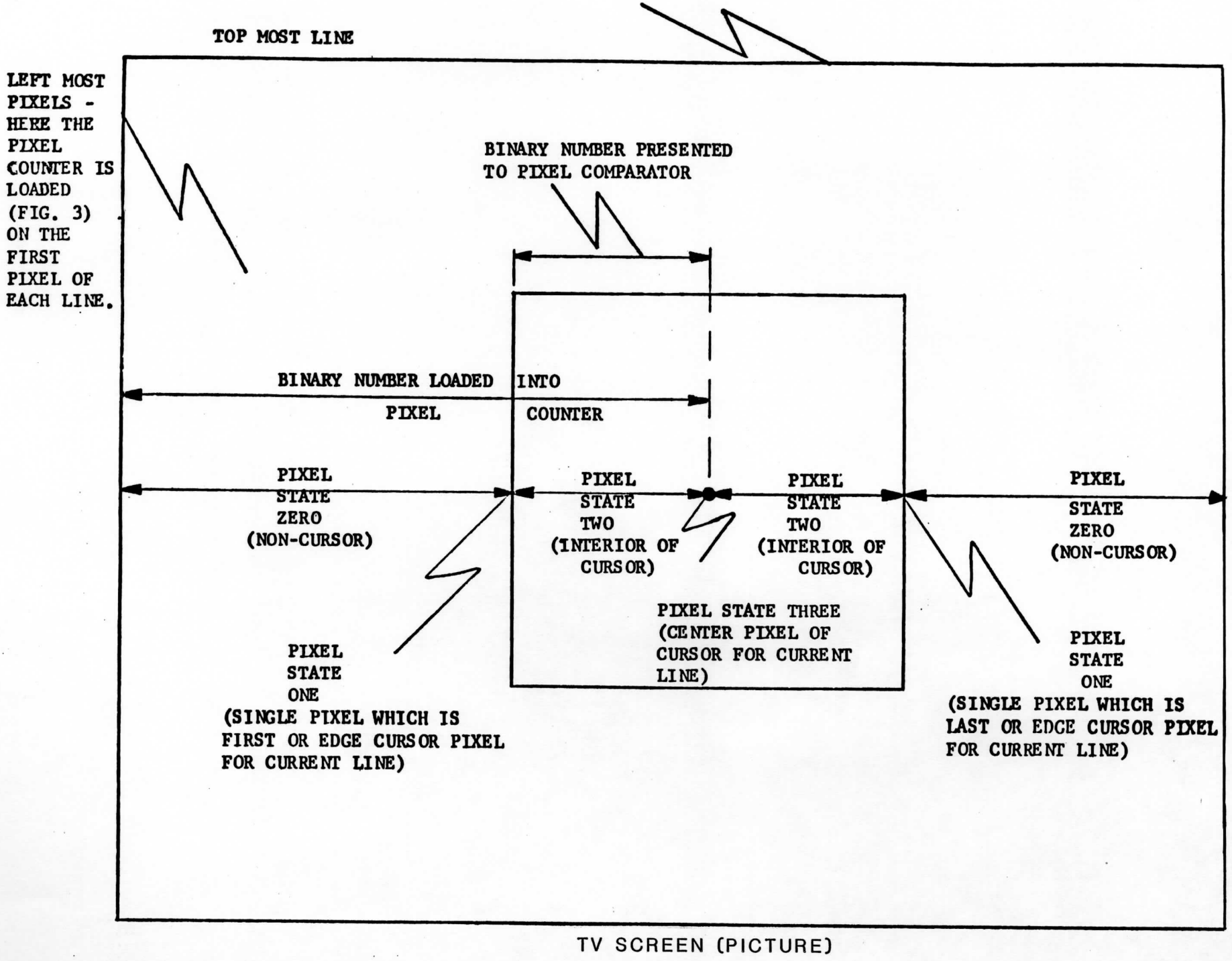


Figure 6. Pixel Cursor States (Horizontal) 3504-029

State	Q_2	Q_1	Function (Pixel State)
Ø	Ø	Ø	Non-cursor pixels
1	Ø	1	Left or right edge cursor pixels
2	1	Ø	Interior cursor pixels
3	1	1	Center cursor pixel

This two-bit binary code is applied to the Cursor Characterizer, discussed in the next paragraph.

Cursor Characterizer Section

The Cursor Characterizer Section is K32, a 16-line to one-line multiplexer; it is located on sheet 3 of 5 on SSEC drawing 35Ø4-Ø29. The multiplexer gates only one of its 16 input lines to the output line (pin 1Ø). An input line is selected by a four-bit address input (A, B, C, and D inputs to pins 15, 14, 13, and 11 respectively). The "A" and "B" address inputs are driven by the two-bit binary state code output of the Line Counter Section output latch, while the "C" and "D" address inputs are driven by the output of the Pixel Counter Section latch. The characterizing input to the multiplexer comes from the Addressable Latch (bytes 6 and 7). There are four binary address inputs, so 16 possible states exist. One of 16 inputs is selected as follows:

PIXEL			LINE				
D	C	State	B	A	State	Input Pin	Characteristic (if selected input is high)
Ø	Ø	Ø	Ø	Ø	Ø	8	Exterior lines and pixels
Ø	Ø	Ø	Ø	1	1	7	Edge line, exterior pixels
Ø	Ø	Ø	1	Ø	2	6	Interior line, exterior pixels
Ø	Ø	Ø	1	1	3	5	Center line, exterior pixels
Ø	1	1	Ø	Ø	Ø	4	Exterior line, edge pixels
Ø	1	1	Ø	1	1	3	Edge line, edge pixel
Ø	1	1	1	Ø	2	2	Interior line, edge pixel
Ø	1	1	1	1	3	1	Center line, edge pixel
1	Ø	2	Ø	Ø	Ø	23	Exterior line, interior pixels
1	Ø	2	Ø	1	1	22	Edge line, interior pixels
1	Ø	2	1	Ø	2	21	Interior line, interior pixels
1	Ø	2	1	1	3	2Ø	Center line, interior pixels
1	1	3	Ø	Ø	Ø	19	Exterior line, center pixels
1	1	3	Ø	1	1	18	Edge line, center pixels
1	1	3	1	Ø	2	17	Interior line, center pixels
1	1	3	1	1	3	16	Center line, center pixel

Figure 7 shows the line and pixel state designations for cursor construction. The output of K32 is sent to the TV Timing and Colorizer board via buffer E12-C, latch E23 and line driver AF1-A. If the output is a "one", the TV Timing and Colorizer board treats the pixel being processed as a "cursor pixel." If the output is a "zero", the TV Timing/Colorizer board treats the pixel as an image or graphics pixel. The Cursor Generator Section provides cursor status information, pixel by pixel, to the TV Timing and Colorizer board.

JOYSTICK SUPPORT INTERFACE CIRCUIT DESCRIPTION

The Joystick Support Interface schematic is located on sheet 4 of 5, on SSEC drawing #35Ø4-Ø29.

The 96ØØ-baud serial asynchronous joystick position data enters the board from J3 pin 5, is converted to TTL logic by line receiver AH3-B, and is applied to the universal asynchronous receiver/transmitter (UART) AF23.

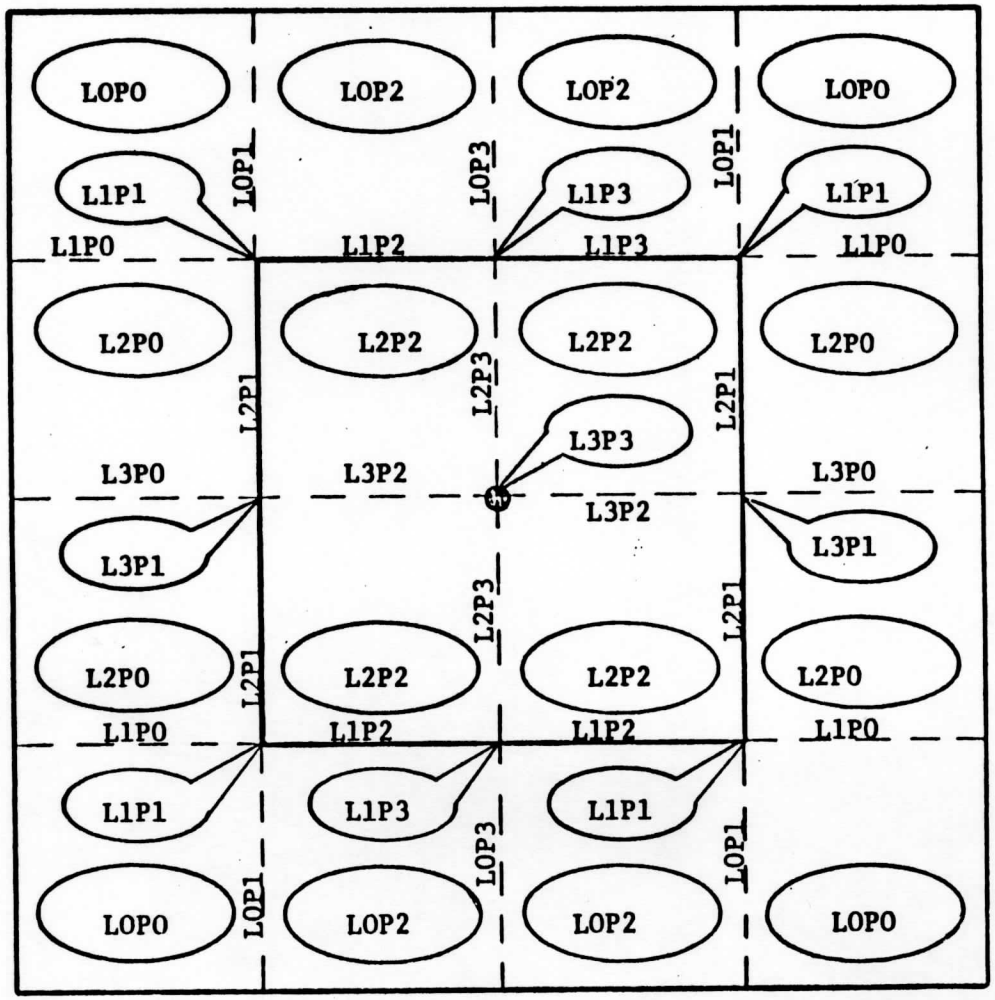


Figure 7. State Designations for Cursor Construction (35Ø4-Ø29)

Similarly, the 153.6-Khz clock enters the board from J3 pin 8, is converted to TTL by AH3-A, and is applied to the clock input (pin 17) of the UART. The Multibus initialization signal (INIT/) enters the board from P1 pin 14, is buffered and inverted by hex buffer Z12-D, and is applied to the master reset (pin 21) on the UART. This initializes (clears) the UART during power-up and manual reset. The program wiring of CLS1, CLS2, SBS, PI, and CLR (pins 38, 37, 36, 35, and 34 respectively) configures the UART for eight data bits, odd parity and two stop bits. The parity bit is invalid, as explained in the "Kraft Digital Joystick" or "Miniature Joystick" circuit description. The Parity Error output (pin 13) from the UART is not used.

When the UART detects the completion of a character, the following happens:

- the eight data bits are latched into the output receive buffer (RB1-RB8, RB1 is LSB)
- the data-received line (DR) goes active high

After the DR line goes high, it must be cleared before completion of the next character (1.25 ms). By providing a high input to DRR (data received reset) pin 18, DRR is interpreted by the UART as a "data read complete." The UART resets the DR to inactive low. The DR output signal is used as one of the inputs to the State Machine (AF1Ø, AD1Ø and AB23). The DRR reset input signal is an output from the State Machine. Note that the LSB (RBR1) of the eight-bit output register is also used as an input to the State Machine. This is the "ID" bit in each character transmitted by the Kraft Digital (or Miniature) Joystick board. If the bit is a "zero", RBR2-RBR8 contain the lower seven data bits (RBR2 is LSB). If the bit is a "one", RBR4-RBR8 contain the upper five data bits (RBR8 is MSB).

There are three requirements for storing data into the register file (Z32, AB32, and AD32): all 12 data bits must be presented to the file at the same time, a file address must be selected, and a "Write Enable" must be applied to the file. The State Machine outputs an active logic low from Y_1 (pin 14) of AB23 when DR is a logic high and the "ID" is a logic low. This signal latches the data inputs into octal latch AD21. The inputs to AD21 are the seven least significant data bits of a joystick position. Note that the two LSBs from the UART are applied to two exclusive OR gates. These gates function as buffers, required because of the

extra TTL loads on these two lines. (In addition to supplying the D1 and D2 latch inputs, the buffers drive the "Write Address" lines on all three register file chips.) After AD21 is latched, its seven data bits are present at the seven LSB input positions of the register file. After the UART completes the next character, DR goes high again; but this time, the "ID" bit is also high. At this time, RBR4-RBR8 are outputting the upper five data bits to the five MSBs of the register file, fulfilling the first requirement for storing data in the data file. Remember, the potentiometer address is contained in the second and third bit positions of the second character (the two buffered UART output lines). The address data is presented to the latch, but has no effect because the latch inputs are not enabled at this time. The address data is also applied to "Write Address" inputs to the register file (pins 12 and 13), fulfilling the second requirement for storing data in the register file. Only the application of a "Write Enable" pulse is needed to write the data into the register file. This pulse is generated by the State Machine.

The State Machine is best understood by examining it during two separate process cycles, data storage and data retrieval. Since we have just finished describing the data storage process, that portion of the State Machine is addressed. The State Machine consists of the following:

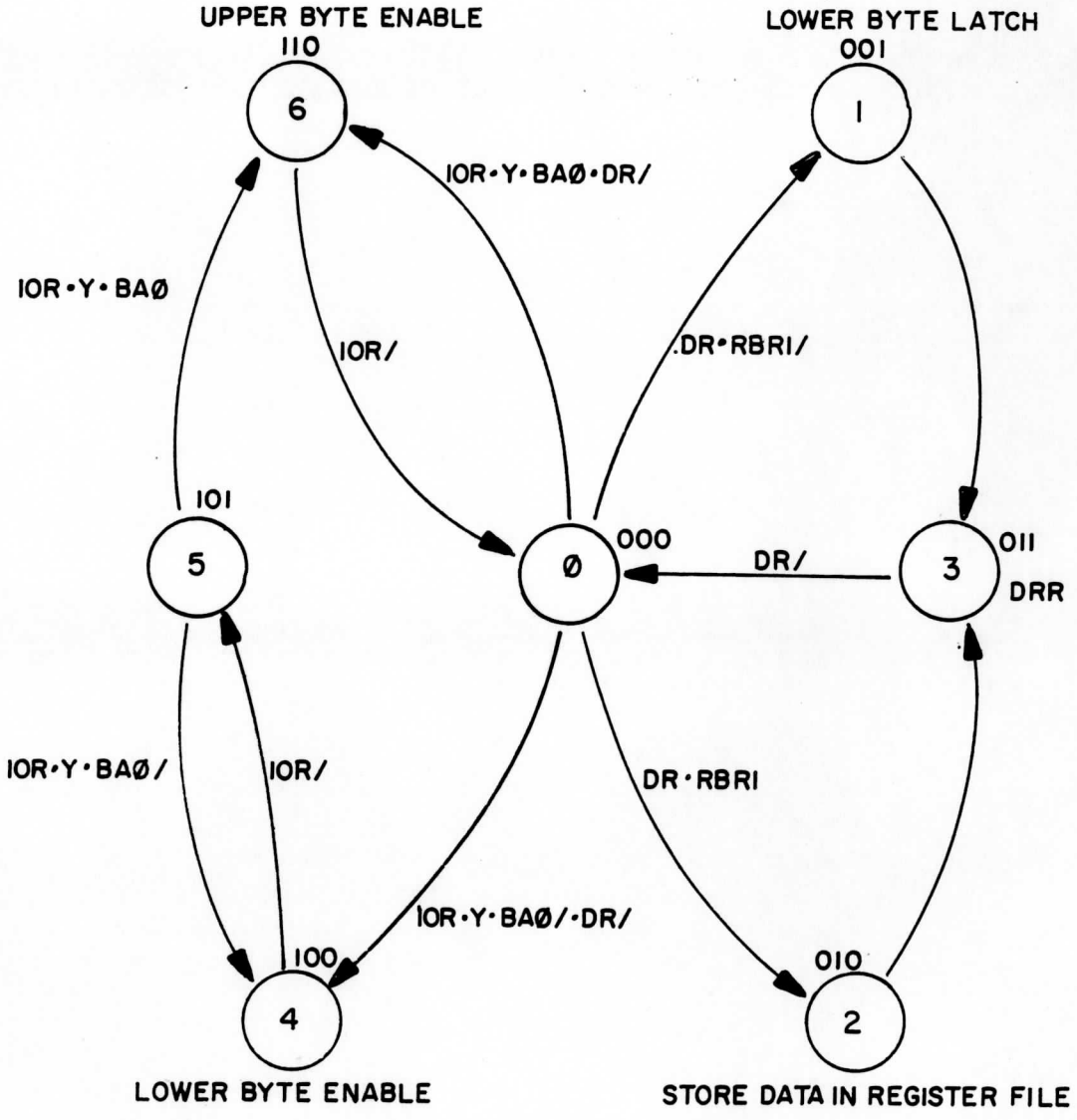
- octal D-latch AF1Ø
- PROM AD1Ø
- 3-to-8 line decoder AB23

Note that the least significant three bits output from the PROM are used as the least significant three bits input to the latch. Because the latch output drives the PROM address lines (lower eight lines) and the latch is clocked by the Multibus 9.68-Mhz clock (SBCCK, P1-31), the present PROM output always determines the A5, A6, and A7 (AD1Ø pins 2, 1, and 15 respectively) inputs after the next 9.68-Mhz clock pulse. The present PROM output becomes a directory to the next process. By loading the proper data into the PROM, a very complicated sequence of timing steps is possible with just three components. Because the inputs to the 3-to-8 line decoder are actually the A5, A6, and A7 address lines, a PROM address-to-decoder function correlation can be made. The table below, shows this correlation.

PROM Address (Hexidecimal)	Decoder Output	Function
ØØØ-Ø1F	$Y_Ø$	not used
Ø2Ø-Ø3F	Y_1	1st character latch
Ø4Ø-Ø5F	Y_2	position data store
Ø6Ø-Ø7F	Y_3	data received reset
Ø8Ø-Ø9F	Y_4	LS 8 bit read
ØAØ-ØBF	Y_5	not used
ØCØ-ØDF	Y_6	MS 4 bit read
ØEØ-OFF	Y_7	not used

During the following analysis, refer to Figure 8, the Joystick Support State Diagram, and the PROM code listings (at the end of this section). If we assume that no data "read" or "write" is in progress, then IORC=Ø, Y=Ø, and DR=Ø. RBR1 and BAØ are not significant (as we will see). The possible address inputs to the PROM under these conditions are ØØH, Ø2H, Ø4H, or Ø6H. The output from the PROM, in each case, is ØH, therefore, the output from AB23 is $Y_Ø$ (idle output).

Assume that the first character of a pot position data pair has just become available (DR goes high and RBR1 is low). After the next 9.68-Mhz clock pulse, the input to the PROM is ØØ1H or ØØ5H (we don't know about BAØ yet). In either case, the PROM output is Ø1H and the data input to the latch is 84H or A4H. After the next clock pulse, this data is latched into the PROM address inputs as Ø21H or Ø25H and the inputs to the decoder yield Y_1 (state 1 in Figure 8). Y_1 causes the octal latch (AD21) to store the UART output data. The PROM input produces an output of Ø3H and the latch (AF1Ø) input is now 86H or A6H. After the next clock pulse, the input to the PROM is Ø61H or Ø65H and the decoder outputs Y_3 (state 3 in Figure 8), resetting DR. When DR is reset, the next clock pulse provides an address of 6ØH or 64H to the PROM, generating an output of ØH. After the next clock pulse, the PROM is back to ØØØH or ØØ4H. Assume that the second character has just arrived and BAØ = "zero", as it has no effect during data store cycles. The latch (AF1Ø) input is ØCØH. After the next clock pulse, the PROM input is ØØ3H, causing an output of Ø2H. With a



JOYSTICK SUPPORT STATE DIAGRAM

FIGURE 8

(3504-029)

PROM output of Ø2H, the latch (AF1Ø) input is ØC2H. After the next clock pulse, the PROM input address is Ø43H, producing an output from AB23 of Y_2 (state 2 in Figure 8). Y_2 is the Write Enable for the Register File. The lower seven bits (stored in latch AD21) and the upper five data bits from the UART are stored in one of the files (determined by the Write Address inputs). With a PROM input of Ø43H, the output is Ø3H. After the next clock pulse, the decoder generates a Y_3 output and resets the DR line. The PROM address input is now Ø63H. With the DR line reset and RBR1 still set, the latch data input is Ø46H. After the next clock pulse, the input to the PROM is Ø62H, generating an output of ØH. After the next clock pulse, the PROM input is ØØ2H and the decoder's output returns to $Y_Ø$, completing the cycle.

The data read analysis process is identical to the data read analysis just described (see above analysis). A listing of the data read control signal inputs follows:

- IORC (I/O Read Command)
- Y (addresses 78-7F hex)
- BAØ (address bit zero)

Note that the BA1 and BA2 are used as read address lines for the Register File. BA1 and BA2 select the file number (1, 2, 3, or 4), while BAØ, via the State Machine, selects which byte (lower or upper). Specifically, the State Machine requires that both IORC and Y must be present before BAØ determines which byte to output. Note that JACK goes true any time a data read request is processed (see Common Circuits Description).

It appears that many of the PROM states were not used because only one function (of the two) was analyzed at a time. Often, both functions are processed concurrently, accessing other PROM states. The following are interesting features about the programming of the State Machine:

1. After a two-byte read cycle process begins, nothing can break into it (UART must wait).
2. If the UART requests service at the same time that a read cycle is requested, the UART is serviced first.

GRAPHICS TABLET INTERFACE CIRCUIT DESCRIPTION

The Graphics Tablet Interface circuit (sheet 5 of the schematic) is very similar to the Joystick Support Interface circuit. The hardware

differences are a result of data format differences, different baud rates and a Pen Status circuit in the Graphics Tablet Interface circuit. There is a different PROM program in the State Machine, though the hardware is identical.

The RS-232 receiver is UART AJ23. 19,2ØØ-baud serial asynchronous receive data enters the board from the Summagraphics Bit Pad One graphics tablet via J2 pin 3. Line receiver AH3-D converts the RS-232 levels to TTL logic levels. This UART requires a clock frequency (3Ø7.2 Khz) that is 16 times the data frequency (19.2 Khz). The graphics tablet does not produce and transmit this clock with the data; it must be generated on this board, as explained in the next paragraph. The UART is configured for eight data bits, odd parity, and two stop bits. The UART is initialized by the same signal which initializes the Joystick Support Interface UART (INIT).

The Clock Generator consists of 9.8304-Mhz crystal oscillator AM28, inverting buffer Z12-F, D latch AP19, and four-bit binary counter AM37. The output from the oscillator is buffered by Z12-F and applied to the latch AP19 and the Pen Status circuit. AP19 is configured as a divide-by-two circuit, yielding an output frequency of 4.9152 Mhz. The latch output is applied to the counter, which divides the input by 16, producing the desired 3Ø7.2-Khz UART clock frequency. The clock is supplied to both the transmit and receive clock pins on the UART, though the transmit capability of the UART is not used.

The Graphics Tablet Interface receives serial data, converts it to parallel data, and writes it into a Register File. The Register File, discussed in this section, reveals most of the timing requirements of the remaining circuits in this section.

There are two Register Files, a Data Register File and a Status Register File. The Data Register File consists of AK1 and AM1. The least significant four data bits from the UART (RBR1-RBR4) are applied to AM1 (D1-D4 respectively) and RBR6-RBR7 are applied to AK1 (D1 and D2 respectively). The most significant two bits in AK1 are tied high. Therefore, AK1 contains the two most significant data bits and AM1 contains the four LSBs. The six data bits of the four coordinate characters are stored in the Data Register File. Two data reads are required by the CPU to read the X or Y coordinate data because only six bits are stored in each file position.

The Status Register File is AP1. The format of the Status Flag Character is:

P	7	6	5	4	3	2	1	UART Bit RBR
P	1	D	D	D	F	Ø	Ø	Data

D = Don't Care
P = Parity
F = Flag

The first two bits of the flag word are always "zero", so they are not stored in the Status Register File. Bit 6 and the parity bit also are not stored. The tip of the Graphics Tablet pen is spring-loaded; when pressed against the tablet surface, bit 3 of the Status Flag Character is set. This is the actual flag bit. PDR is the buffered DR output (UART pin 19) from the UART. PDR goes active high from the time that the UART finishes reception of a character (data or status) until after the character is stored in one of the Register Files. Note that PDR and bit 2 are ANDed by AND gate X3-B and applied to D1 of the Status Register File. PDR is also applied directly to the D4 input of the file. D2 and D3 (bits 4 and 5) have no use in the file. D1 and D4 carry the required status information. The Status Register File can receive a Write Enable (AP1 pin 12) from two different sources via gate Z3-D. When the UART receives a character and RBR7 (signal TRBR7) is high (Status Flag Character), the State Machine outputs a Write Enable from pin 13 of AP10, latching a "one" into D1 and D4 of AP1. The other Write Enable source is the Pen Status Circuit. The Pen Status Circuit is a timer, prevented from reaching its timeout as long as data groups are being received ("Pen Down"). If the pen is down, the Write Enables come from the State Machine only.

The Pen Status Circuit consists of inverter AB12-A, 16-stage binary counter AD1, quad latch AP19, and gate X23-C. The counter counts UART clock pulses (3Ø7.2 Khz), resulting in a natural output frequency of 75 hz (6.67-ms low half cycle followed by a 6.67-ms high half cycle). When the pen is down, the counter is reset at least every 4.54 msec,* preventing it from reaching its high half cycle. If the pen is lifted, pin 1 of AD1

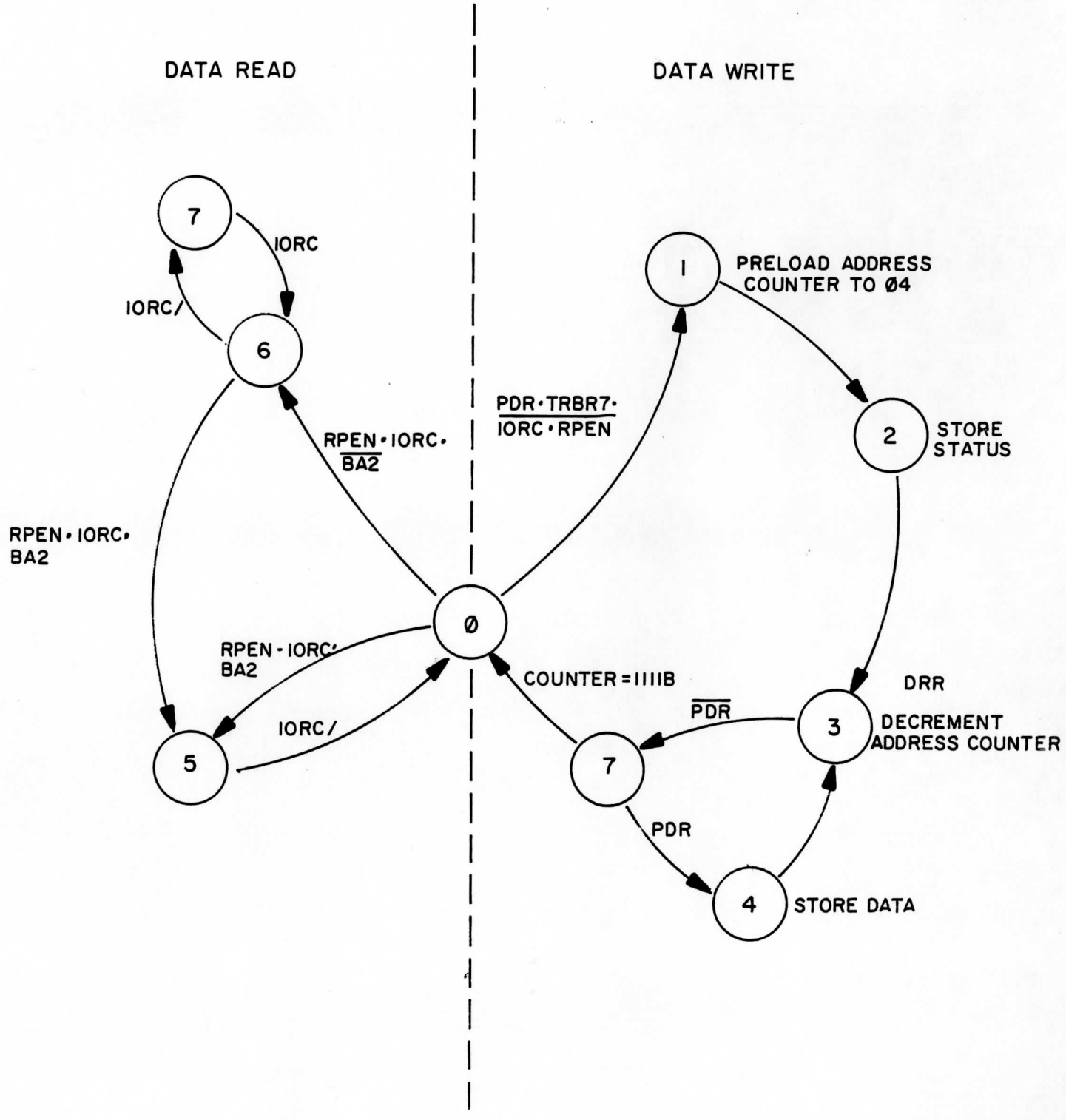
---

*The time between character 5 reset and the next Flag Character reset (at 135 groups of five characters per second) is 4.54 msec. The time between resets for characters within the same group is 0.573 msec.

goes high 6.67 msec after the last DR reset, providing a high level input to AP19 D3. AP19 is a rising edge detector. AP19 is clocked by the 9.8304-Mhz clock and generates an active low Write Enable pulse at the output of gate X23-C, two clock pulses after the D3 input of AP19 goes high. When this Write Enable pulse is generated, the UART output is still the 6 MSBs of the last Y coordinate. This loads a "zero" into the D1 and D4 positions of the Status Register File because PDR is a "zero". The first clock pulse into AP19, after D3 goes high, produces a "zero" at AP19-11 (PROXLD/). This signal forces the Storage Address Generator to an address of Ø1ØØB before the Status Register File Write Enable is applied. Therefore, regardless of which Write Enable source causes data to be loaded into the Status Register File, only address ØØ is used (only the two LSBs of the Storage Address Generator are used).

The Storage Address Generator consists of 4-stage binary counter AM19 and gate X3-A. The Data Received Reset (DRR) for the UART is applied to the counter as a clock and the counter is configured as a down counter. Immediately after detecting a Flag Character, the State Machine loads the counter with a count of Ø1ØØB, by setting Y_1 of AP1Ø low. Because only the two LSBs of the counter are used, an effective address of ØØ is output to the Register Files. The State Machine generates a Write Enable on the next clock pulse. On the next clock pulse, the State Machine generates the DRR pulse which causes the counter to decrement to a count of ØØ11B (an effective address of 3). With the reception of each new character, the State Machine stores data and then decrements the counter, until the counter reaches an underflow count of 1111 (MSB of Y stored at address ØØØØB followed by a counter decrement). The second MSB of the counter is ORed with an active high "Pen Up" signal from the Pen Status Circuit (AP19 Q3) and applied to the State Machine as a status.

The State Machine consists of octal latch AK1Ø, PROM AM1Ø, and 3-to-8 line decoder AP1Ø. The operation of these components is similar to the operation of the Joystick Support Interface State Machine, already described (see the preceding section). Also, a listing of the PROM program and a State Diagram (see Figure 9) are included, if you want to analyze the logic more carefully. The State Machine is analyzed in terms of inputs, sequences, and outputs, during data "write," data "read," and simultaneous requests for data "read," and data "write."



GRAPHICS TABLET INTERFACE STATE DIAGRAM

FIGURE 9

(3504-029)

The following are State Machine input requirements for data write operations:

- PDR (buffered UART data received signal)
- TRBR7 (Flag/Data identification bit)

The sequence which the State Machine goes through, assuming the pen is down for one data group and then raised, is as follows:

1. $Y_{\emptyset}$ initially active (not used)
2. Y_1 active (preload the address counter to Ø1ØØB)
3. Y_2 active (store status at address ØØB in Status Register File)
4. Y_3 active (decrement address counter to ØØ11B and reset the data received line on the UART)
5. Y_7 active (not used, idle state until next character is received)
6. Y_4 active (store first data byte at address ØØ11B)
7. Y_3 active (decrement counter to ØØ1ØB and reset DR)
8. Y_7 active (idle state)
9. Y_4 active (store second data byte at address ØØ1ØB)
10. Y_3 active (decrement counter to ØØØ1B and reset DR)
11. Y_7 active (idle state)
12. Y_4 active (store third data byte at address ØØØ1B)
13. Y_3 active (decrement counter to ØØØØB and reset DR)
14. Y_7 active (idle state)
15. Y_4 active (store fourth data byte at address ØØØØB)
16. Y_3 active (decrement counter to 1111B and reset DR)
17. Y_7 active (idle state)
18. $Y_{\emptyset}$ active (process complete)

The following are State Machine input requirements for data read operations:

- IORC (I/O read command)
- RPEN (addresses 7Ø-74H)
- BA2 (Multibus address bit 2)

When IORC and RPEN are both active, the level on BA2 determines which register file is "read" enabled. If BA2 = "zero", the Data Register File is enabled and if BA2 = "one", the Status Register File is enabled. Once a Data Register File "read" operation starts, it can only be ended by reading the Status Register File (see Figure 9). For this analysis, each

of the Data Register Files is read, followed by reading of the Status Register File. The sequence is as follows:

1. $Y_{\emptyset}$ active (idle)
2. Y_6 active (Data Register File read enable)
   Note: BA1 and BA$\emptyset$ determine which data file is read, as follows:

BA1	BA$\emptyset$	data
$\emptyset$	$\emptyset$	Y MSB coordinate data
$\emptyset$	1	Y LSB coordinate data
1	$\emptyset$	X MSB coordinate data
1	1	X LSB coordinate data

3. Y_7 active (not used)
4. Y_6 active (Data Register File read - see note above)
5. Y_7 active (not used)
6. Y_6 active (Data Register File read - see note above)
7. Y_7 active (not used)
8. Y_6 active (Data Register File read - see note above)
9. Y_7 active (not used)
10. Y_5 active (Status Register File read)
11. $Y_{\emptyset}$ active (idle)

A simultaneous request for a data "read" and a data "write" process is resolved in favor of the data "read" request. However, once a data "write" process begins, the "read" request must wait until all five characters in the data group are received. This can effectively hang up the microprocessor for as long as 2.86 msec per character group.

PROM #53

CHECKSUM = 4536 INTEGER
= 11B8 HEX

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	0	1	0	2	0	1	0	2	0	1	0	2	0	1	0	2
01	0	1	0	2	0	1	0	2	4	1	4	2	6	1	6	2
02	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
03	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
04	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
05	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
06	0	3	0	3	0	3	0	3	0	3	0	3	0	3	0	3
07	0	3	0	3	0	3	0	3	0	3	0	3	0	3	0	3
08	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
09	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
0A	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
0B	5	5	5	5	5	5	5	5	4	4	4	4	6	6	6	6
0C	0	1	0	2	0	1	0	2	0	1	0	2	0	1	0	2
0D	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
0E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
11	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
12	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
13	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
14	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
15	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
16	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
17	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
18	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
19	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1B	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

PROM #55C

CHECKSUM = 1672 INTEGER
= 688 HEX

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	6	6	6	6	5	5	5	5	0	B	0	1	0	B	0	1
01	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
02	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
03	7	3	7	3	7	3	7	3	7	3	7	3	7	3	7	3
04	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
05	5	5	5	5	5	5	5	5	0	0	0	0	0	0	0	0
06	6	6	6	6	6	6	6	6	F	F	F	F	F	F	F	F
07	7	4	7	0	7	4	7	0	7	4	7	0	7	4	7	0
08	8	8	8	8	8	8	8	8	0	0	0	0	0	0	0	0
09	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B	0	B	0	B	0	B	0	B	0	B	0	B	0	B	0	B
0C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0F	6	6	6	6	5	5	5	5	F	F	F	F	F	F	F	F
10	6	6	6	6	5	5	5	5	0	B	0	1	0	B	0	1
11	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
12	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
13	7	3	7	3	7	3	7	3	7	3	7	3	7	3	7	3
14	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
15	5	5	5	5	5	5	5	5	0	0	0	0	0	0	0	0
16	6	6	6	6	6	6	6	6	F	F	F	F	F	F	F	F
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	8	8	8	8	8	8	8	8	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1B	0	B	0	B	0	B	0	B	0	B	0	B	0	B	0	B
1C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1F	6	6	6	6	5	5	5	5	F	F	F	F	F	F	F	F

PROM #54A

CHECKSUM = 149 INTEGER
= 95 HEX

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
06	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
08	A	A	A	A	A	A	A	A	0	9	0	C	C	C	C	C
09	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SECTION 6
BISYNCHRONOUS COMMUNICATIONS MODULE
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BISYNCHRONOUS COMMUNICATIONS MODULE

(SSEC DRAWING 645Ø-ØØ85, MODIFICATION AC, DATED 8/21/84)

INTRODUCTION

The Bisynchronous Communications Module (Bisync) provides a synchronous, bidirectional, serial data link between the McIDAS workstation and the host computer. The link can transmit and receive data at rates of up to 614.4K baud. It has an error detection mode that incorporates a cyclic redundancy code (CRC) generator and checker for validating the data received over an RS-232C serial data link. The term "bisynchronous" is defined as capable of simultaneous synchronous transmission and reception of data.

Transmissions between the workstation and the host computer are sent in units called messages. Each message begins with two sync characters, for synchronization, followed by a start-of-transmission marker (STX), and ending with an end-of-message marker (EOM). Each message is made up of one or more sub-units called packets. Each packet begins with a start-of-packet (SOP) marker and ends with an end of packet (EOP) marker (the last packet ends with EOM). CRC error checking is done on each packet and is compared to the two 8-bit CRC characters immediately following the EOP or EOM marker. The general form of a message is:

```
SYN SYN  | STX <DATA> EOP P1 P2 | SOP <DATA> EOM P1 P2 |
              packet #1              packet #2
```

where:

SYN = synchronizing character

STX = start of transmission

<DATA> = packet data, including internal record separators and routing codes

EOP = end of packet

P1 = least significant eight bits of the CRC code

P2 = most significant eight bits of the CRC code

EOM = end of message

For more information on the data formats, routing codes, and record separators, refer to the SSEC document HOST TO TERMINAL - TERMINAL TO HOST SYSTEM PROTOCOL DESCRIPTION, dated 11 September, 1984.

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the Bisynchronous Communications module.

The Bisync module is divided into the following five functional sections:

- Multibus Interface Section
- Memory Section
- Transmitter Section
- Receiver Section
- RS-232 Interface Section

MULTIBUS INTERFACE SECTION

Any block which connects to the Multibus address, control, or data bus is technically part of the Multibus Interface Section. But, in the case of the Memory Data Multiplexer and Memory Address Multiplexer blocks, their primary functions place them in other sections. The following blocks in Figure 1 are primarily Multibus-interfacing in function:

- Unit Select and Read/Write Controller
- Status Buffer
- Control Register
- Timing Generator

The Unit Select and Read/Write Controller block contains programmable I/O-mapping and memory-mapping circuits. When the address on the Multibus address bus matches the programmed address, a memory-mapped or I/O-mapped read or write control signal is generated. The Memory Read and Memory Write Control signals are used to control memory block reading and writing operations. The I/O Read signal dumps Bisync Card Status onto the Multibus data bus and the I/O Write signal latches a Multibus data bus-transported control word into the Bisync Card.

The Status Buffer block is a tri-state buffer which monitors transmitter and receiver status. It also monitors the latched MSB address bits of the transmitter and receiver buffer memories. This is covered in more

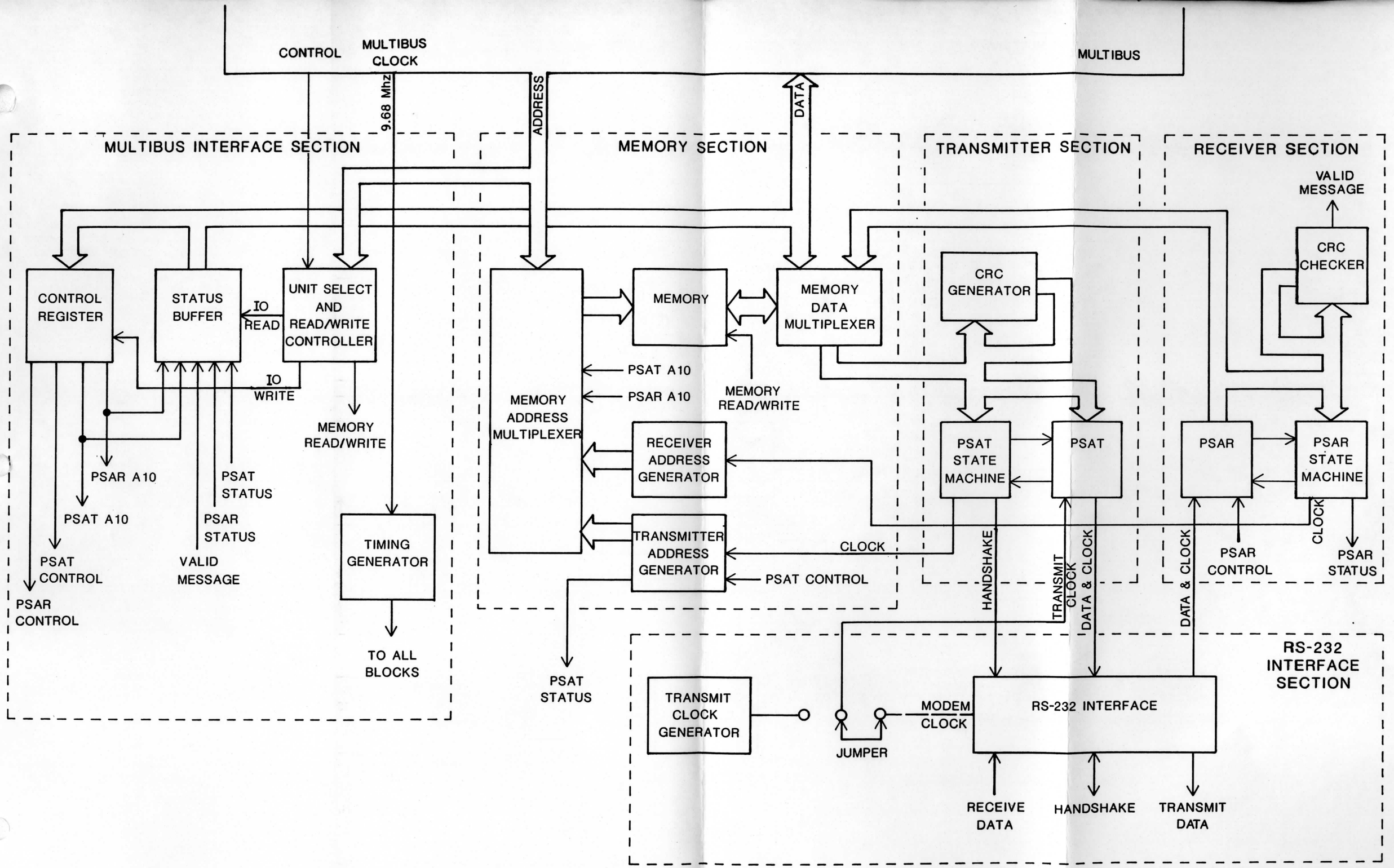


FIGURE 1. BISYNCHRONOUS COMMUNICATIONS MODULE FUNCTIONAL BLOCK DIAGRAM

detail in the following paragraph and in the Memory Address Multiplexer description.

The Control Register block is a four-bit data register, latched by the I/O Write signal. The register initiates a message transmission via the PSAT (Programmable Synchronous and Asynchronous Transmitter) Control outputs, activates (turns on) the receiver via the PSAR (Programmable Synchronous and Asynchronous Receiver) Control signal, and assigns the transmitter or receiver to the appropriate half of the buffer memory via the PSAT and PSAR A1Ø signals. These signals must always be logical opposites. The signal that is a logical high controls the upper 1Ø24 bytes of memory while the logic low controls the lower 1Ø24 bytes. Thus, the transmitter and receiver can be assigned to either half of the memory. The states of PSAT A1Ø and PSAR A1Ø are also inputs to the Status Buffer block.

The Timing Generator block divides the 9.68-Mhz Single Board Computer (SBC) clock to produce a 6Ø5-Khz, four-phase timing signal. Four-phase timing is used primarily by the multiplexers in the Memory Section but the Timing Generator provides timing (6Ø5 Khz or multiples of 6Ø5 Khz) to nearly all blocks in Figure 1.

MEMORY SECTION

The Memory Section consists of the following blocks:

- Memory block
- Memory Data Multiplexing block
- Memory Address Multiplexing block
- Transmitter Address Generator
- Receiver Address Generator

The Memory block is a 2Ø48 (2K)-byte by eight-bit static RAM memory. It is logically divided into two 1K memories which function as buffers for the transmitter and receiver. Because, even at the highest baud rates (614K baud), the serial data link is slow compared to the microprocessor, all communication with the Bisync card is via the buffers. When the microprocessor must transmit a message, it loads the message into the buffer at unrestricted speed. Then, via the Control register, it initiates the transmission. After the transmission is initiated, the Bisync Card transmits the message at the relatively slow serial baud rate. During the reception of an incoming message, the Receiver section

automatically receives the message and stores it in the receiver section of the memory. At completion, the receiver sends a "message received" status signal to the Status Register. Periodically, the microprocessor reads the Bisync Status and, detecting a "message received" status, reads the Receiver's buffer, again, at unrestricted speed.

In addition to the microprocessor, two sections of the Bisync Card read or write data to the same memory. A multiplexer for both the data and address lines is required to make the process orderly and predictable. The Memory Data Multiplexer and the Memory Address Multiplexer receive timing information from the Timing Generator block, located in the Multibus Interface Section. Several outputs from the Timing Generator block are combined to produce a four-phase control cycle. This control cycle drives the multiplexers; they sequentially select the receiver, Multibus, transmitter and Multibus, in that order. Because each phase is equal in length, the microprocessor, via the Multibus, has control of the buffers 5Ø% of the time while the receiver and transmitter each have control 25% of the time. This multiplexing scheme is referred to as Time Division Multiplexing (TDM).

Transmitter and receiver address generation are accomplished by the Transmitter Address Generator and Receiver Address Generator respectively. The generators are binary counters, controlled by the respective state machines.

TRANSMITTER

The core of the transmitter section is a single large-scale-integrated circuit (LSI), called a "Programmable Synchronous and Asynchronous Transmitter" (PSAT). This chip converts the eight-bit parallel input data to serial output data. The device operates in one of three modes: asynchronous, isochronous and synchronous. The device generates and appends even parity, odd parity or no parity and can transmit characters of five, six, seven, or eight bits. In the McIDAS, this chip is programmed, by tying various programming pins to VCC or ground, for synchronous mode, no parity, and eight-bit character length.

After synchronous data transmissions begin, the transmitter cannot be allowed to run out of data. If this happens, the receiving device loses synchronism and is unable to assemble the remainder of the message. When

no data is available and the transmitter is still active, the PSAT transmits a filler character. This filler character is programmed by tying inputs from the Filler Character Register (FR) to VCC or ground. The Filler Character is programmed as an FFH by tying all FR inputs to VCC.

The transmitter section includes the CRC Generator and the PSAT State Machine. The CRC Generator is a 14-pin IC. It is a 16-bit programmable device that operates on serial data streams and detects transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. The resulting remainder is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, the division results in a "zero" remainder. Although it is possible to choose many generating polynomials of a given degree, there are standards that specify a small number of useful polynomials. The CRC Generator uses one of eight possible polynomials, determined by programming three polynomial select pins. The polynomial used in the McIDAS workstation is in the form $X^{16} + X^{15} + X^2 + 1$ and is referred to as "CRC-16".

The PSAT State Machine controls the entire transmitter section. It performs the following functions:

- clears the CRC Generator at the beginning of each message
- loads new data into the transmitter
- loads the CRC check code at the end of each message (if required)
- increments the Transmitter Address Generator each time a word is read from the transmitter buffer memory

RECEIVER

The main component of the receiver section is an LSI IC called a "Programmable Synchronous and Asynchronous Receiver" (PSAR). The PSAR is a companion chip for the PSAT. The PSAR chip converts serial RS-232 receive data to parallel characters, checks the parity (if programmed to do so) and generates a "Data Ready" (DR) signal each time a new character is completed. Mode of operation, character length, and parity mode are

all programmable as discussed above for the PSAT. However, instead of using a Fill Character Register (like the PSAT), the PSAR employs a Sync Character Match Holding Register (MHR). In the synchronous mode of operation, the input data stream shifts through a PSAR shift register. The register's parallel outputs are compared with the programmed sync character. When there is a match, the receiver is in synchronism with the transmitter. After that, the serial data stream is converted to five-, six-, seven-, or eight-bit characters and transported to its output buffer.

The receiver section includes a CRC Checker and the PSAR State Machine. The CRC Checker is the same as the one used in the transmitter. In fact, the only differences between the two circuits are the output pin connections. The data output is used in the transmitter while the error output is used in the receiver.

The PSAR State Machine controls the entire receiver section. It performs the following functions:

- stores data in the receiver buffer memory
- clears the CRC Checker at the beginning of each message
- clears the Data Ready flag in the PSAR
- controls the processing of the CRC check characters
- writes the message status to the receiver buffer memory

RS-232 INTERFACE

The RS-232 Interface section consists of line drivers, line receivers, and minor small-scale TTL logic. The control signals are receiver and transmitter clocks and interface handshake signals. The data is serially transmitted and received.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the Bisynchronous Communications Module is shown on SSEC drawing #645Ø-ØØ85 (Modification AC, dated 8/21/84). The schematic circuit analysis is accomplished by analyzing groups of components, represented by a single block in Figure 1.

SCHEMATIC CONVENTIONS

To refer to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and the section letter designator. The symbol ID number alone is used to refer to single sections ICs.

MULTIBUS INTERFACE SECTION

Refer to Figure 1 for the following discussion of the Multibus Interface Section.

Timing Generator

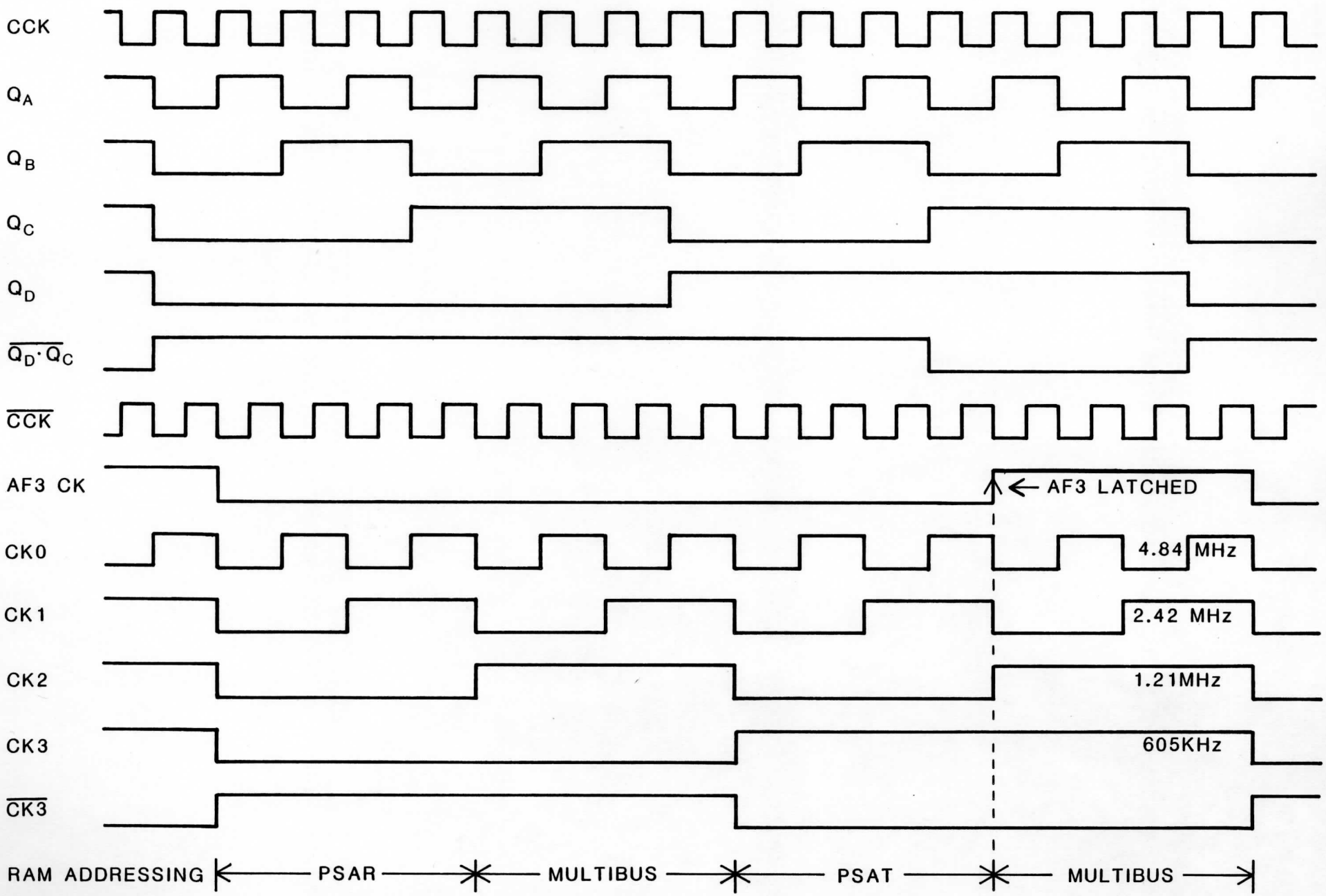
The Timing Generator is located at the bottom of sheet 5 on the schematic and consists of binary counter AF35, D-latch AD35, and inverters X35-E, -F, and X3-E. During the following discussion of the Timing Generator, refer to Timing Diagram 1.

The 9.68-Mhz SBC (Single Board Computer) clock (SBC CCLK) is buffered and inverted by each of the three inverters. The inverters produce both phases of the SBC CCLK clock and slightly delay the CCK signal applied to AF35 and AD35. CCK transitions lead those in AD35 by a few nanoseconds, CCK/ leads CCK by a few nanoseconds and PRECCK leads CCK/ by a few nanoseconds. These "early" signals are required in the Receiver and Transmitter section's CRC circuits. The signals shift present stable data into a receiving device just before the sending device is clocked by a delayed version of the same signal.

CCK is counted down by four-stage binary counter AF35. The four outputs from the counter are latched by octal latch AD35. AD35 resynchronizes all counter outputs to CCK and produces both phases of each input clock signal. However, CKØ/ and CK1 are not used.

Unit Select and Read/Write Controller

The Unit Select and Read/Write Controller is located on the lower half of sheet 2 of the schematic. The core of this block consists of six-bit comparators J26, J35, and L37. L37 is the memory address comparator while J26 and J35 are the I/O comparator. Edge Connector J2 is a programming (personality) connector on the Bisync board. For programming information on this connector, refer to SSEC drawing #35Ø4-ØØ5 (sheets 4 and 5 of 12), located in the Bisync Supplemental Data Section, immediately



TIMING DIAGRAM 1. TIMING GENERATOR WAVEFORMS

(6450-0085)

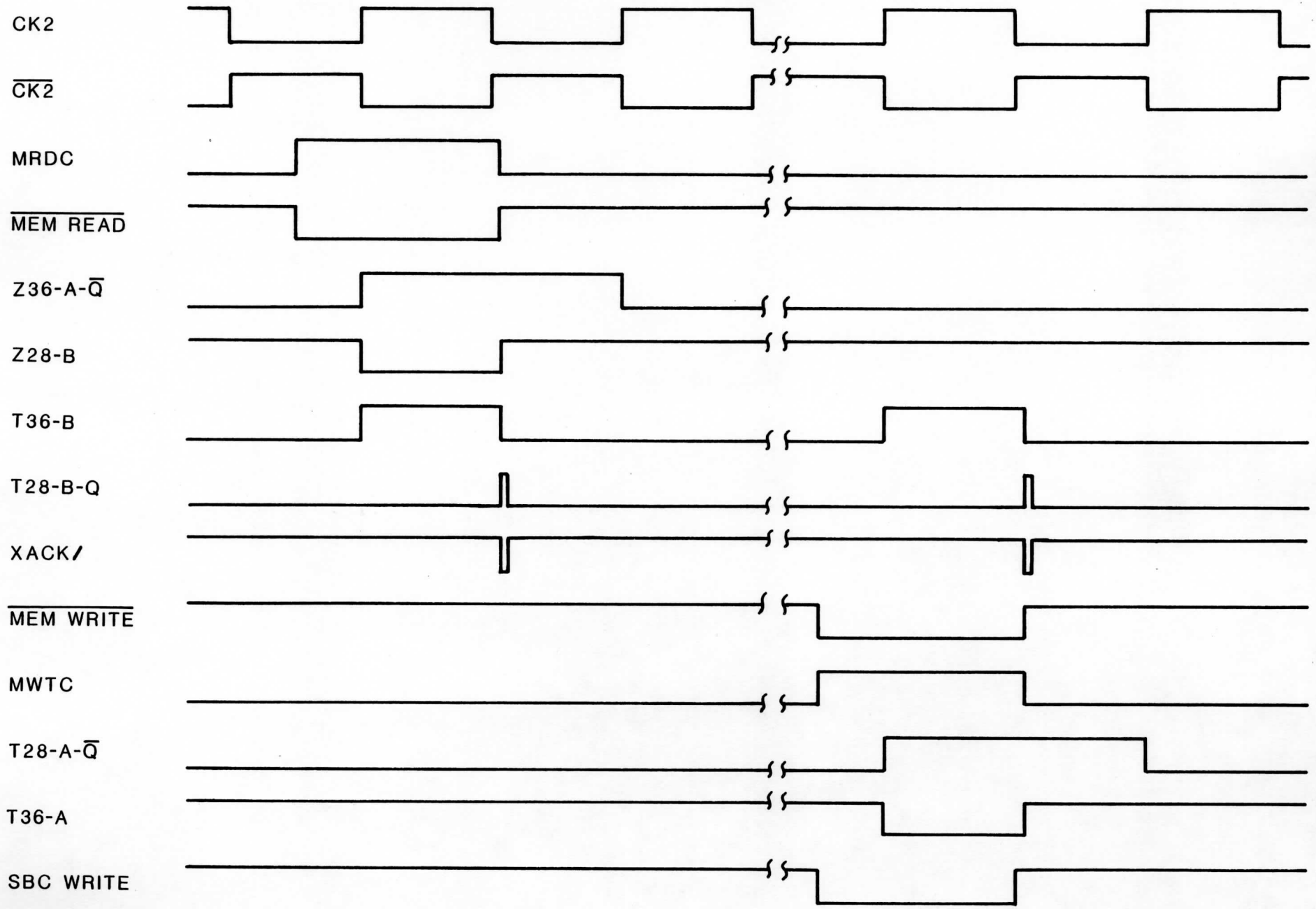
following the Detailed Circuit Description. As shown in 35Ø4-ØØ5, J2-9, -10, -11, -12, -13, -14, -15, -18, -20, and -21 are grounded while J2-16, -17, and -19 are connected to VCC.

The open collector outputs of J26 and J35 are tied together to pull up resistor AD27, so the two comparators must produce a match simultaneously to produce a logic high input to NAND gates R29-A and -B. With J2 connected as previously described, a Multibus address of 77XXH (port address 77H) is required to produce the logic high (the address lines are inverted). NAND gate R29-A combines the match signal with IORC to produce I/O READ/ while NAND gate R29-B combines the match with IOWC to produce I/O WRITE/. Thus, any time a port read or write to port 77H is performed, NAND gate R29-A or R29-B respectively goes active low.

L37 compares the upper five address lines from the Multibus address bus with the address programmed on J2. With the connector programmed as shown in 35Ø4-ØØ5 sheet 4, addresses of FØØØH-F7FFH (2Ø48 decimal addresses) produce a match. NAND gates R29-C and -D function like R29-A and -B to produce MEM READ/ and MEM WRITE/ respectively.

D-latches T28-A and Z36-A synchronize the MEM WRITE/ and MEM READ/ commands respectively with the rising edge of CK2 (refer to Timing Diagram 2). This qualifies NAND gate T36-A or Z28-B on the first rising edge of CK2 following a MEM WRITE/ or MEM READ/ command. Gate T36-B combines both of these signals to produce an active high at the input to D-latch T28-B for either a MEM READ/ or MEM WRITE/ command. T28-B is clocked by CK2/ and, if qualified, generates an active high output in synchronism with the falling edge of CK2. The output of T28-B is combined with the output of T36-C (I/O READ + I/O WRITE) to produce an active low input to the XACK/ generator (N3-E) for any valid I/O or memory command to this board. As soon as the microprocessor recognizes the XACK/ signal, initiated by T28-B or T36-C, it removes the memory or I/O read or write command from the Multibus, thereby placing a logic "zero" at the output of T36-B, asynchronously clearing T28-B.

Two outputs from the memory read/write circuitry other than the XACK/ input are SBC WRITE and a tri-state control for L26. The tri-state control for L26, the Status Buffer, is discussed in the next paragraph. Because the D-latch, T28-B, has a low output at all times except during a XACK/ time (see Timing Diagram 2), the pin 12 input to R21-D normally is



TIMING DIAGRAM 2. UNIT SELECT AND MULTIBUS READ/WRITE CONTROLLER

(6450-0085)

qualified. Since the other input to R21-D is MEM WRITE/, R21-D has a low output which begins with the falling edge of MEM WRITE/ and ends with the rising edge of the output from T28-B. This period always begins on or before the beginning of a Multibus timing cycle and extends to the end of that cycle. SBC WRITE is routed through the multiplexers (on sheet 1), where it is effectively gated by the negative portion of CK2/, thereby limiting it exactly to the Multibus timing cycle period. For more information on SBC WRITE, refer to the Memory Data Multiplexer Section.

Status Buffer

The Status Buffer, shown at the top center of sheet 2, is inverting tri-state octal buffer J4. The buffer output connects directly to the Multibus data bus; the tri-state control is driven by the I/O READ/ command. Thus, an I/O read to port 77H connects the five active J4 inputs to the Multibus data bus. Each of the five inputs, PSAT DONE, PSAR RESET, VLDMSG, PSATA1Ø, and PSARA1Ø, is covered in the section where that signal is generated.

Control Register

The Control Register consists of D-latches N28-A and -B, and N36-A and -B. The D inputs of these latches are connected directly to Multibus DATØ/ - DAT3/ and are clocked by I/O WRITE/. Thus, an I/O write to port 77H causes the Multibus data bus, bits DATØ/ - DAT3/, to be latched into N36-B and -A, and N28-B and -A respectively. The function of each latched output is covered in the section where it is used.

Miscellaneous Multibus Interface Circuits

The Multibus initialization signal, INIT/ (see sheet 5), is buffered by X35-A and routed to sheets 2 and 4 as CARD INIT. In turn, CARD INIT is applied to inverter X35-B, whose output (CARD INIT/) is routed to the Receiver and Transmitter State Machines (sheets 3 and 4), and to J2-28. J2-28 loops this signal back into J2-26 where it is routed, as A1Ø INIT, to the Status Registor (sheet 2). A1Ø INIT/ presets N28-A and clears N28-B. CARD INIT is used (on sheet 2) to preset both sections of N36. Thus (on sheet 2) A1Ø INIT and CARD INIT set the Control Register to default values on a power-up condition. CARD INIT and CARD INIT/ (on

sheet 4) initialize the PSAT and PSAT State Machine respectively. CARD INIT/ (on sheet 3) initializes the PSAR State Machine.

MEMORY SECTION

The Memory Section consists of the following: Memory block, Memory Data Multiplexer, Memory Address Multiplexer, Receiver Address Generator and Transmitter Address Generator. The Memory Section is shown on sheet 1 of the schematic diagram.

Memory

The Memory block is shown on sheet 1 and consists of four 1K (1Ø24) by 4-bit static RAM memory chips, A4, C4, E4, and G4. All address lines on all four chips are driven in parallel, as is the WE/ (Write Enable) line (pin 10). Note that CS/ (Chip Select) of A4 and C4 are connected to each other and to the input of inverter N3-D. The output of this inverter drives the CS/ pins on E4 and G4. Thus, when A4 and C4 are enabled (selected), E4 and G4 are not selected. When E4 and G4 are enabled, A4 and C4 are not selected. The data input/output pins of the two memory chip pairs are cascaded. Therefore, A4 and C4 function as a 1K by 8-bit static RAM, as do E4 and G4.

Receiver Address Generator

The Receiver Address Generator, shown on sheet 1, consists of three cascaded presettable binary four-stage counters, A14, A25, and A34. The load control (pin 9) is driven by PSAR GOING. This signal is low except during reception of a message. When the signal is low, the counter is preset to a count of CØØH. However, because only the 1Ø least significant outputs are used, the address output is ØØØ. The counters are clocked by CK3/ from the Timing Generator and are enabled by PSAR WRITE. PSAR WRITE is generated by the PSAR State Machine each time a new character is written into the receiver buffer memory. The counter increments each time a character is written into it. If the counter reaches a full count of 1Ø24 characters, (this should not happen), the ripple carry output of the most significant stage goes active high and is used as an overflow input to the PSAR State Machine.

Transmitter Address Generator

The Transmitter Address Generator is identical to the Receiver Address Generator. Refer to the preceding paragraph.

Memory Address Multiplexer

The Memory Address Multiplexer, shown on sheet 1, consists of multiplexer chips C14, C25, C34, E14, E25, and E34. Each chip is a four-section 2-to-1 multiplexer. The "A" or "B" inputs are selected by the "S" control signal. When "S" is low, the "A" inputs are coupled to the inverting "Y" outputs. When "S" is high, the "B" inputs are coupled to the inverting "Y" outputs.

The Receiver Address Generator outputs are connected to the "A" inputs of a multiplexer chip set consisting of C14, C25, and C34 while the outputs of the Transmitter Address Generator are applied to the "B" inputs. CK3 drives the "S" input of the multiplexers, so therefore, when "S" is low, the "Y" output of the multiplexer is driven by the Receiver Address Generator output. When "S" is high, the "Y" output is driven by the Transmitter Address Generator.

The "Y" output from the first multiplexer chip set is applied to the B input of a second multiplexer set consisting of E14, E25, and E34. The "A" input of this multiplexer is driven by Multibus Address lines ADRØ/ - ADRA/ and the"S" input is driven by CK2/. Timing Diagram 1 shows the resultant timing phases for the Memory Address Multiplexer.

Memory Data Multiplexer

An internal data bus (MEM Ø - MEM 7) connects the buffer memory to all data sources and sinks. The portion of the Memory Data Multiplexer that connects the internal data bus to the Multibus is bidirectional because messages must be both read from and written to the buffers. The portions of the Memory Data Multiplexer which connect the Receiver section and the Transmitter section to the internal data bus are unidirectional; the Receiver needs only to write received data to the memory and the Transmitter needs only to read the data about to be transmitted.

The bidirectional Multibus-to-internal-data-bus multiplexer, shown on sheet 2 of the schematic, consists of D-latch L13 and inverting buffers

J15 and L26. The Multibus data write portion of the Memory Data Multiplexer is J15. Because the tri-state control of J15 is driven by WRITE NANDed with CK2, the signal WRITE is discussed here.

The signal WRITE is generated by N2Ø (on sheet 1) and is made up from SBC WRITE and PSAR WRITE. SBC WRITE is the Multibus memory write command, shown on sheet 2. PSAR WRITE is the receiver write signal, generated by the PSAR State Machine each time a character is to be written into the buffer memory. Both of these signals pass through the Memory Address Multiplexer (refer to sheet 1 of the schematic) and arrive at NAND gate N12-A. N12-A produces an active low output during the positive portion of the CK1/ signal if pin 2 is active high (Write command).

Refer to Timing Diagram 3 for the generation of WRITE caused by the signal, SBC WRITE. The signal SBC WRITE is asynchronous and can occur at any time. Because SBC WRITE is multiplexed, it is present at the input of N12-A only during the Multibus time window. Therefore, if it goes active high during a current Multibus time window, it must occur before the first rising edge of CKØ if it is to be gated through N12-A and latched by N2Ø-A. Otherwise, it must wait for the next Multibus time window.

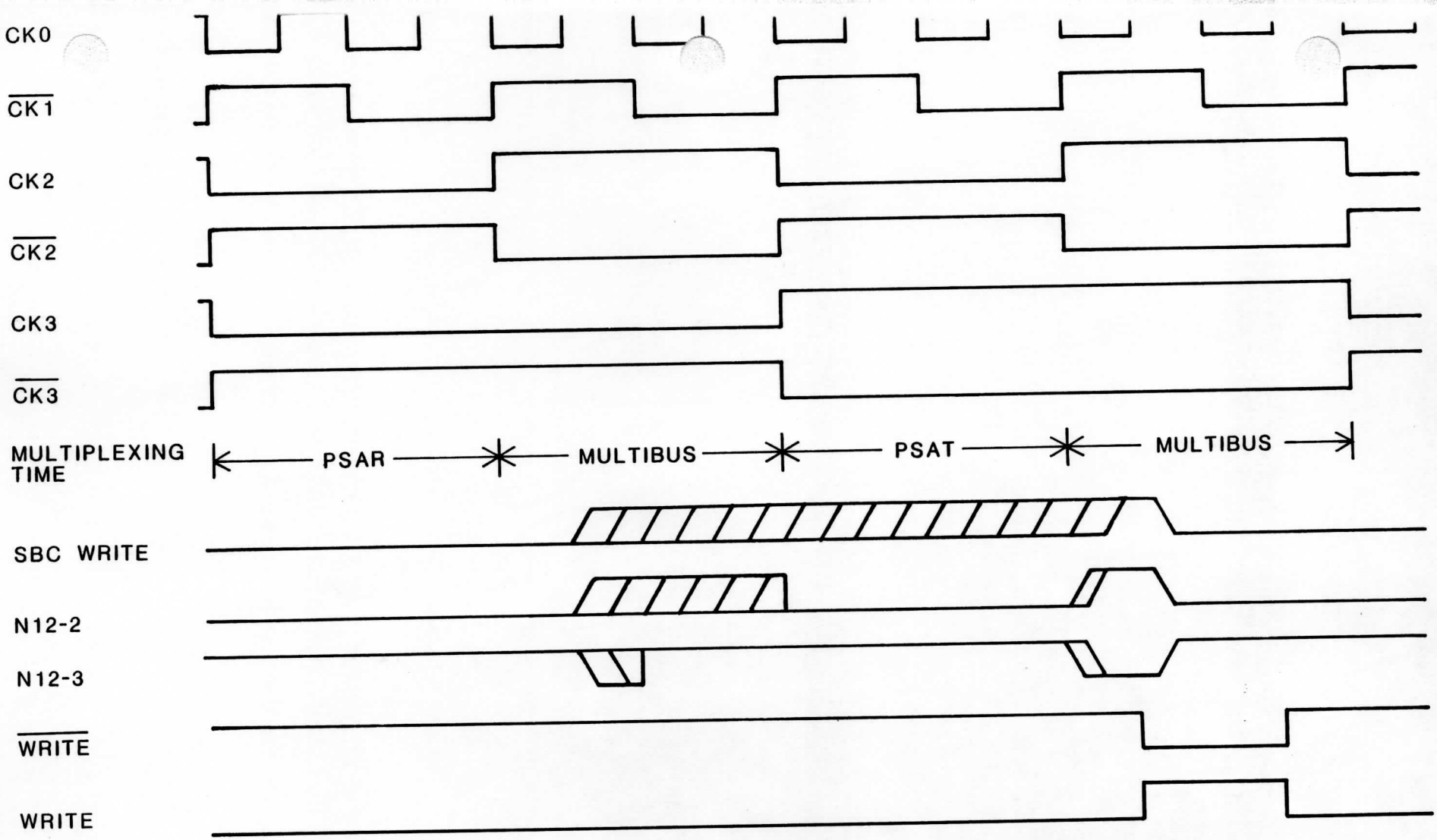
J15 places Multibus "write data" onto the internal data bus when NAND gate T36-D goes active low. CK2 limits the duration of the WRITE command to the Multibus time window.

PSAR WRITE is generated by the PSAR State Machine, in synchronism with CK3. In fact, PSAR WRITE is always equal in time to a full CK3 cycle. The generation of PSAR WRITE is further explained in the Receiver Section. Timing Diagram 4 shows the WRITE signal generation when it is caused by PSAR WRITE.

Note that, regardless of which command generates the signal WRITE, it always occurs in the middle of the corresponding multiplexing time window. This ensures that the data is stable before the WRITE command is active.

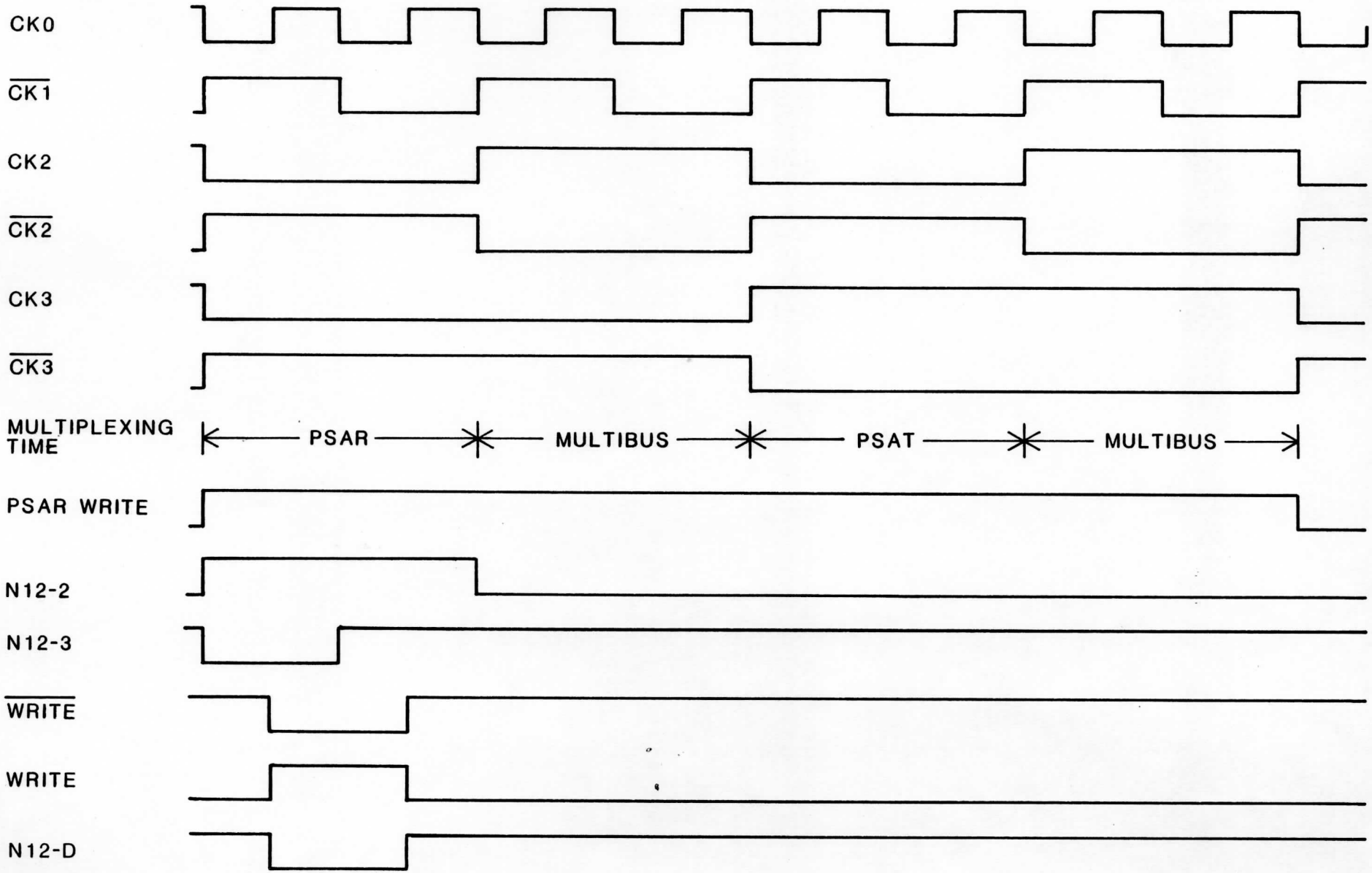
The Multibus data read multiplexer consists of D-latch L13 and tri-state buffer L26. The rising edge of CK2/ latches buffer memory "read data" into L13 at the end of each Multibus time window. Tri-state buffer L26 dumps the output of L13 onto the Multibus when a MEM READ/ command is processed.

The Receiver section to internal data bus multiplexer is shown on sheet 3 and consists of non-inverting buffer L2. (Refer to Timing Diagram



TIMING DIAGRAM 3. MULTIBUS MEMORY WRITE TIMING

(6450-0085)



TIMING DIAGRAM 4. PSAR MEMORY WRITE TIMING
(6450-0085)

4.) NAND gate A26-C is qualified active low only during a PSAR time window and then only if the PSAR has requested a Write cycle.

The Transmitter section of the internal data bus multiplexer is shown on sheet 4 and consists of octal latch AF3, D-latch AP14-B, and NAND gates AM38-A, Z28-A, and N12-D. Q_C and Q_D are outputs from the Timing Generator (see sheet 5 and Timing Diagram 1). NAND gates Z28-A and N12-D, together, function as an AND gate which ANDs Q_C and Q_D. AP14-B is clocked by CCK, therefore has a rising (clocking) edge in synchronism with the end of the PSAT time window. AF3, then, is latched near the end of the PSAT time window. NAND gate AM38-A controls the tri-state output of AF3. Q_M and Q_X, the inputs to NAND gate AM38-A, are latched outputs from the PSAT State Machine. The output of AF3 is in a state of high impedance if the state machine is in a state of C, D, E, or F (see Figure 2). For more information on the state machine, see the Transmitter sub-section of the Detailed Circuit Description.

TRANSMITTER SECTION

The Transmitter section is shown on sheet 4 of the schematic diagram.

PSAT

C1, the PSAT, is the heart of the Transmitter. The PSAT is a 40-pin chip designed to convert the 5-, 6-, 7-, or 8-bit parallel input characters into a serial output data stream. Complete PSAT information is located in the Bisync Supplemental Data Section, immediately following the Detailed Circuit Description.

As shown in the schematic, the PSAT is always enabled (CD tied to ground); it is programmed for synchronous transmission (MS1 tied to ground and MS2 tied to VDC), and it does not transmit parity (PI is tied to VCC). In addition, the PSAT is programmed for eight-bit operation (WLS1 and WLS2 are tied to VCC) and the transmit clock output (TCO) equals the data bit rate (CS1 and CS2 tied to ground).

The PSAT is gated on by the "Clear to Send" (CTS) RS-232 handshake signal. When CTS goes high, the PSAT transfers a character from the Transmitter Holding Register (THR) to the Transmit Register (or from the Fill Character Register if no character is in the THR). The Transmit Register is simply a parallel load shift register, shifted by the transmit

clock. When a character is transferred from the THR, the "Transmitter Holding Register Empty" (THRE) line goes true. THRE causes external circuitry to retrieve the next character and load it into the PSAT THR, by strobing the Transmitter Holding Register Load (THRL) line low. The transmission process continues until the CTS line goes inactive low.

With the exception of AF3 (part of the Memory Data Multiplexer), all circuitry on sheet 4 is used to control the PSAT or generate a CRC check sum.

PSAT State Machine

The PSAT State Machine primarily consists of PROM AM1Ø, D-latch AM21, and D-latch AP3-B. The following additional components are required for state decoding: 3-to-8 line decoder AK25, D-latch AH2Ø, NAND gate AM38-C, NAND gate AM38-D, and quad input NOR gate X11-B.

PROM AM1 and OR gate T2Ø-C convert the seven-bit ASCII input code into forms the State Machine can accept. PSAT Ø - PSAT 7, the Transmitter Section internal data bus, is connected to the eight LSB address inputs of AM1, the Character Attribute PROM. This PROM maps each ASCII character into one of the following five categories:

- SOP (Start of Packet)
- EOP (End of Packet)
- EOM (End of Message)
- EOX (End of Transmission - Do not send check word)
- Data Bytes

These categories are used by the State Machine for state sequencing control.

The hexadecimal ASCII code to PROM output mapping is as follows:

ASCII (HEX VALUE) INPUT	PROM OUT	CATEGORY
ØØ	Ø	DATA
Ø1	4	SOP
Ø2	4	SOP
Ø3	3	EOM
Ø4-1E	Ø	DATA
1F	2	EOP
2Ø-25	Ø	DATA
26	3	EOM
27-3C	Ø	DATA
3D	1	EOX
3E-7F	Ø	DATA

Although more than one ASCII code generates an SOP or EOM character, the McIDAS workstation-to-host protocol does not use all codes for each category. However, if a different host requires, for example, an ASCII Ø1 as an SOP character, the PROM does not have to be replaced.

The three-bit output from PROM AM1 is applied to the D4-D6 inputs of D-latch AP3-B. Note that PROM output bit Ø is first ORed with PSAT END OF COUNT before being applied to AP3-B. PSAT END OF COUNT goes active high if the transmit buffer memory becomes exhausted (incremented to its maximum count of 1Ø23 words); this does not happen under normal conditions. This causes the State Machine to reset to its initial state for processing data and SOP characters during State 8 or 9, or an EOP during State 8. The D7 input to AP3-B is THRE ANDed with the Q output of AF19-B. An active high THRE signals that the THR is empty and can accept a new character.

Momentarily, let us turn our attention to AF19 (top right of sheet 4). Both the A and B sections of AF19 are preset to a logic high, at their Q outputs, by the control signal PSAT GO/. After the microprocessor loads a transmit message into the PSAT half of the memory, a PSAT GO/ command is issued by writing a data byte with a logic zero LSB to port 77H (refer to the Control Register Detailed Circuit Description). When AF19-B is preset, AND gate AH31-A can pass THRE flags to AP3-B. Also, PSAT RESET is an inactive low and is the Request To Send (RTS) signal (see sheet 5). When the host (if it is not busy) receives the RTS, it responds by bringing CTS (Clear To Send) high. The CTS is an input to the PSAT (pin 17) and allows the transmitter to generate its first THRE signal. THRE now passes to AP3-B where it is latched on the next rising edge of CK3 (the A portion of AP3 is used for the corresponding latch in the PSAR State Machine shown on sheet 3).

The status of the State Machine is defined by the hexidecimal code output of D-latch AM21 (See Figure 2). Since CK3 clocks D-latch AM21 after each subsequent rising edge of CK3, the PROM output becomes the four MSB address inputs to itself; the output of AP3-B becomes the four LSBs. Three-to-eight line decoder AK25 uses the D3 output of PROM AM1Ø as an enable input. If D3 is high, AK25 is enabled and PROM outputs DØ-D2 are decoded to one of eight lines dependent on the three data input lines (pins 1, 2 and 3). The selected active low output (providing AM1O-D3 is

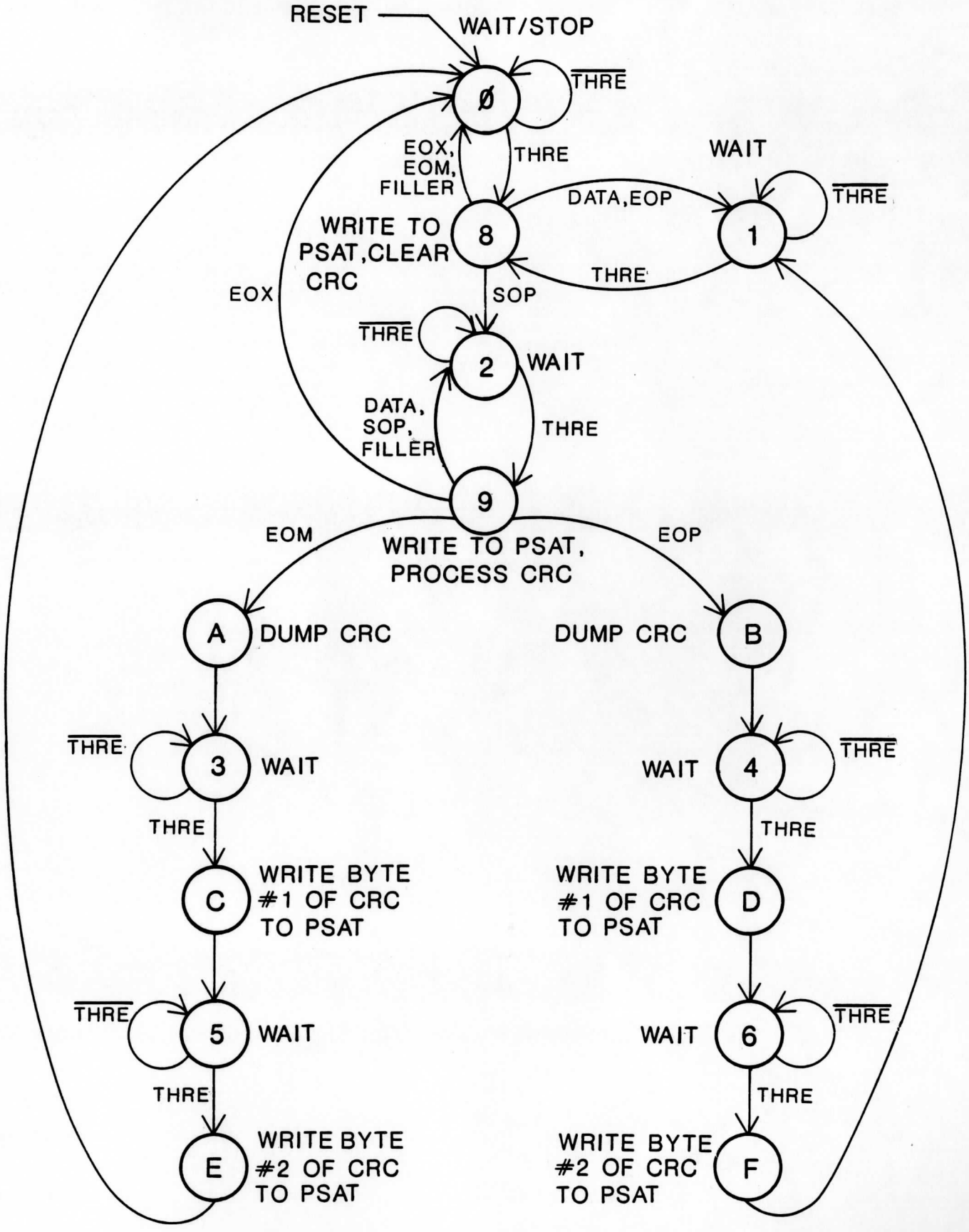


FIGURE 2. BISYNCRONOUS TRANSMITTER STATE DIAGRAM (6450-0085)

high) and the seven non-selected high outputs are latched in AH2Ø on the next rising edge of CK3/, producing one of the active low state outputs STATE 8/ through STATE F/. If AM1Ø-D3 is low, none of the outputs from AH20 are active. NOR gate X11-B produces a high output when all PROM (AM1Ø) outputs are low. AM21 latches the NOR gate output and produces STATE Ø (active high). Latch AM21 also latches the output of NAND gate AM38-C, which yields an active low latch output during STATE A/ or STATE B/ times. This latch output is CHECK WORD ENABLE/.

CRC Generator

The CRC Generator, located on the lower center of sheet 4, consists of eight-bit shift register AK34, CRC generator AM3Ø, serial-to-parallel converters AK3 and AK14, D-latches AP14-A, AP14-C, AP14-D, and AP14-E, AND gates AH31-B, AH31-C, and AH31-D, OR gate T2Ø-D, NAND gate T12-A, and inverter AH1-D.

Shift register AK34 has its parallel inputs connected to the transmitter's internal data bus. AK34 latches the parallel input data on the next rising edge of CCK if its shift/load pin (pin 15) is low. During a message transmission, AK34 remains mostly in the load state. Only during the last half of PSAT STATE 9/ does OR gate T2Ø-D produce an active low output. At this same time, PSAT STATE A/ and PSAT STATE B/ are high, producing a high output from NAND gate T12-A. The high output from T12-A is latched by AP14-A on the next rising edge of CCK. This condition remains until the output of OR gate T2Ø-D returns to a high state. The period of PSAT STATE 9/ is 16 CCK cycles in duration and the low half of CK3 is eight CCK cycles, so AP14-A has a high output for exactly eight CCK cycles. The AK34 is clocked by CCK and is in the shift mode for eight CCK clock periods. Eight shift pulses are processed by AK34 during PSAT STATE 9/, shifting its entire contents out of pin 13 and over to the CRC generator chip AM3Ø. The PSAT STATE A/ and PSAT STATE B/ inputs to T12-A are discussed in the next paragraphs.

AM3Ø performs the CRC generation on the serial data entering pin 11. The chip is negative-edge-clocked by the clock applied to pin 1. CCK/, via AND gate AH31-D, clocks AM3Ø. Since the falling edge of CCK/ clocks AM3Ø and the rising edge of CCK/ clocks AK34, the date is clocked out of AM3Ø and into AK34 by the same clock. Even under worst case conditions,

the falling clock edge at AM3Ø pin 1 is at least two nanoseconds ahead of data transitions at the output of the shift register, clocked by the positive going clock at AK34 pin 7. Thus, AM3Ø meets the zero nanosecond data hold time requirement.

AM3Ø is in a check word generation mode or in a data output shift mode, as a function of the logic level at pin 1Ø (CWE). When pin 1Ø is high, check word is generated. When pin 1Ø is low, the 16-bit check word is shifted out of pin 12 (Q) by the clock applied to pin 1. Because the check word is 16 bits long, 16 clock pulses must be gated through AND gate AH31-D. D-latch AP14-A has a high output for the entire PSAT STATE A/ or PSAT STATE B/ time (16 CCK/ clock periods), due to the high output from T12-A. CHECK WORD ENABLE/, an output from the State Machine, is active low during PSAT STATE A/ or PSAT STATE B/ times, thereby placing AM3Ø in the data output shift mode at the same time the 16 clock pulses are gated to pin 1. AM3Ø pins 3, 5, and 8 (polynomial select pins) all are grounded by the "Personality Connector" (J2) and select the CRC-16 polynomial.

AK3 and AK14 are cascaded serial-to-parallel converters. The serial output of AK3 is connected to the serial input of AK14. Thus, after 16 bits have been shifted out of AM3Ø and into AK3 and AK14, AK14 will contain the eight LSBs while AK3 contains the eight MSBs. The serial-to-parallel converters operate in one of the following four modes: shift right, shift left, parallel load and hold. $S_Ø$ and S_1 (pins 1 and 19) are mode controls. Because S_1 is grounded, only the shift right and hold modes are available. When $S_Ø$ is high, the chips shift the data one bit to the right on each rising edge of the input clock (PRECCK). When $S_Ø$ is low, the chips retain their present data regardless of the clock input. G1/ and G2/ (pins 2 and 3) are tri-state output controls. When both tri-state pins are low, the chip dumps its output onto the transmitter internal data bus. With the tri-state inputs high, the chip outputs are "floating" (high impedance). Note that PSAT STATE C/ and PSAT STATE D/ cause AK14 to dump the least significant character onto the bus, while PSAT STATE E/ and PSAT STATE F/ do the same with the most significant character (refer to Figure 2, the Transmitter Bisynchronous State Diagram). After a character is dumped onto the bus, the PSAT LOAD/ control is brought low, loading the character into the transmitter. For more information on PSAT LOAD/, refer to the next two paragraphs.

The remaining circuitry on sheet 4 deals with PSAT COUNTER BUMP and PSAT LOAD/ command generation (refer to Figure 2 as necessary). The PSAT COUNTER BUMP, located at the bottom center of sheet 4, consists of D-latch AF27-A and NAND gate AM38-B. The chip is clocked by the rising edge of CK2 and cleared by the logic low portion of CK3 (refer to Timing Diagram 3). Thus, it is latched at the beginning of the Multibus time window and cleared at the end of it. NAND gate AM38-B provides a logic high input to AF27-A during PSAT STATE 8/ and PSAT STATE 9/ only, the two states in which data is read from the PSAT buffer.

The PSAT LOAD/ generator is identical to the PSAT COUNTER BUMP generator except the NAND gate is replaced with a three-input AND gate (X19-C) and produces an active high input to AP14-A for PSAT states 8, 9, C, D, E, and F. Again, states 8 and 9 are data loading states while states C, D, E, and F are CRC loading states.

RECEIVER SECTION

The Receiver Section is shown on sheet 3 of the schematic diagram.

PSAR

Z1, the Programmable Synchronous and Asynchronous Receiver (PSAR), is the core of the Receiver Section. The PSAR is a 40-pin chip that converts the serial input data stream into 5-, 6-, 7-, or 8-bit parallel characters. Complete PSAR information is located in the Bisync Supplemental Data Section, immediately following the Detailed Circuit Description.

RR_1 - RR_9 (pins 15-7 respectively) constitute the Receiver Holding Register (RHR). RR_9, the ninth bit, is a parity bit output and is not used. Serial input data enters the chip on pin 35 (RI). The receiver clock (64 times the baud rate) is applied to pin 31 (RRC). A match character is required for synchronous operation since there are no start and stop bits. MHR_1 - MHR_8 (pins 18, 22, 17, 36, 3, 38, 4, and 40 respectively) constitute the match register. In the McIDAS communications scheme, 32H is the hexadecimal code of the match character. It is programmed into MHR_1 - MHR_8 by tying appropriate inputs to VCC or ground. RMS_1 - RMS_3, the mode select pins and part of the control register, are tied to VCC via the J2 personality connector, thereby programming the chip for synchronous communication.

Only the following four pins, not yet described, are important in the understanding of receiver operation and its interface with the remaining blocks in the Receiver section:

- DR (Data Ready - pin 26)
- DRR (Data Ready Reset - pin 25)
- MR (Master Reset - pin 32)
- CD (Chip Disable - pin 6).

The chip is programmed for eight-bit characters and even parity via the two word-length select pins (WLS_1 and WLS_2) and the even-parity enable pin (EPE).

The CD pin must be active low before the PSAR can receive data. When this pin is high, it places the RHR in a state of high impedance, thereby disconnecting it from the Receiver Section internal data bus (PSAR Ø - PSAR 1Ø).

Two match characters are used at the beginning of each message. Internally, the PSAR shifts the last eight received data bits each time a new data bit is received. The oldest bit shifts out and is discarded as the newest bit shifts in. While this happens, the parallel outputs of the internal shift register are compared with the Match Character Holding Register. When a match occurs, the MDET (Match Detect - pin 3Ø) pin goes high. In the McIDAS, this pin is not used and there is no other external evidence of a match. However, the next match character is now treated as data and causes the DR pin to go active high when the second sync character is completed and transferred to the RHR.

After the DR flag is set, it must be reset by bringing DRR active low, prior to completion of the next character. Failure to read a character and reset the DR flag (DRR goes active low) causes loss of a data character.

The DR flag is an input to the PSAR State Machine and indicates that the PSAR has a character in the RHR. The State Machine produces the memory storage cycles necessary to load the character into the buffer memory before generating an active low input to the DRR pin.

PSAR State Machine

The PSAR State Machine is nearly identical to the PSAT State Machine. Refer to Figure 3, the Bisynchronous Receiver State Diagram and the PSAT State Machine Detailed Circuit Description as necessary.

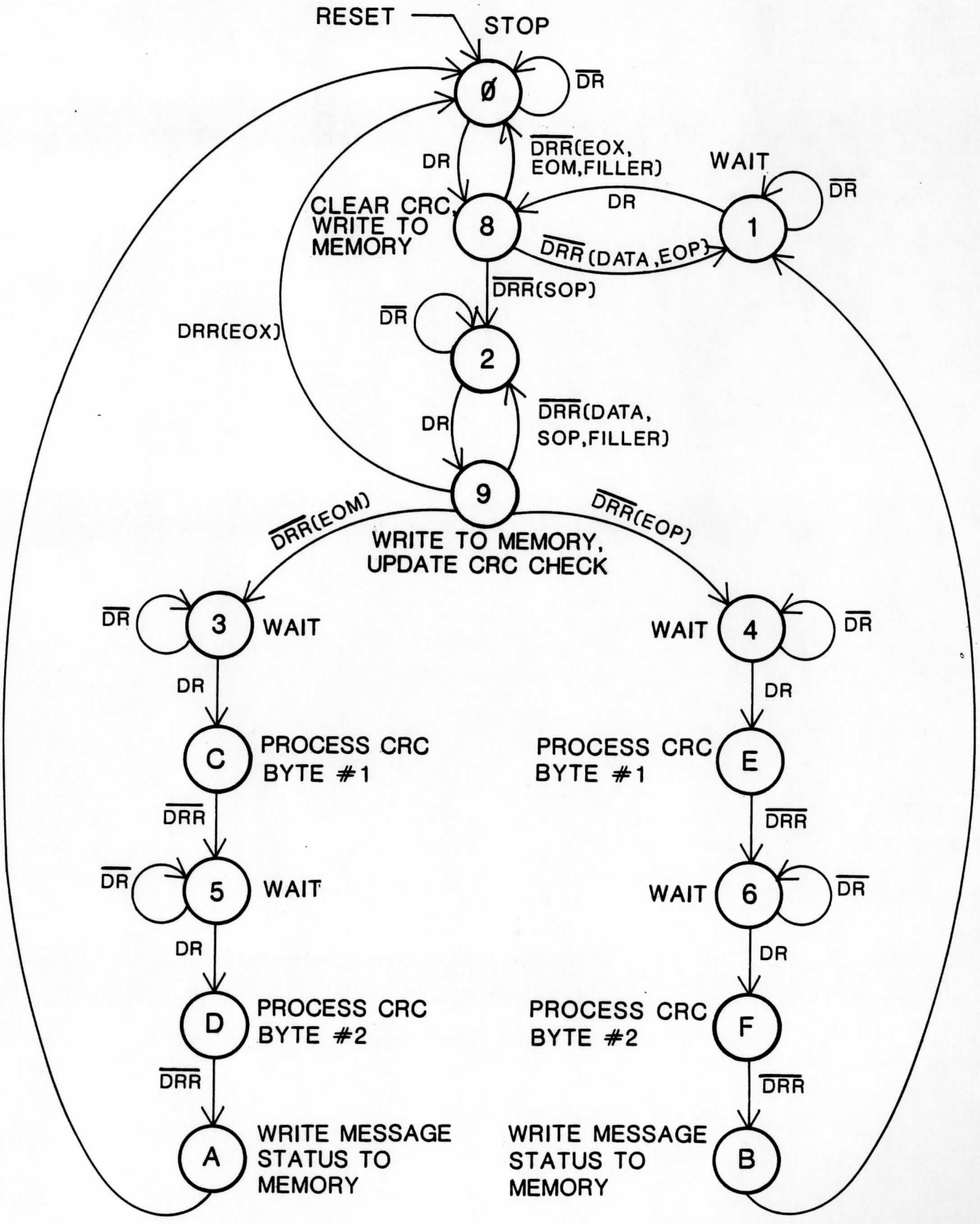


FIGURE 3. BISYNCHRONOUS RECEIVER STATE DIAGRAM (6450-0085)

While R_1 has the same mapping code as AM1 in the Transmitter Section, it can output one additional code that the Transmitter counterpart never outputs. That code, Ø6, is generated if a filler character is received (FF_H). Otherwise, the mapping described for AM1 is valid for R1.

During a power-up condition, CARD INIT/ goes active low, resetting the State Machine to state Ø by clearing V_1 and V_{12} and clearing N2Ø-B. This brings PSAR RESET active high. The active high PSAR RESET is applied to the MR (Master Reset) input of the PSAR, resetting it to its idle state. PSAR RESET is also applied to the Status Buffer. Upon detection of PSAR RESET, the microprocessor issues a PSAR GO/ command. This command removes the master reset from the PSAR, presets N36-A (PSAR GOING active high on schematic sheet 2) and provides a Data Terminal Ready (DTR) command input to the RS-232 Interface Section (for those installations which require a DTR signal). After N36-A is preset, it removes the preset signal from N20-B, completing the PSAR reset cycle. At the end of each message, the State Machine enters State Ø. The rising leading edge of state Ø clocks N2Ø-B and forces another master reset of the PSAR. Therefore, after receiving a message, the PSAR is reset and must be cleared by the microprocessor, as explained above. This prevents the host from writing a second message before the microprocessor has read the current message. After the master reset has cleared, the receiver begins hunting for a match character.

Only three state outputs from D-latch V1 are used. The first, PSAR STATE 8/, resets the CRC Checker (X27) just as PSAT STATE 8/ does in the Transmitter Section. The others, PSAR STATE A/ and PSAR STATE B/ are multiplexer controls and are explained in the CRC Checker Section.

D-latch V12 latches PSAR STATE Ø, explained above. It also latches the CRC Checker clock gate (V12 pin 15) and the inputs to a PSAR WRITE command generator (X19-A). NAND gates T12-B and -C, and OR gate T2Ø-B combine states 9, C, D, E, and F to produce an active high input to the D6 input of V12 during those states. The latched Q6 output of V12 is applied to AND gate X19-B, along with CK3 and CCK (see Timing Diagram 1). Since each of the above states is one CK3 timing cycle in duration, X19-B gates eight CCK clock pulses during each state. For more information, refer to the CRC Checker Detailed Circuit Description. PSAR WRITE, the output of AND gate X19-A, is active high when V12-Q_4 is active high and V12-Q_3 is low. Thus, PSAR WRITE is active high for states 8, 9, A, and B.

CRC Checker

The CRC Checker circuit is nearly identical to the CRC Generator in the Transmitter Section. The major differences are no serial-to-parallel converters in the CRC Checker, the CRC Checker CWE pin is tied high, and instead of using the serial check sum output, as is done in the generator, the Error (ER) output is used. This output is a logic low after the last bit of the second CRC character has been clocked into X27, if there are no errors. Eight shift pulses are provided for states 8 and 9 (data states), and states C, D, E, and F (CRC States).

The ER output from X27 is applied to all inputs of D-latch V23 and to the D input of latch Z36-B. NAND gate N12-B produces a logic low output for all states except PSAR STATE A/ and PSAR STATE B/. The logic low output from N12-B puts the RHR in the PSAR in an active state (reads the internal data bus PSAR 1 - PSAR 7) and places a logic high at the tri-state control pin on V23. When N12-B goes low, the RHR goes to a high impedance and V23 goes active, placing a logic low or high on all internal data bus lines, indicating a valid or invalid message respectively. At the end of PSAR STATE A/ or PSAR STATE B/, Z36-B is clocked, latching the message status signal, VLDMSG.

RS-232 INTERFACE

The RS-232 Interface is shown on sheet 5 of the schematic.

Transmit Clock Generator

The Transmit Clock Generator produces 12 standard J2 selectable baud-rate clock signals for use in installations with no modem transmit clock. The generator consists of crystal oscillator AB38 (1.2288 Mhz) and baud-rate generator AB29.

AB29 is a 12-stage binary counter in which all stage outputs are externally available for use as a baud rate clock.

RS-232 Interface

PSAT output data (TRO, see sheet 4) is buffered by inverting buffers AH1-A and AH1-B before it is applied to inverting line driver AB24-A. At the host end of the system, this data is "receive" data. The host's transmitted data enters the McIDAS workstation as Received Data on pin

J3-3. This data is buffered by inverting line receiver AH9-A and applied to pin 35 of the PSAR (sheet 3).

PSAT RESET is the Q/ output of AF19-A (on sheet 4). When a PSAT GO command is received, AF19-A is preset, thereby producing a logic zero on PSAT RESET. PSAT RESET (on sheet 5) is applied to inverting line driver AB24-B, producing an active high Request to Send (RTS) output signal to the host. If the host is ready to receive data, this signal causes a Clear to Send (CTS) signal to be transmitted back to the workstation. The RTS and CTS are the request and acknowledge handshake signals required to complete the workstation's transmit channel. The CTS signal enters the workstation at J3-9 and is applied to buffers AH9-B and AH1-C before being applied to pin 17 on the PSAT (see sheet 4). Note that PSAT RESET and CTS are applied to NAND gate AP23-D, whose output is inverted by NAND gate AP25-C to produce the signal PSAT DONE. PSAT RESET and CTS are both low during a data transmission. PSAT DONE does not go high until PSAT RESET goes high (transmission complete) and the host acknowledges this fact by dropping the CTS in response (CTS is high). PSAT DONE is a status input to the Status Buffer.

When the host needs to transmit a message, it must use handshake signals. The host initiates a request for transmission by bringing Data Set Ready (DSR) high. In the McIDAS workstation, the Receiver Section is always ready to receive data because a separate buffer is provided for the receiver. Therefore, in most installations, the DSR signal is looped back to the host via line receiver AP31-A, NAND gate AP23-A, NAND gate AP13-B (pin 5 is normally connected to a pull up via J2-32), and line driver AH41-A. If, occasionally, the microprocessor cannot unload the receiver buffer before another input message begins, J2-32 can be connected to J2-3Ø (PSAR GOING) in place of the pull up.

Frequently, the workstation is connected to the host by a modem. The workstation's modem normally produces a transmit clock which enters the workstation on J3-4 as MTC (Modem Transmit Clock). The signal is applied to inverting line receiver AH9-C and re-inverted by buffer AH1-F. It is then routed to J2-38, normally connected to J2-5Ø (FAKE SOURCE). The FAKE SOURCE signal (also called TRC - Transmit Clock) is connected to pin 5 (CLK) of the PSAT. After shifting the data out of the transmitter, the clock is looped back out of the PSAT on pin 11 (TCO). On sheet 5, TCO is

applied to inverting buffer AH1-E and applied to inverting line driver AF14-A. The output of AF14-A is routed off-board via J3-22 and is the RS-232 transmit clock output.

The received data clock enters the board via J3-8 (ROC) and is applied to inverting line receiver AH9-D and NAND gate Z28-D (functions as an inverter). The output of Z28-D (RRC) is applied to pin 31 of the PSAR (Receiver Register Clock - RRC).

BISYNC SUPPLEMENTAL DATA SECTION

WESTERN DIGITAL
CORPORATION

PT1482 (PSAT)
Programmable Synchronous & Asynchronous Transmitter

FEATURES

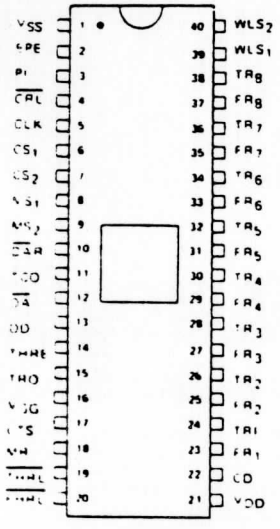
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC, 1X CLOCK PT1482-01
- DC TO 100K BITS/SEC, 1X CLOCK PT1482-00
- PROGRAMMABLE MATCH (FILL) CHARACTER
- SELECTABLE 5,6,7, OR 8 BIT PER CHARACTER
- EVEN/ODD PARITY GENERATOR, PARITY INHIBIT
- PROGRAMMABLE CLOCK RATE 1X, 16X, 32X, OR 64X.
- AUTOMATIC START & STOP BIT GENERATION IN ASYNCHRONOUS & ISOCHRONOUS MODES
- PROGRAMMABLE 1 AND 2 STOP BITS, (1½ IN 5 LEVEL MODE)
- AUTOMATIC CHARACTER STATUS AND DELIMITING SIGNAL GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE COMPATIBILITY
- DOUBLE BUFFERED
- TTL AND DTL COMPATIBLE — INTERNAL ACTIVE PULL UP
- COMPATIBLE RECEIVER, PR1472.

GENERAL DESCRIPTION

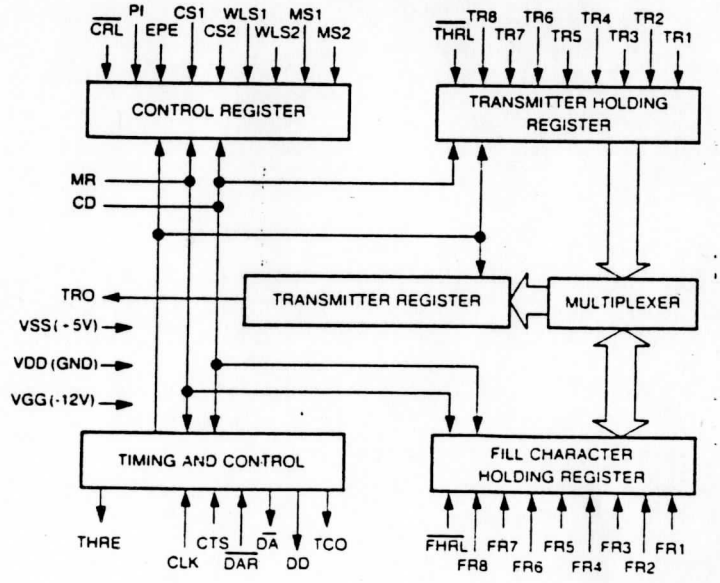
The Western Digital PT1482 (PSAT) is a programmable transmitter that interfaces variable length parallel data to a serial data channel. The transmitter converts parallel characters into a serial data stream with a format compatible with all standard Synchronous, Asynchronous or Isoschronous data communications media.

Contiguous serial characters are transmitted in the Synchronous Mode with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data. Programming the Asynchronous Mode selects serial transmission with automatic insertion of Start and Stop Bits. Isoschronous mode selects transmission with automatic fill character insertion during the absence of parallel input data. Four internal registers and a multiplexer, in conjunction with Three-State Output Lines, provide full system versatility.

The PSAT is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a compatible Receiver, PR1472.



PIN CONNECTIONS



PT1482 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+ 5 Volt Supply
2	EVEN PARITY ENABLE	EPE	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the EPE and PI Inputs.
3	PARITY INHIBIT	PI	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be generated by the Transmitter. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable.
			PI / EPE / SELECTED PARITY / COMMENTS V_{IL} / V_{IL} / ODD / CD = V_{IL} V_{IL} / V_{IH} / EVEN / CD = V_{IL} V_{IH} / X / NONE / CD = V_{IL}
			NOTE: IF CD = V_{IH}, NO PROGRAMMING IS PERFORMED SINCE INPUTS ARE DISABLED.
			X – either V_{IL} or V_{IH} When programmed, the appropriate parity is generated following, and is contiguous with, the last data bit of a character, immediately preceding the stop element of asychronous and isochronous characters.
			A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.
4	$\overline{CONTROL\ REGISTER\ LOAD}$	$\overline{CRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{CRL}$ input.
			A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Control Register and loads it with Control Bits (EPE, PI, CS_1, CS_2, MS_1, MS_2, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD, disables $\overline{CRL}$.
5	TRANSMITTER REGISTER CLOCK	TRC	This is a fifty (50) percent duty cycle clock. The positive going edge of this Clock shifts data out of the Transmitter Register at a rate determined by the Control Bits CS_1 and CS_2, and provides the basic time reference for all device functions.
6-7	CLOCK RATE SELECT	CS_1-CS_2	A low-level input voltage, V_{IL}, applied to CD enables the CS_1 and CS_2 inputs. These two lines select the internal clock rate divider ratio to produce the transmitter bit rate defined by the Truth Table below:
			CS_2 / CS_1 / SELECTED CLOCK INPUT RATE V_{IL} / V_{IL} / 1X BIT RATE V_{IL} / V_{IH} / 16X BIT RATE V_{IH} / V_{IL} / 32X BIT RATE V_{IH} / V_{IH} / 64X BIT RATE

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
8-9	MODE SELECT	MS_1-MS_2	A high-level input voltage, V_{IH}, applied to CD disables CS_1 and CS_2. These lines may be strobed or hard-wired to the appropriate input voltage. A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the MS_1 and MS_2 inputs. These lines select the transmitter operating mode. **MS_2 MS_1 MODE** V_{IL} V_{IL} ASYNCHRONOUS — ONE STOP BIT V_{IL}* V_{IH}* ASYNCHRONOUS — TWO STOP BITS V_{IH} V_{IL} SYNCHRONOUS V_{IH} V_{IH} ISOCHRONOUS *Selects 1.5 stop bits for 5-level codes. A high-level input voltage, V_{IH}, applied to CD disables MS_1 and MS_2.
10	$\overline{\text{DATA NOT AVAILABLE}}$ $\overline{\text{RESET}}$	$\overline{\text{DAR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DAR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the Data Not Available Flag. A high-level Input, V_{IH}, applied to CD disables $\overline{\text{DAR}}$. This input is not used during asynchronous operation.
11	TRANSMITTER CLOCK OUTPUT	TCO	This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive going edge corresponds to the start of each data bit transmission. All waveforms in this specification are referenced to TCO.
12	$\overline{\text{DATA NOT AVAILABLE}}$ FLAG	$\overline{\text{DA}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DA}}$ input. A high-level output voltage, V_{OH}, on this line indicates that a Fill-Character has been transmitted, since a character was not loaded into the Transmitter Holding Register by the center of the last bit of a Synchronous Character or the center of the Stop Element of an Isochronous character. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{DA}}$. This input is not used during asynchronous operation.
13	DATA DELIMIT/ END OF CHARACTER	DD/EOC	During asynchronous operation, a high-level output voltage, V_{OH}, indicates data is being transmitted. A low-level output voltage, V_{OL}, indicates that a Start or Stop Element is being transmitted. A low-level output voltage during synchronous operation indicates that the last bit of a character is being transmitted.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
14	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A low-level input voltage applied to CD (pin 22) enables the THRE input. A high-level output voltage, V_{OH}, on this line indicates the Transmitter Holding Register is empty and has transferred its contents to the Transmitter Register and may be loaded with a new character. This line goes to a low-level output voltage, V_{OL}, when THRL goes to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables THRE.
15	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the Transmitter Holding Register are serially shifted out as an NRZ waveform on this line provided that a character was loaded into the Transmitter Holding Register prior to $\overline{DA}$ Flag (in Synchronous or Isochronous Modes). If a character was not loaded prior to a $\overline{DA}$ Flag, the contents of the Fill-Character Register are transmitted as the next character.
16	V_{GG} POWER SUPPLY	V_{GG}	– 12 Volts Supply.
17	CLEAR-TO-SEND	CTS	The Clear-To-Send Control initiates or disables transmission as a function of the state of this line. A high-level input voltage, V_{IH}, initiates serial data transmission provided a character has been loaded into the Transmitter Holding Register. A low-level input voltage, V_{IL}, applied to this line during transmission allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.
18	MASTER RESET	MR	The rising edge of a high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets THRE, the contents of the Fill-Character Holding Register, and TRO to a high-level output voltage, V_{OH}.
19	$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{THRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Transmitter Holding Register and loads it with the Transmitter Holding Register data and forces THRE to a low-level output voltage, V_{OL}. A high-level input voltage, V_{IH}, applied to this line disables the Transmitter Holding Register. A high-level input voltage, V_{IH}, applied to CD disables $\overline{THRL}$.
20	$\overline{\text{FILL-CHARACTER HOLDING REGISTER LOAD}}$	$\overline{FHRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{FHRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Fill-Character Holding Register and loads it with the Fill-Character Register data FR_1-FR_8. A high-level input voltage. V_{IH}, applied to this line disables the $\overline{FHRL}$ Register. This line may be strobed or hard-wired to a low-

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			level input voltage, V_{IL}. This input is not used during asynchronous operation. A high-level input voltage, V_{IH}, applied to CD disables $\overline{FHRL}$.
21	V_{DD} POWER SUPPLY	V_{DD}	Ground.
22	CHIP DISABLE	CD	This line controls the disconnect associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line removes drive from push-pull outputs causing them to float. Drivers of disabled inputs are required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **INPUT LINES** / **TRI-STATE OUTPUT LINES** $\overline{CRL}$, $\overline{THRL}$ / $\overline{DA}$ EPE, $\overline{FHRL}$ / THRE PI, FR_1-FR_8 CS_1-CS_2, TR_1-TR_8 $\overline{MS_1}$-MS_2, WLS_1, WLS_2 $\overline{DAR}$
23, 25 27, 29 31, 33 35, 37	FILL-CHARACTER HOLDING REGISTER DATA INPUTS	FR_1-FR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Fill-Character Holding Register and associated Load Strobe, $\overline{FHRL}$. Parallel 8-bit characters are input into the Fill-Character Holding Register with the $\overline{FHRL}$ Strobe (pin 20). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2) only the least significant bits are accepted. These lines may be strobed or hard-wired to the appropriate input voltage. These inputs are not used during asynchronous operation. During Synchronous or Isochronous transmission, the Fill-Character is transmitted if a character was not loaded into the Transmitter Holding Register prior to a $\overline{DA}$ Flag; i.e., the Transmitter Holding Register did not contain a character at the center of the last bit being transmitted from the Transmitter Register. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted, Least Significant Bit (FR_1) to Most Significant Bit (FR_n) order. A high-level input voltage, V_{IH}, applied to CD disables FR_1-FR_8.
24, 26 28, 30 32, 34 36, 38	TRANSMITTER HOLDING REGISTER DATA INPUTS	TR_1-TR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs to the Transmitter Holding Register and associated Load Strobe, $\overline{THRL}$. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. A high-level input

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
39-40	WORD LENGTH	WLS_1-WLS_2	voltage, V_{IH}, will cause a high-level output voltage to be transmitted, Least Significant Bit (TR_1) to Most Significant Bit (TR_n) order. A high-level input voltage, V_{IH}, applied to CD disables TR_1-TR_8. A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Control Register and Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below: WLS_2 / WLS_1 / SELECTED WORD LENGTH V_{IL} / V_{IL} / 5 BITS V_{IL} / V_{IH} / 6 BITS V_{IH} / V_{IL} / 7 BITS V_{IH} / V_{IH} / 8 BITS A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2, forcing them to float.

ORGANIZATION

PT1482 block diagram is illustrated on page 1.

Control Register — Programming of the PSAT is accomplished by loading the 8 Bit Control Register. Mode selection, clock divisor, word length, and parity are selected when the Control Register Load signal is activated.

Transmitter Register — The Transmitter Register is used to store the outgoing data stream. The contents of this register are derived from either the Transmitter Holding Register or the Fill (Match) Character Holding Register with the Control and Timing Logic automatically adding the required start and stop bits during Asynchronous and Isoschronous Modes.

Transmitter Holding Register — The Transmitter Holding Register, a buffer register, is used to store the parallel character to be serially transmitted.

Fill Character Holding Register — The Fill Character Holding Register is used to store the Fill (Match) Character which is transmitted during the absence of characters in the Transmitter Holding Register.

Timing and Control — The Timing and Control Logic generates the required control signals to transmit Data and Fill Characters. Character transmission status signals are also derived from this logic.

SYNCHRONOUS MODE OPERATION

Synchronous transmission requires that characters (programmably variable from 5 to 8 data bits plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiuous does not imply that the system servicing the transmitter always has ample time to load the Transmitter Holding Register, it is necessary that a character be transmitted when data has not been loaded into the Transmitter Holding Register. This character is defined as the Fill or Idle Character and a separate register has been provided to load this character upon initialization. The Fill-Character Holding Register is loaded by strobing the Fill-Character Holding Register Load ($\overline{FHRL}$) line or hard-wiring it to a low-level input voltage.

Referring the Block Diagram of the Transmitter, it can be seen that the Chip Disable (CD) enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register. Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{CRL}$, $\overline{THRL}$, and $\overline{FHRL}$ are under CD control. In addition, the Transmitter Holding Register Empty (THRE) Flag, Data Not Available ($\overline{DA}$) Flag, and the Data Not Available Reset ($\overline{DAR}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. The P/SAT will enter a defined "idle" state when the Master Reset (MR) is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Flag is set to a high-level output voltage, the Data Delimit/End of Character (DD/EOC) Flag

is set to a low-level output voltage, and the contents of the Fill-Character Holding Register are forced to a high-level output voltage.

When the P/SAT is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage, defines the mode of operation, character length, selected parity if required, and the clock rate selection. Table 1 illustrates all the programmable synchronous character formats.

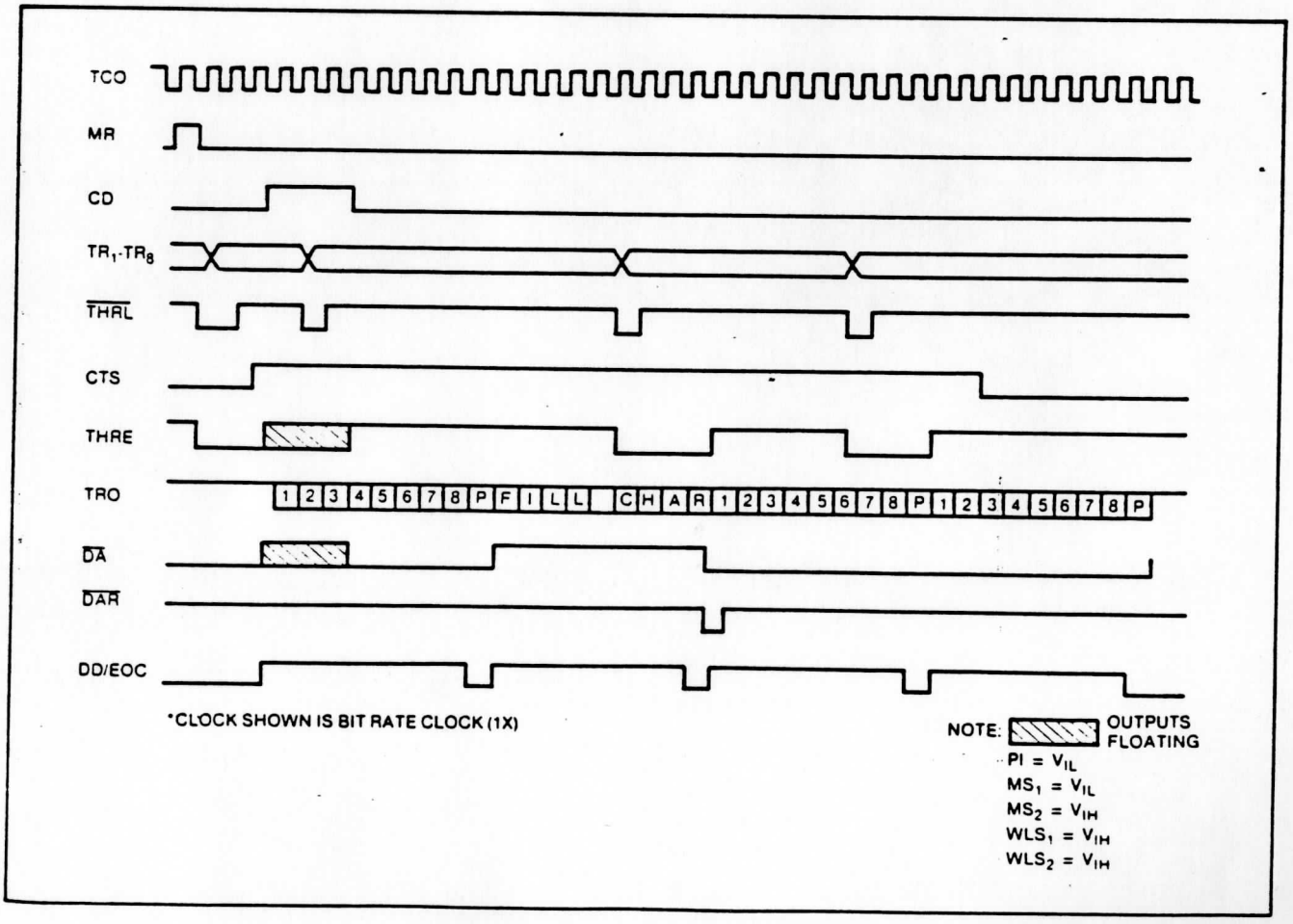
To initialize transmission the CTS signal must be set to a high state and the transmitter holding register must be loaded with a character to be transmitted. The transmitter will remain in an idle state until this is accomplished.

The character transferred into the Transmitter Register (from the Transmitter Holding Register or the Fill-Character Holding Register) is determined at the center of the last bit of the character being transmitted. If, at this time, no character has been loaded into the Transmitter Holding Register, the Fill-Character is loaded into the Transmitter Register at the end of the bit being transmitted

Table 1. SYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT	
MSS2	MSS1	WLS2	WLS1	PI	EPE	DATA BITS	ADDED PARITY BIT
1	0	0	0	0	0	5	ODD
1	0	0	0	0	1	5	EVEN
1	0	0	0	1	X	5	NONE
1	0	0	1	0	0	6	ODD
1	0	0	1	0	1	6	EVEN
1	0	0	1	1	X	6	NONE
1	0	1	0	0	0	7	ODD
1	0	1	0	0	1	7	EVEN
1	0	1	0	1	X	7	NONE
1	0	1	1	0	0	8	ODD
1	0	1	1	0	1	8	EVEN
1	0	1	1	1	X	8	NONE

↑ Sets to SYNC Mode



SYNCHRONOUS TIMING EXAMPLE

tion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register and the THRE flag will be set to a high-level output voltage.

The start bit, selected parity and stop bit(s), determined by the Control Register programming, are added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform.

A low-level input voltage, applied to CTS during transmission, allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. Data Delimit is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. Neither TRO, CTS nor DD/EOC is under control of Chip Disable.

ISOCHRONOUS MODE OPERATION

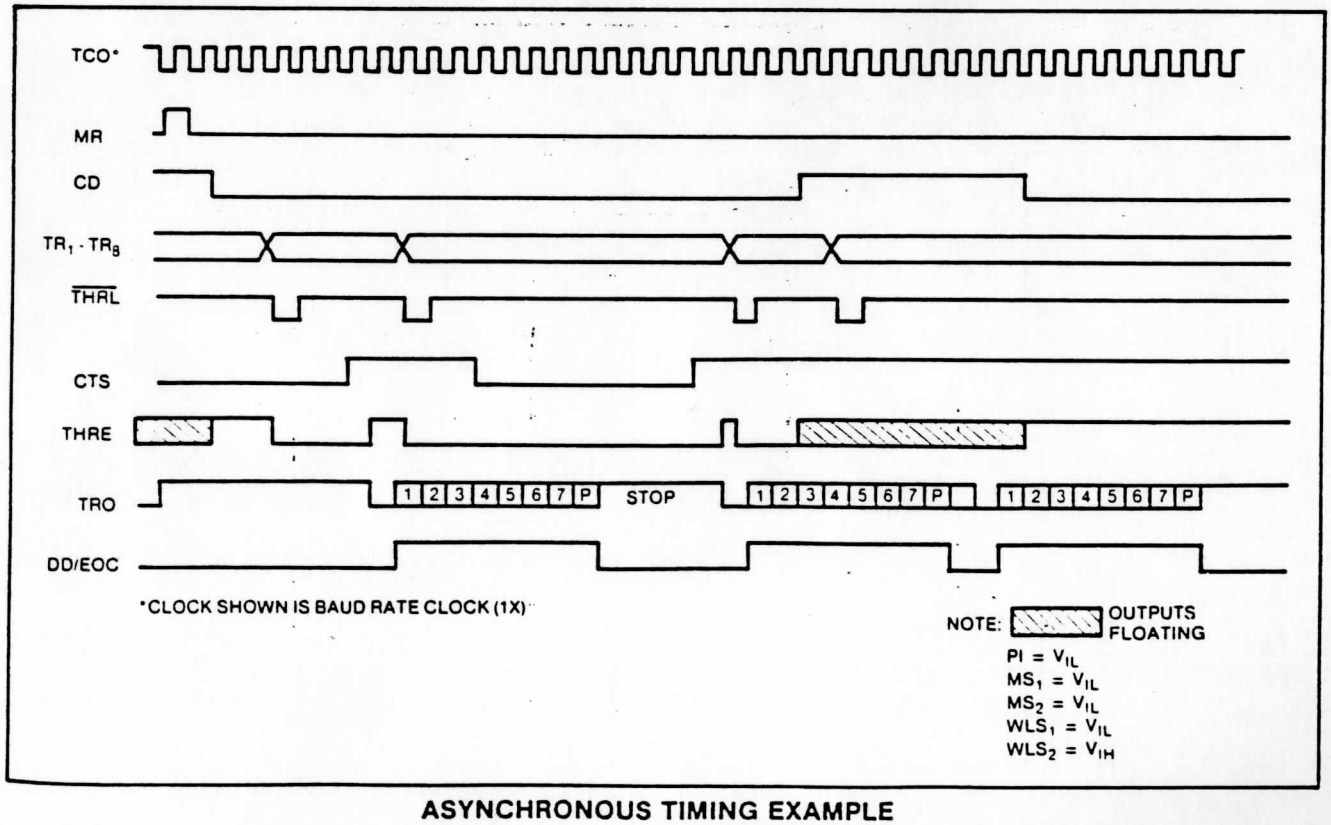
In the Isochronous Mode of operation all (Synchronous Mode) definitions apply with the exception of those for the Data Delimit/End of Character (DD/EOC) Flag and the Data Not Available Flag (DA).

This is the case since Isochronous Data Transmission requires contiguous characters with the addition of a start and a single stop bit added to each character.

Table 2. ASYNC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MS2	MS1	WLS2	WLS1	PI	PE		START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
0	0	0	0	0	0		1	5	ODD	1
0	1	0	0	0	0		1	5	ODD	1.5
0	0	0	0	0	1		1	5	EVEN	1
0	1	0	0	0	1		1	5	EVEN	1.5
0	0	0	0	1	X		1	5	NONE	1
0	1	0	0	1	X		1	5	NONE	1.5
0	0	0	1	0	0		1	6	ODD	1
0	1	0	1	0	0		1	6	ODD	2
0	0	0	1	0	1		1	6	EVEN	1
0	1	0	1	0	1		1	6	EVEN	2
0	0	0	1	1	X		1	6	NONE	1
0	1	0	1	1	X		1	6	NONE	2
0	0	1	0	0	0		1	7	ODD	1
0	1	1	0	0	0		1	7	ODD	2
0	0	1	0	0	1		1	7	EVEN	1
0	1	1	0	0	1		1	7	EVEN	2
0	0	1	0	1	X		1	7	NONE	1
0	1	1	0	1	X		1	7	NONE	2
0	0	1	1	0	0		1	8	ODD	1
0	1	1	1	0	0		1	8	ODD	2
0	0	1	1	0	1		1	8	EVEN	1
0	1	1	1	0	1		1	8	EVEN	2
0	0	1	1	1	X		1	8	NONE	1
0	1	1	1	1	X		1	8	NONE	2

↑ Sets to ASYNC Mode



ASYNCHRONOUS TIMING EXAMPLE

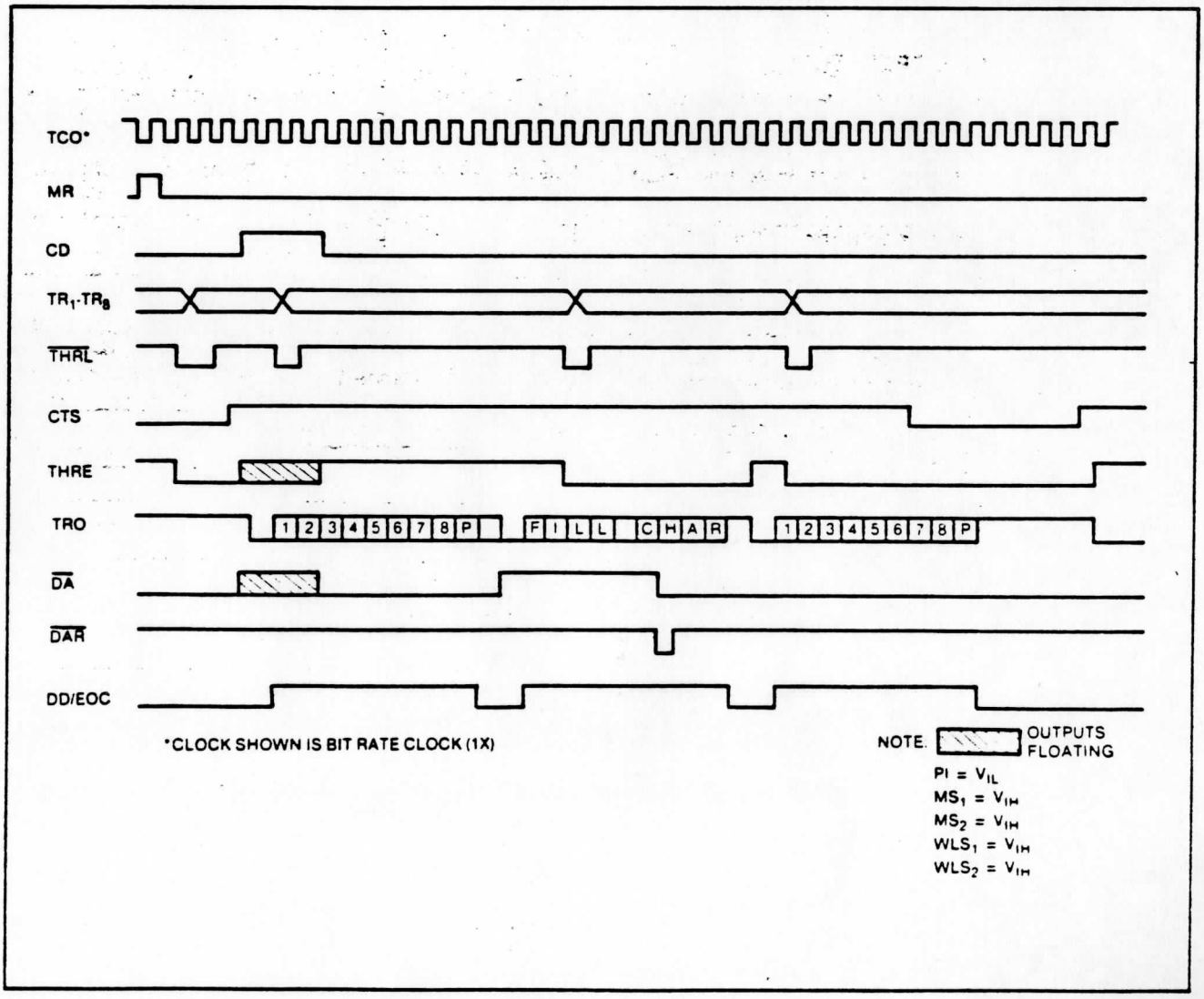
The Data Delimit/End of Character Flag is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. The Data Not Available Flag ($\overline{DA}$) is set to a high-level output voltage at the end of the stop bit if a character has not been loaded into the Transmitter Holding Register at the center of the stop bit. The contents of the Fill-Character Holding Register will be transferred into the Transmitter Register and repeatedly transmitted until a character is loaded into the Transmitter Holding Register. At this time, the Fill-Character will be completed and the newly loaded isochronous character will follow contiguously.

Table 3 illustrates all the programmable isochronous character formats.

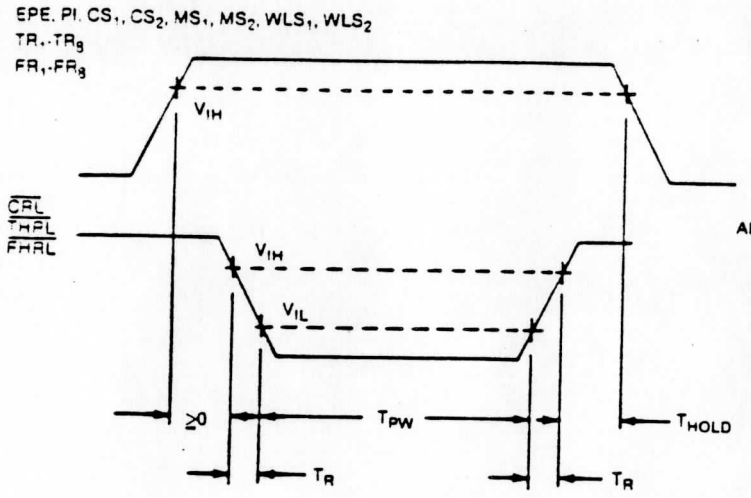
Table 3. ISOC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MSS2	MSS1	WLS2	WLS1	PI	EPE		START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
1	1	0	0	0	0		1	5	ODD	1
1	1	0	0	0	1		1	5	EVEN	1
1	1	0	0	1	X		1	5	NONE	1
1	1	0	1	0	0		1	6	ODD	1
1	1	0	1	0	1		1	6	EVEN	1
1	1	0	1	1	X		1	6	NONE	1
1	1	1	0	0	0		1	7	ODD	1
1	1	1	0	0	1		1	7	EVEN	1
1	1	1	0	1	X		1	7	NONE	1
1	1	1	1	0	0		1	8	ODD	1
1	1	1	1	0	1		1	8	EVEN	1
1	1	1	1	1	X		1	8	NONE	1

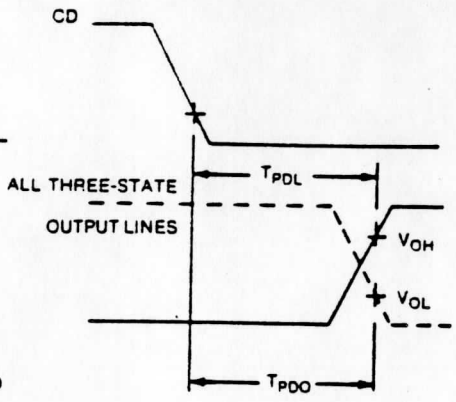
↑ Sets to ISOC Mode



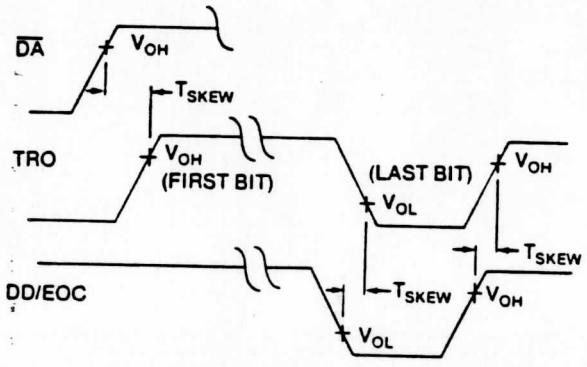
ISOCHRONOUS TIMING EXAMPLE



DATA INPUT LOAD CYCLE

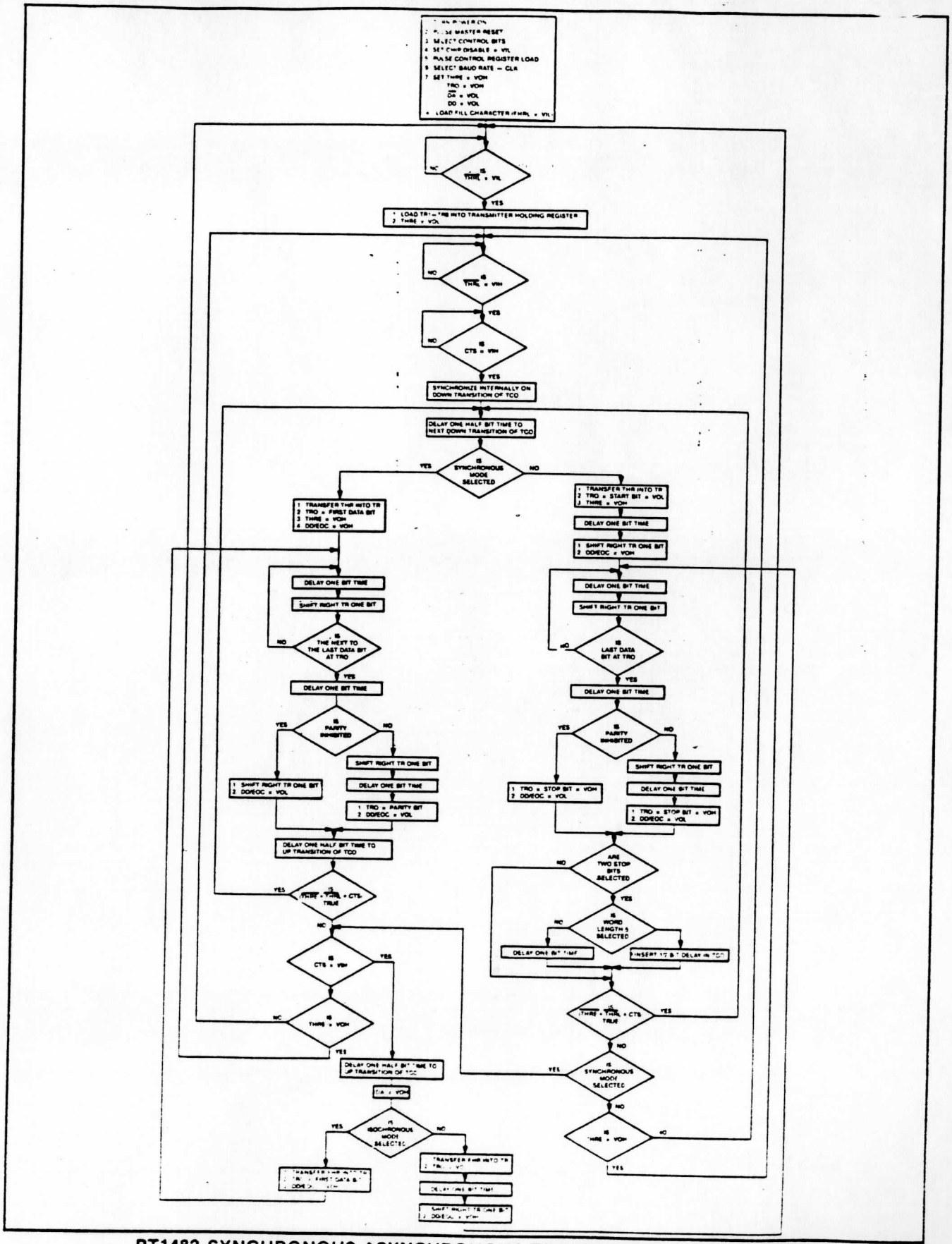


OUTPUT ENABLE DELAYS

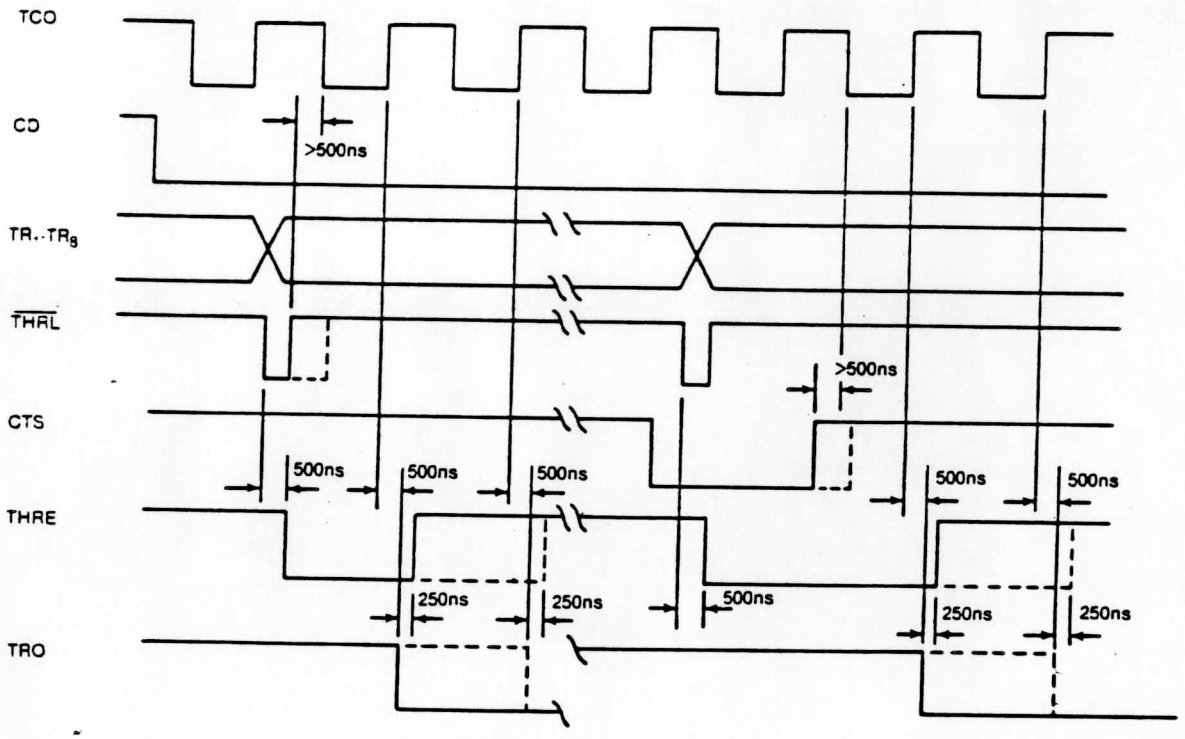


SKEW TIMES

SWITCHING WAVEFORMS



PT1482 SYNCHRONOUS ASYNCHRONOUS TRANSMITTER FLOW CHART



TIMING DETAIL

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage		+ 0.3V to − 20V
V_{DD} Supply Voltage		+ 0.3V to − 20V
Clock Input Voltage*		+ 0.3V to − 20V
Logic Input Voltage*		+ 0.3V to − 20V
Logic Output Voltage*		+ 0.3V to − 20V
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range		0°C to + 50°C
Lead Temperature (Soldering, 10 sec.)		300°C

*$V_{GG} = V_{DD} = 0V$

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+50°C$ unless otherwise specified)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
V_{IL} V_{IH}	**INPUT LOGIC LEVELS**[1] Low-level Input Voltage High-level Input Voltage	 V_{SS}-1.5V	0.8V	V_{SS} = 4.75V
V_{OL} V_{OH}	**OUTPUT LOGIC LEVELS**[2] Low-level Output Voltage High-level Output Voltage	 V_{SS}-1.0V	0.5V	V_{SS} = 5.25V I_{OL} = −1.6mA V_{SS} = 4.75V I_{OH} = −100μA
I_{IL}	**INPUT CURRENT —** Low-level Input Current (each input)		−1.6mA	V_{SS} = 5.25V V_{IN} = 0.4V
I_{LO}	Output Leakage Current[2]		10μA	

**Not more than one output should be shorted at a time.

NOTES: 1) Inputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically disabled and appear as a single TTL load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD) are logically and electrically disconnected and caused to float.

3) All switching characteristics are measured at 0.8V and 2.0V.

SWITCHING CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+50°C$, $C_L = 20pf$)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC DC	100 KHz 640 KHz	1482B-00 1482B-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
$T_{\overline{CRL}}$	Control Register Load	250 nsec		
$T_{\overline{THRL}}$	Transmitter Holding Register Load	250 nsec		
$T_{\overline{FHRL}}$	Fill-Character Holding RegisterLoad	250 nsec		
$T_{\overline{DAR}}$	Data Not Available Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay		500 nsec	
T_{SKEW}	Skew Time		250 nsec	
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	

See page 429 for ordering information.

WESTERN DIGITAL
CORPORATION

PR1472-01 Programmable Synchronous & Asynchronous Receiver(PSAR)

FEATURES

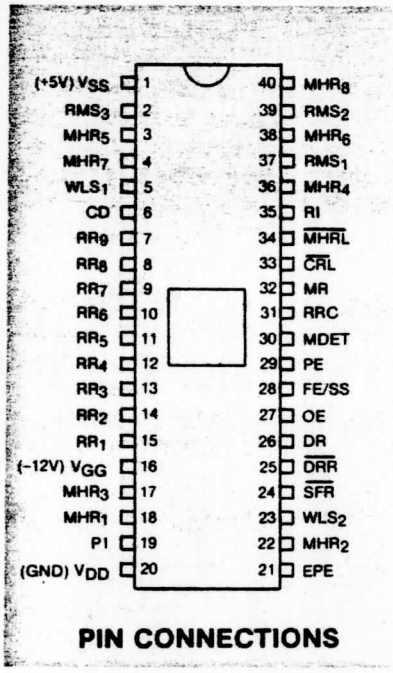
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC (1X CLOCK) PR1472-01; DC TO 100K BITS/SEC PR1472
- PROGRAMMABLE MATCH (FILL) CHARACTER WITH MATCH DETECT FLAG.
- INTERNAL OR EXTERNAL CHARACTER SYNCHRONIZATION
- NINE BIT WIDE RECEIVER HOLDING REGISTER
- SELECTABLE 5, 6, 7 OR 8 BITS PER CHARACTER
- EVEN/ODD OR NO PARITY SELECT
- PROGRAMMABLE CLOCK RATE; 1X, 16X, 32X OR 64X
- AUTOMATIC START AND STOP BIT STRIPPING
- AUTOMATIC CHARACTER STATUS AND FLAG GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE CAPABILITY
- DOUBLE BUFFERED
- TTL & DTL COMPATIBLE — INTERNAL ACTIVE PULLUP
- COMPATIBLE TRANSMITTER. PT1482

GENERAL DESCRIPTION

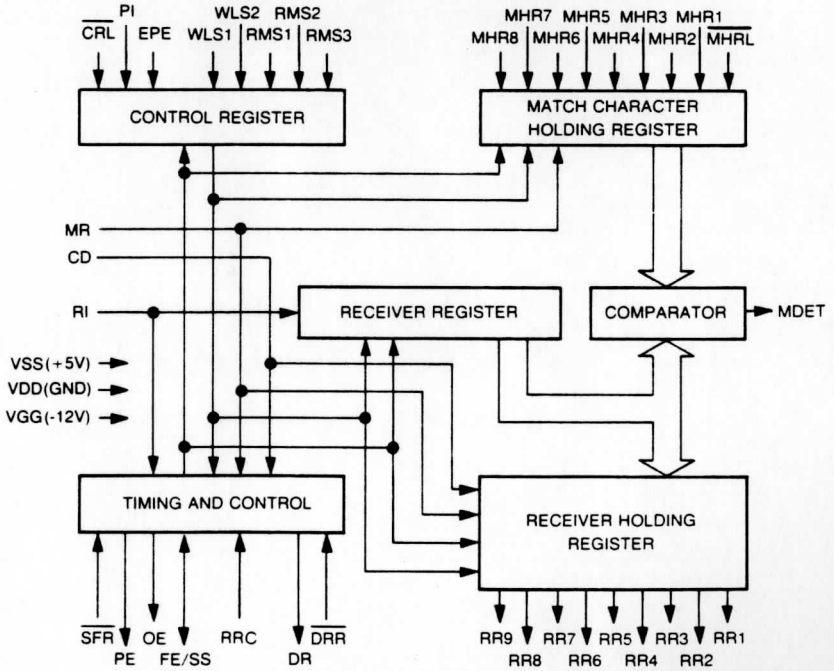
The Western Digital PR1472 (PSAR) is a programmable receiver that interfaces variable length serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard Synchronous, Asynchronous, or Isochronous data communications media.

Contiguous synchronous serial characters are compared to a programmable Match-Character Holding Register, character synchronized and assembled. Programming the Asynchronous or Isochronous Mode provides assembly of characters with start and stop bit(s) which are stripped from the data. Four internal registers, in conjunction with Three-State Outputs provide full system versatility.

The PSAR is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a Compatible Transmitter. PT1482.



PIN CONNECTIONS



PR1472 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+5 Volt Supply
37, 39, 2	RECEIVER MODE SELECT	RMS_1, RMS_2, RMS_3	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables RMS_1, RMS_2, and RMS_3 inputs. The Receiver Mode Select Inputs, in conjunction with the Control Register Load and Chip Disable, select the Receiver operating mode. RMS_1, RMS_2, and RMS_3 may be strobed or hard-wired to the appropriate input voltage. **RMS_3 / RMS_2 / RMS_1 / Selected Operating Mode** 0 0 0 ASYNCH OR ISOCH, 1X CLOCK 0 0 1 ASYNCH OR ISOCH, 16X CLOCK 0 1 0 ASYNCH OR ISOCH, 32X CLOCK 0 1 1 ASYNCH OR ISOCH, 64X CLOCK 1 X 0 SYNCH-EXTERNAL CHARACTER SYNCHRONIZATION 1 X 1 SYNCH-INTERNAL CHARACTER SYNCHRONIZATION NOTE: When operating in asynchronous or isochronous mode with 1X clock there is no protection against false start bits. A high-level input voltage, V_{IH}, applied to CD disables RMS_1, RMS_2 and RMS_3.
18,22 17, 36, 3, 38, 4, 40	MATCH-CHARACTER HOLDING REGISTER DATA	MHR_1, MHR_2, MHR_3, MHR_4, MHR_5, MHR_6, MHR_7, MHR_8	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs to the Match-Character Holding Register Load, $\overline{MHRL}$. Parallel 8-bit characters are input into the Match-Character Holding Register with the $\overline{MHRL}$ Strobe (pin 34). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. These inputs may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IL}, applied to CD disables MHR_1 and MHR_8.
5,23	WORD LENGTH SELECT	WLS_1, WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs of the Control Register Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below: **WLS_2 / WLS_1 / Selected Word Length** V_{IL} V_{IL} 5 BITS V_{IL} V_{IH} 6 BITS V_{IH} V_{IL} 7 BITS V_{IH} V_{IH} 8 BITS WLS_1 and WLS_2 may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
6	CHIP DISABLE	CD	This line controls the disable associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line disables inputs and removes drive from push-pull output buffers causing them to float. Drivers of disables outputs are not required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **Input Lines** / **Three-State Output Lines** $\overline{CRL}$, EPE, PI, WLS_1WLS_2, RMS_1-RMS_3, $\overline{DRR}$, $\overline{SFR}$, $\overline{MHRL}$, MHR_1-MHR_8 / PE, FE, OE, RR_1-RR_8
7-15	RECEIVER HOLDING-REGISTER DATA OUTPUT	RR_9-RR_1	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the Receiver Holding Register outputs, RR_1-RR_9. The parallel data character, including parity (RR_9), appears on these lines. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 15) is the least significant bit of the character. A high-level input voltage, V_{IH}, applied to CD disables RR_1-RR_9.
16	V_{GG} POWER SUPPLY	V_{GG}	– 12 Volts Supply.
19	PARITY INHIBIT	PI	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the EPE and PI inputs.
21	EVEN PARITY ENABLE	EPE	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be verified by the receiver. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, select odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable. PI and EPE may be strobed or hard-wired to the appropriate input voltage.

PI	EPE	Selected Parity	Comments
V_{IL}	V_{IL}	Odd	CD = V_{IL}
V_{IL}	V_{IH}	Even	CD = V_{IL}
V_{IH}	X	None	CD = V_{IL}

NOTE: If CD = V_{IH}, no programming is performed since inputs are disabled.

X — either V_{IL} or V_{IH}. When programmed, the appropriate parity is verified following the last data bit of a character, immediately preceding the stop element of asynchronous and isochronous characters.

A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
24	$\overline{\text{STATUS FLAG RESET}}$	$\overline{\text{SFR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{SFR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the PE, FE and OE Status Flags.
25	$\overline{\text{DATA RECEIVED RESET}}$	$\overline{\text{DRR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{DRR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the DR Flag. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{DRR}}$.
26	DATA RECEIVED FLAG	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the Receiver Holding Register. When operating in the synchronous mode, the first SYN character, when located and transferred to the Receiver Holding Register, will not cause DR to go to a high-level output voltage, V_{OH}, but will cause MDET to go to a high-level output voltage. Character transfer to the Receiver Holding Register occurs in the center of the last bit of a synchronous character or the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated.
27	OVERRUN ERROR FLAG	OE	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the OE input. A high-level output voltage, V_{OH}, indicates that the prevously received character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the Receiver Holding Register. This transfer occurs in the center of the last bit of a received synchronous character or in the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated. A high-level input voltage, V_{OH}, applied to CD disables OE.
28	FRAMING ERROR/ SYN SEARCH	FE/SS	FE/SS is a two-way (I/O) bus. If programmed for the ASYNCHRONOUS or ISOCHRONOUS MODE, a low-level input voltage, V_{IL}, applied to CD (pin 6) enables the FRAMING ERROR FLAG output which indicates the status of the STOP BIT detection circuit. A high-level output voltage, V_{OH}, indicates that the character transferred to the Receiver Holding Register has no valid STOP BIT; i.e., the bit following the PARITY BIT is not a high-level input voltage, V_{IH}. This transfer occurs in the center of the first stop element at which time this flag is updated. When programmed for the SYNCHRONOUS MODE, this line is an input and is not under control of CD. This line should be driven by a tri-state or an open collector device. If programmed for INTERNAL CHARACTER SYNCHRONIZATION, a transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, initiates the automatic internal "SYN" CHARACTER search operation.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
28	FRAMING ERROR/ SYN SEARCH	FE/SS	Prior to initiation of this operation, the Receiver Holding Register is "transparent" so that its contents are identical to that of the RECEIVER REGISTER. Upon receipt of a SYN character, (previously loaded into the Match-Character Holding Register during initialization), the Receiver Holding Register becomes non-transparent, the MATCH DETECT output (MDET) goes to a high-level output voltage. V_{OH}, but, the Data Received (DR) FLAG does not assume a high-level output voltage, V_{OH}. The P/SAR is now in character synchronization. Subsequent SYN or data character will be transferred to the RECEIVER HOLDING REGISTER as they are assembled (at the center of the last bit) and the DR FLAG will be raised. A transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, causes the P/SAR to lose character synchronization and forces the Receiver Holding Register to become "transparent." If programmed for EXTERNAL CHARACTER SYNCHRONIZATION, the system external to the P/SAR examines the data stream for "SYN" characters when SYN SEARCH is a low-level input voltage, V_{IL}. The Receiver Holding Register is "transparent" which allows the contents of the RECEIVER REGISTER to be monitored as it ripples through the shift register. When the external logic locates a "SYN" CHARACTER, indicated by a high-level input voltage, V_{OH}, on MDET, the SYN SEARCH line is externally raised to a high-level input voltage, V_{IH}. This high-level input voltage causes character synchronization to be initiated, returns the Receiver Holding Register to a "non-transparent" condition, causing subsequent characters to be transferred to the RECEIVER HOLDING REGISTER (when the center of the last bit of a character is recognized) and raises the DR FLAG.
30	MATCH DETECT FLAG	MDET	A high-level output voltage, V_{OH}, indicates that the contents of the Transmitter Register are identical to the contents of the Match-Character Holding Register. This flag is set to a high-level output voltage, V_{OH}, at the center of the first STOP ELEMENT of an asynchronous or isochronous character.
31	RECEIVER REGISTER CLOCK	RRC	This fifty (50) percent duty cycle clock provides the basic receiver timing. The negative transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, shifts data into the RECEIVER REGISTER at a rate determined by RMS_1, RMS_2 and RMS_3. Synchronous operation requires that this negative transition occur at the center of each data bit.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
32	MASTER RESET	MR	A high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets the contents of the Receiver Holding Register to a high-level output voltage, V_{OH}, resets the contents of the Match-Character Holding Register, the MDET, DR, PE, FE, and OE outputs to a low-level output voltage, V_{OL}, but does not effect the contents of the control register.
33	$\overline{\text{CONTROL REGISTER LOAD}}$	$\overline{\text{CRL}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{CRL}}$ input. A low-level input voltage, V_{IL}, applied to this line enables inputs to DC "D Type" Latches of the Control Register and loads it with Control Bits (EPE, PI, RMS_1, RMS_2, RMS_3, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables CRL.
34	$\overline{\text{MATCH CHARACTER HOLDING REGISTER LOAD}}$	$\overline{\text{MHRL}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{MHRL}}$ input. A low-level input voltage, V_{IL}, applied to this line enables input to DC "D Type" Latches of the Match-Character Holding Register and loads it with the Match-Character Holding Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{MHRL}}$.
35	RECEIVER INPUT	RI	The serial input data stream received on this line enters the Receiver Register determined by the character length, parity and the number of stop bits programmed. A high-level input voltage, V_{IH}, must be present when no ASYNCHRONOUS data is being received.

ORGANIZATION

PR1472 block diagram is illustrated on page 1.

Control Register — Programming of the PSAR is accomplished by loading the 7 Bit Control register. Mode selection, clock division, word length, and parity are selected when the Control Register Load (CRL) signal is activated.

Receiver Register — The Receiver Register is used to store the incoming data stream. The contents of this register can be gated to the Holding register during the transparent mode, or compared with the Match Holding Register. When a character is assembled it is transferred to the Receiver Holding Register.

Receiver Holding Register — The Receiver Holding Register, a buffer register, is used to store the assembled character.

Match Holding Register — The Match Holding Register is used to store the match character. The contents of this register are compared with the receiver register to establish character synchronization.

Timing & Control — The Timing and Control Logic generates the required control signals to assemble characters, match comparison, bit stripping, and generation of status/flag signals.

SYNCHRONOUS MODE OPERATION

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no Start or Stop bits. Character synchronization (the "framing" of this continuous bit stream into characters of a predetermined fixed length), must be accomplished by a comparison of this bit stream and a synchronization sequence. The P/SAR is designed to accommodate internal or external character synchronization by program control.

Referring to the Block Diagram of the Receiver, the Chip Disable (CD) enables or disconnects various in-

puts and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, DRR, SFR, PE, and OE and the outputs of the Receiver Holding Register, are also controlled by CD. It is necessary that CD enable these lines to allow strobing information in these registers and to allow examination of these output flags and data.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

Enabled by CD, the Control Register is loaded by strobing $\overline{CRL}$ to a low-level input voltage which defines mode of operation and clock rate selection, character length and selected parity if required. Table 1 illustrates all programmable synchronous formats.

Character synchronization from the data stream requires Receiver recognition of specific bit pattern(s) which define the relative position of synchronous characters in the data stream and subsequent character assembly. The P/SAR programmably accommodates internal or external character synchronization.

Programmed for internal character synchronization, a high-level input voltage on the Sync Search line, the Receiver Holding Register is "transparent" and its contents are identical to the Receiver Holding Register. The data stream, gated into the Receiver Input (RI) by the negative transition of the Receiver Register Clock (RRC), shifts through the Receiver Register and is compared with the preprogrammed character in the Match-Character Holding Register. A match, indicated by a high-level output voltage on Match Detect (MDET), returns the Receiver Holding register to its non-transparent state and initializes timing and control logic but does not set the Data Received Flag to a high-level output voltage. The character following the match will be transferred to the Receiver Holding Register at the receipt of the center of its last bit and the Data Received Flag is set to a high-level output voltage. Depending on line discipline, this last character may also be a synchronizing character, in which case, Match Detect will continue to be a high-level output voltage when the Data Received Flag is set. Therefore, sequence verification can be performed by the system (additional hardware or software as desired).

Parity, if programmed, is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. If a parity error exists, the associated PE register is set to a high-level output voltage.

Transfer of a character to the Receiver Holding Register sets the associated Data Received Register Flag (DR) to a high-level output voltage. The transfer of a character to the Receiver Holding Register, if the Data Received Register Flag had already been set to a high-level output voltage, causes the previous character to be lost (written over) and is alerted by an Overrun Error Flag which is a high-level output voltage. In normal operation, the Data Received Flag is reset by $\overline{DRR}$ when the Receiver Holding Register is serviced (unloaded). The Status Flags, PE and OE, are also provided with an external reset $\overline{SFR}$ so that block status and character status may be (accumulated) verified. A low-level input voltage on Sync Search causes character synchronization to be lost and initiates transparency of the Receiver Holding Register.

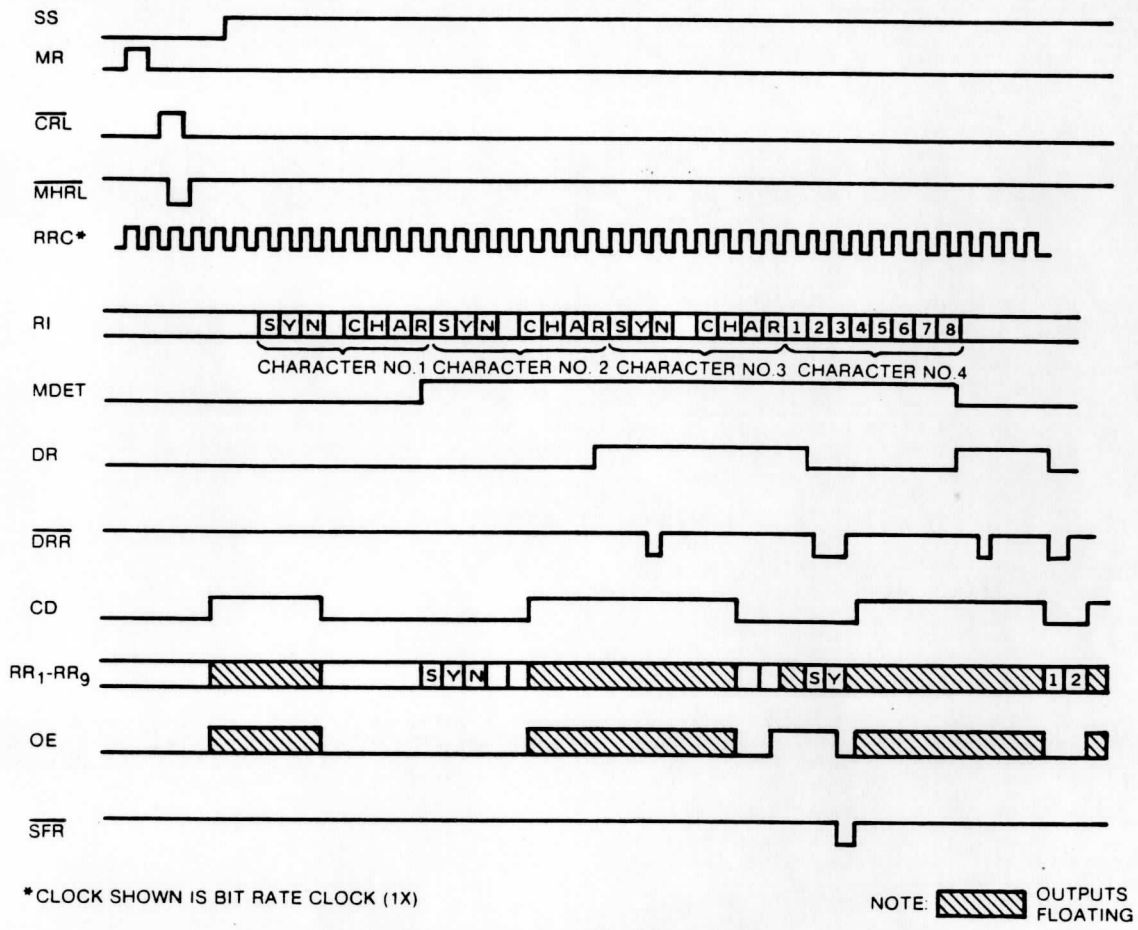
External character synchronization, programmed by the Control Register, is similar to the description above with the exception that the Sync Search line controls the nontransparency of the Receiver Holding Register directly and comparison is done externally. Upon recognition of the appropriate synchronizing pattern, the Sync Search line is set to a high-level input voltage prior to the end of the last bit. Raising the Sync Search line to a high-level input voltage causes the buffer to go "nontransparent", initializing timing and control circuitry to "frame" characters. The first bit received after a high-level input voltage is applied to Sync Search, defines the start of the "frame". Character length defined by the Control Register defines the end of the "frame".

Table 1. SYNC MODE CONTROL DEFINITION

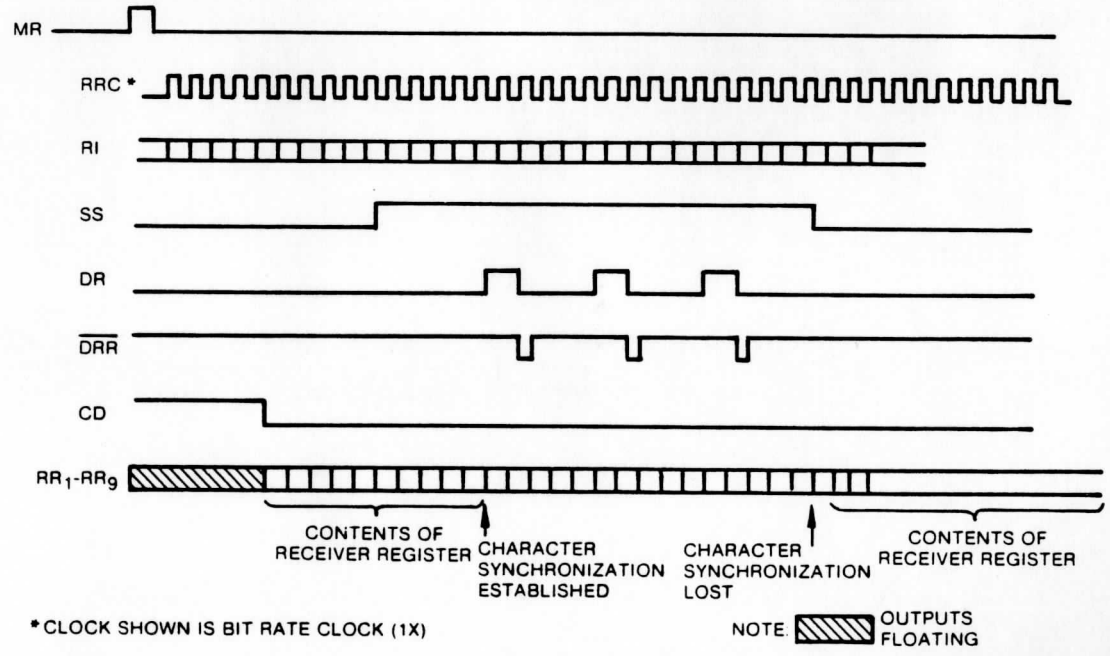
CONTROL WORD					CHARACTER FORMAT	
RMS	WLS2	WLS1	PI	EPE	DATA BITS	PARITY BIT CHECKED
1	0	0	0	0	5	ODD
1	0	0	0	1	5	EVEN
1	0	0	1	X	5	NONE
1	0	1	0	0	6	ODD
1	0	1	0	1	6	EVEN
1	0	1	1	X	6	NONE
1	1	0	0	0	7	ODD
1	1	0	0	1	7	EVEN
1	1	0	1	X	7	NONE
1	1	1	0	0	8	ODD
1	1	1	0	1	8	EVEN
1	1	1	1	X	8	NONE
↑ Sets to SYNC Mode						

If RMS_1 = 1, the receiver operates in the internal character SYNC mode.

If RMS_1 = 0, character SYNC must be externally provided.



(INTERNAL SYNCHRONIZATION)



(EXTERNAL SYNCHRONIZATION)

SYNCHRONOUS TIMING DETAIL

ASYNCHRONOUS & ISOCHRONOUS MODE

The completed assembly of a parallel character, by the P/SAR, from a serial data stream and buffered by its Receiver Holding Register is indicated by the status of the Data Received (DR) Flag. The assembly of character from a serial data stream consisting of a start bit, data, parity (if programmed), and a stop interval is initiated by the Start bit transition.

Verification of parity and receipt of a valid stop bit is accomplished prior to the character transfer to the Receiver Holding Register. Simultaneously, this data is compared with a preprogrammed character in the Match-Character Holding Register.

Status Flags, Data Received, Parity Error, Framing Error, Overrun Error and Match Detect are loaded into status registers during character transfer to the Receiver Holding Register.

Referring to the Block Diagram of the Receiver, the Chip Disable enables or disconnects various inputs and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, $\overline{DRR}$, $\overline{SFR}$, PE, FE, OE and the outputs of the Receiver Holding Register are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output data and flags.

Device operation is programmed subequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage, and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Characer Holding Register to be reset to a low-level output voltage.

When the Receiver is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage defines the mode of operation and clock rate selection, character length and selected parity if required. Table 2 illustrates all the programmable asynchronous formats.

A mark to space transition on the receiver input initializes the clock counter causing it to count to the theoretical center of the start bit. At this time, the input is sampled. A high-level input voltage at the Receiver Input causes the first mark to space transition to be interpreted as a noise spike and resets all timing and control logic. This provides one-half data bit noise immunity on all clock selection rates except 1X. A low-level input voltage at the Receiver Input at the theoretical center of the start bit causes timing and control circuitry to sample the theoretical center of succeeding data bits. This data is shifted through the Receiver Register. When an entire character (as defined by the Control Register) is assembled in the Receiver Register, the line is "tested" for a valid stop bit at its theoretical center. This character is also compared with the contents of the Match-Character Holding Register at the center of the stop bit and its parity is verified. A parallel transfer occurs, loading the contents of the Receiver Register (less start and stop bits) into the Receiver Holding Register. The status of the parity verification, framing error, and overrun error circuitry are also loaded into their approriate registers to provide output error flags when the Data Received Flag is set. If the Data Received Flag had not been reset prior to the assembly of the current character, the previous character is lost and this is indicated by a high-level output voltage on the Overrun Error Flag.

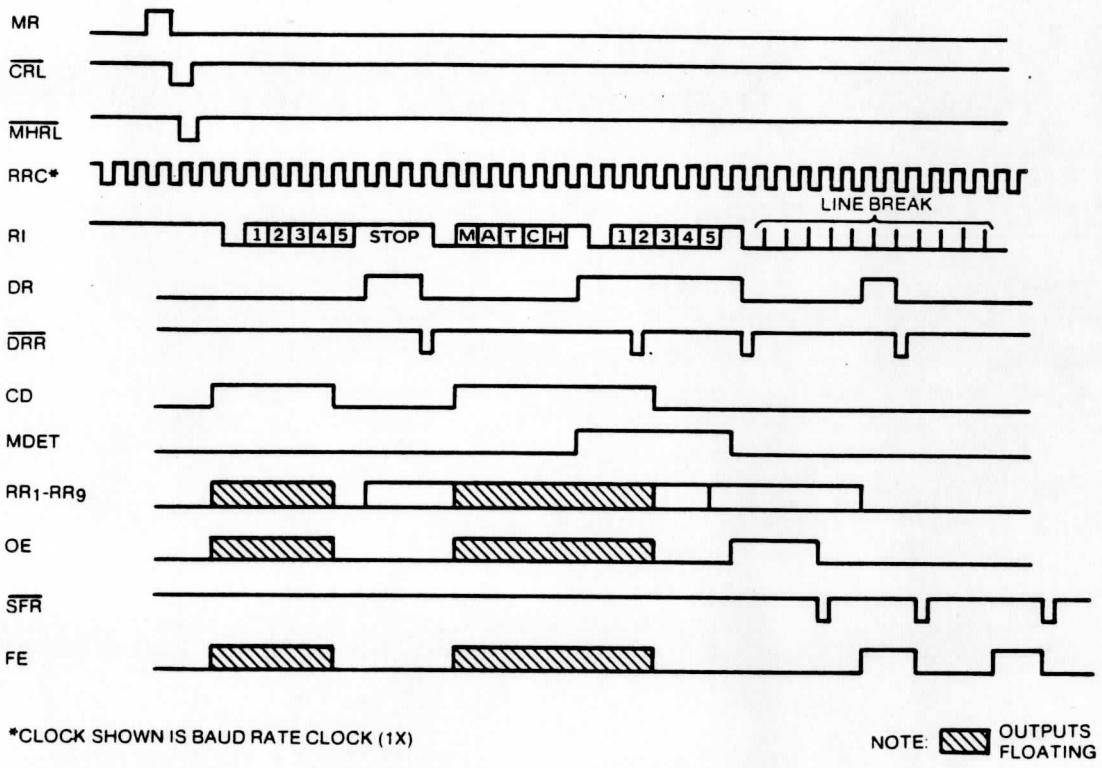
Table 2. ASYNCHRONOUS OR ISOCHRONOUS MODE CONTROL DEFINITION

RMS3	WLS2	WLS1	PI	EPE	Start Bit	Data Bits	Added Parity Bit	Stop Elements
0	0	0	0	0	1	5	Odd	1 or more
0	0	0	0	1	1	5	Even	1 or more
0	0	0	1	X	1	5	None	1 or more
0	0	1	0	0	1	6	Odd	1 or more
0	0	1	0	1	1	6	Even	1 or more
0	0	1	1	X	1	6	None	1 or more
0	1	0	0	0	1	7	Odd	1 or more
0	1	0	0	1	1	7	Even	1 or more
0	1	0	1	X	1	7	None	1 or more
0	1	1	0	0	1	8	Odd	1 or more
0	1	1	0	1	1	8	Even	1 or more
0	1	1	1	X	1	8	None	1 or more

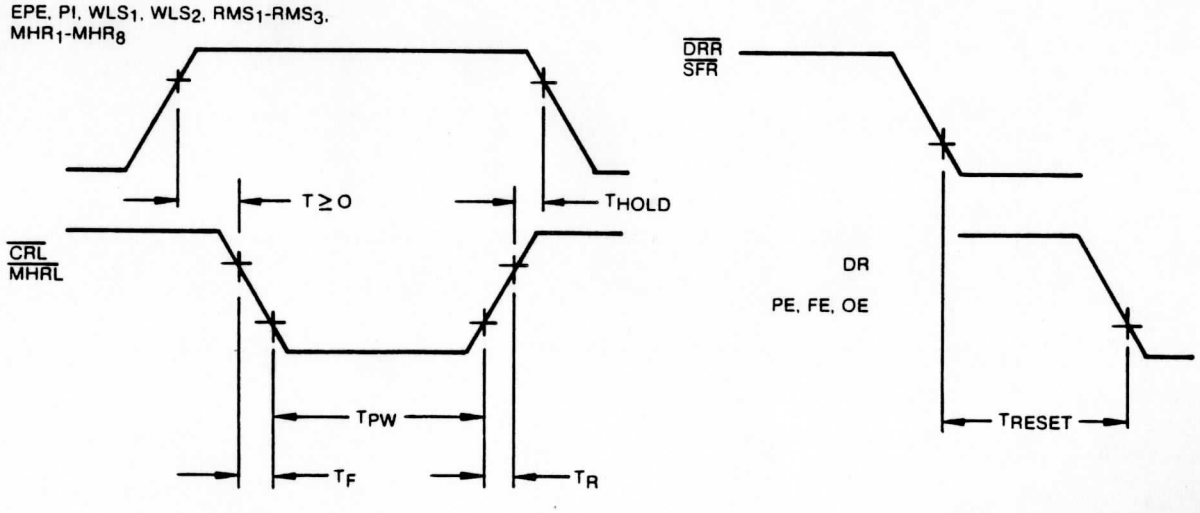
↑ Set to ASYNC or ISOC Mode

When RMS_3 is 0 (ASYNC or ISOC Mode), RMS_2 and RMS_3 determine the clock frequency according to the following table:

RMS_2	RMS_1	Clock Frequency
0	0	1X Baud Rate
0	1	16X Baud Rate
1	0	32X Baud Rate
1	1	64X Baud Rate

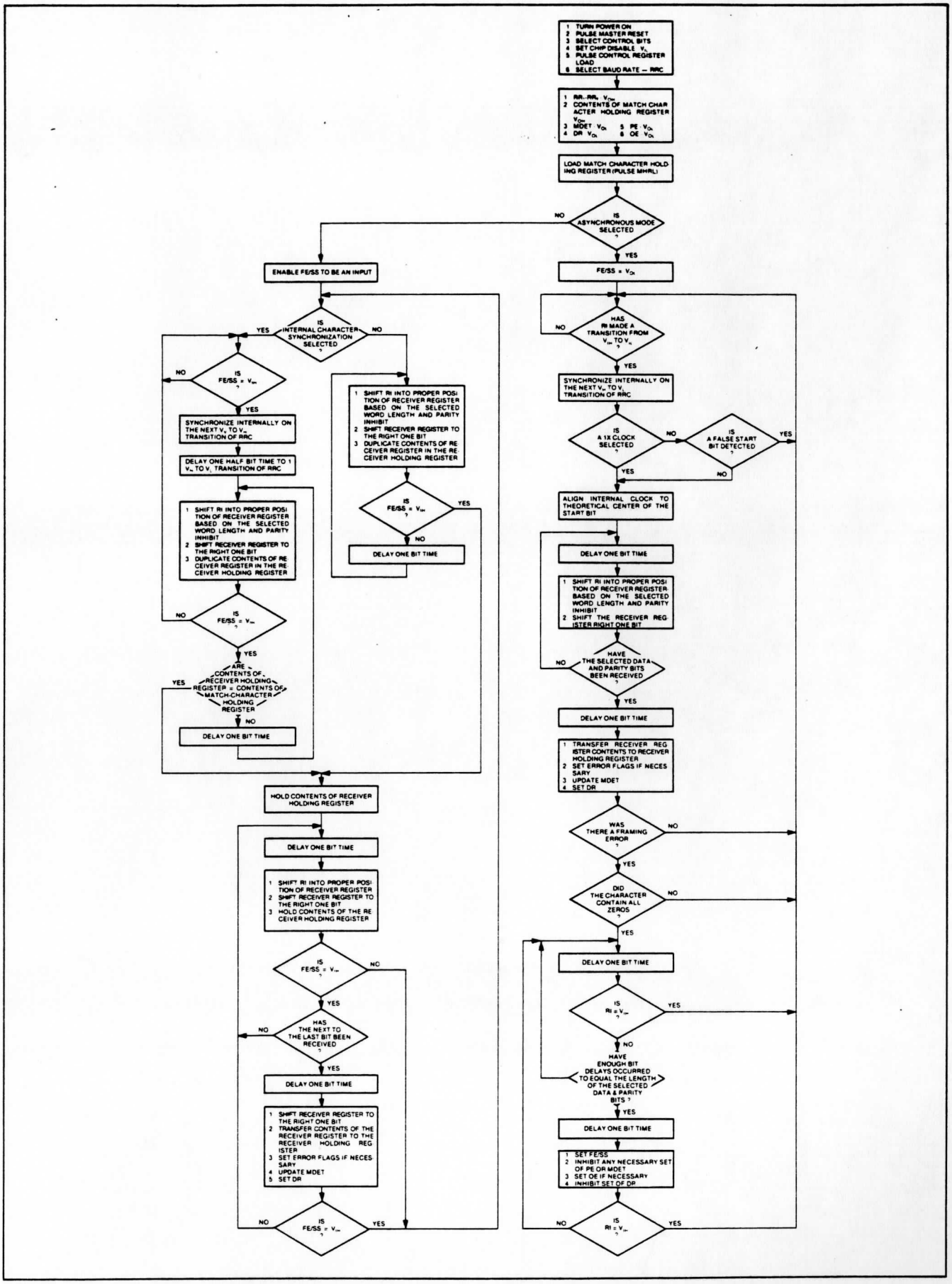


ASYNCHRONOUS & ISOCHRONOUS TIMING EXAMPLE



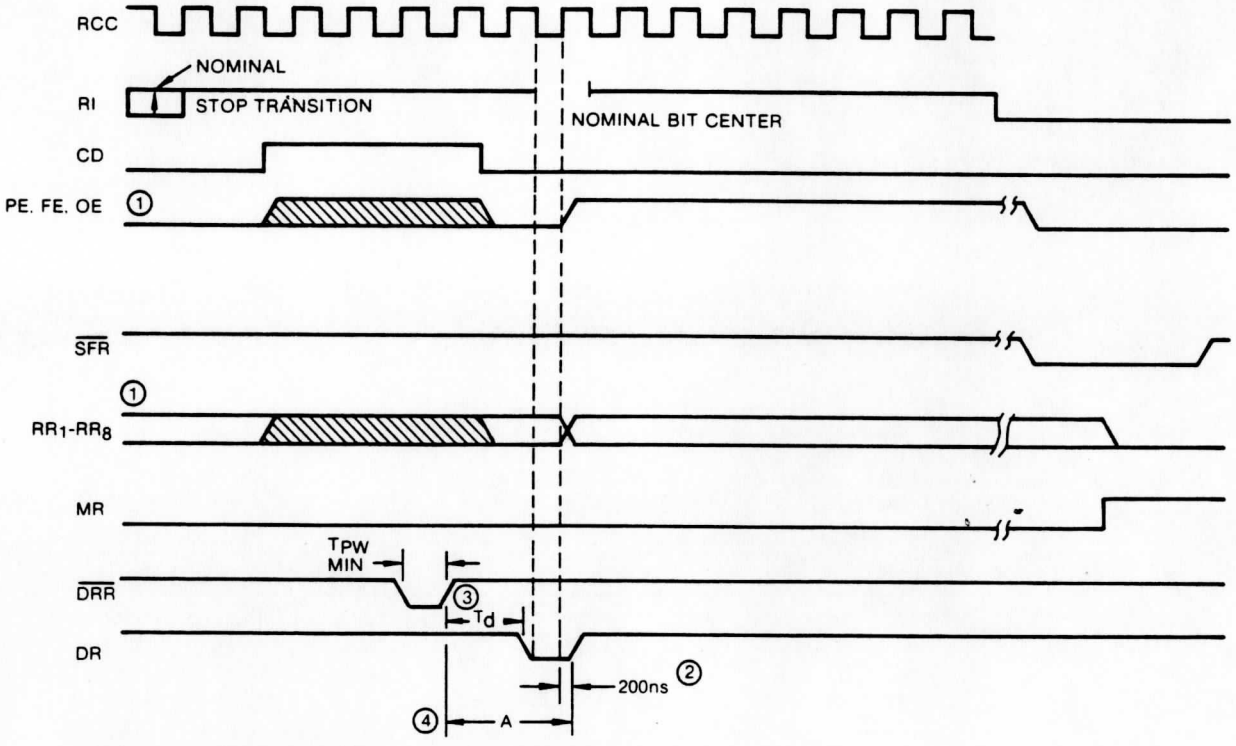
DATA INPUT LOAD CYCLE **RESET DELAY**

SWITCHING WAVEFORMS



PR1472 SYNCHRONOUS ASYNCHRONOUS RECEIVER FLOW CHART

6B-11



1. DATA AND ERROR FLAGS ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT.
2. DR IS DELAYED 200ns FROM DATA AND ERROR FLAGS.
3. THE DELAY BETWEEN DRR AND DR = T_d = 500ns.
4. $\overline{DRR}$ SHOULD BE HIGH A MINIMUM OF "A" ns (T_d +1/2 CLOCK + 200ns) PRIOR TO THE NEXT RISING EDGE OF DR.

TIMING DETAIL

MAXIMUM RATINGS

V_{GG} Supply Voltage		+0.3V to −20V
V_{DD} Supply Voltage		+0.3V to −20V
Clock Input Voltage*		+0.3V to −20V
Logic Input Voltage*		+0.3V to −20V
Logic Output Voltage*		+0.3V to −20V
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range		0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

*V_{GG} = V_{DD} = OV

NOTE: These voltages are measured with respect to V_{SS} (Substrate).

ELECTRICAL CHARACTERISTICS

(V_{SS} = V_{CC} = 5V ± 5%, V_{DD} = OV, V_{GG} = −12V ±5%, T_A = 0°C to +70°C unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
	INPUT LOGIC LEVELS[1]			
V_{IL}	Low-level Input Voltage		0.8V	V_{SS} = 4.75V
V_{IH}	High-level Input Voltage	V_{SS}-1.5V		
	OUTPUT LOGIC LEVELS[2]			
V_{OL}	Low-level Output Voltage		0.4V	V_{SS} = 5.25V I_{OL} = 1.6mA V_{SS} = 4.75V I_{OH} = −100uA
V_{OH}	High-level Output Voltage	V_{SS}-1.0V		
	INPUT CURRENT[1]			
I_{IL}	Low-level Input Current (each input)		-1.6mA	V_{SS} = 5.25V V_{IN} = 0.4V
	OUTPUT CURRENT			
I_{OS}	Short-circuit Output Current**		-2.2mA	V_{SS} = 5.25V V_{OUT} = OV

**Not more than one output should be shorted at a time.

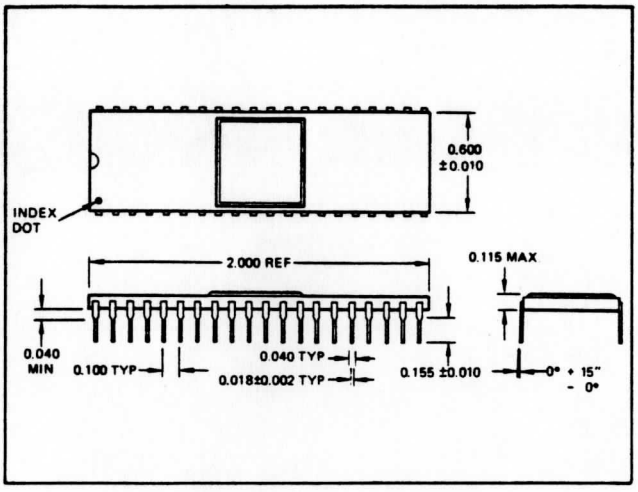
NOTE: 1) Inputs under Chip Disable control when disabled, (V_{IH} applied to CD), are logically disabled and appear as a single TTL Load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically and electrically disconnected and caused to float. The Three-State Output has three stages; (1) Low impedance to V_{CC} (2) Low impedance to GND (3) High impedance OFF ≃ 10 Megohm.

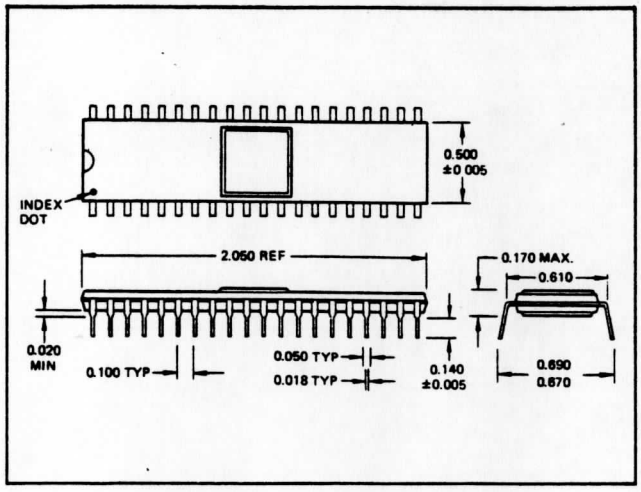
SWITCHING CHARACTERISTICS

(V_{SS} · V_{CC} = 5V, V_{DD} = OV, V_{GG} = −12V, T_A = 25°C, C_L = 20 pf)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC	100 KHz	PR1472-00
		DC	640 KHz	PR1472-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
$T_{\overline{CRL}}$	Control Register Load	250 nsec		
$T_{\overline{MHRL}}$	Match-Character Holding Register Load	250 nsec		
$T_{\overline{DRR}}$	Data Received Reset	200 nsec		
$T_{\overline{SFR}}$	Status Flag Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay	500 nsec		
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	



PR1472A CERAMIC PACKAGE



PR1472B PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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Printed in U.S.A.
Document No. A0020

PROM #1A

CHECKSUM = 5006 INTEGER
= 138E HEX

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
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01	1	1	1	1	1	1	1	1	8	8	8	8	8	8	8	8
02	2	2	2	2	2	2	2	2	9	9	9	9	9	9	9	9
03	3	3	3	3	3	3	3	3	C	C	C	C	C	C	C	C
04	4	4	4	4	4	4	4	4	D	D	D	D	D	D	D	D
05	5	5	5	5	5	5	5	5	E	E	E	E	E	E	E	E
06	6	6	6	6	6	6	6	6	F	F	F	F	F	F	F	F
07	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
08	1	0	1	0	2	0	0	0	1	0	1	0	2	0	0	0
09	2	0	B	A	2	0	2	0	2	0	B	A	2	0	2	0
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0B	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
0C	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
0D	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
0E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0F	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
11	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
12	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
13	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
14	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
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17	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
18	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
19	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1B	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

PROM #2A

CHECKSUM = 5202 INTEGER
= 1452 HEX

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02	2	2	2	2	2	2	2	2	9	9	9	9	9	9	9	9
03	3	3	3	3	3	3	3	3	C	C	C	C	C	C	C	C
04	4	4	4	4	4	4	4	4	E	E	E	E	E	E	E	E
05	5	5	5	5	5	5	5	5	D	D	D	D	D	D	D	D
06	6	6	6	6	6	6	6	6	F	F	F	F	F	F	F	F
07	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
08	1	0	1	0	2	0	0	0	1	0	1	0	2	0	0	0
09	2	0	4	3	2	0	2	0	2	0	4	3	2	0	2	0
0A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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0D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0E	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
0F	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
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11	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
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1B	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
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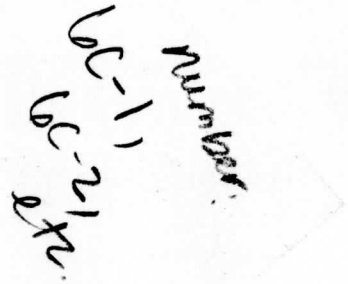

PROM #13A

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03	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
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08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
09	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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0F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
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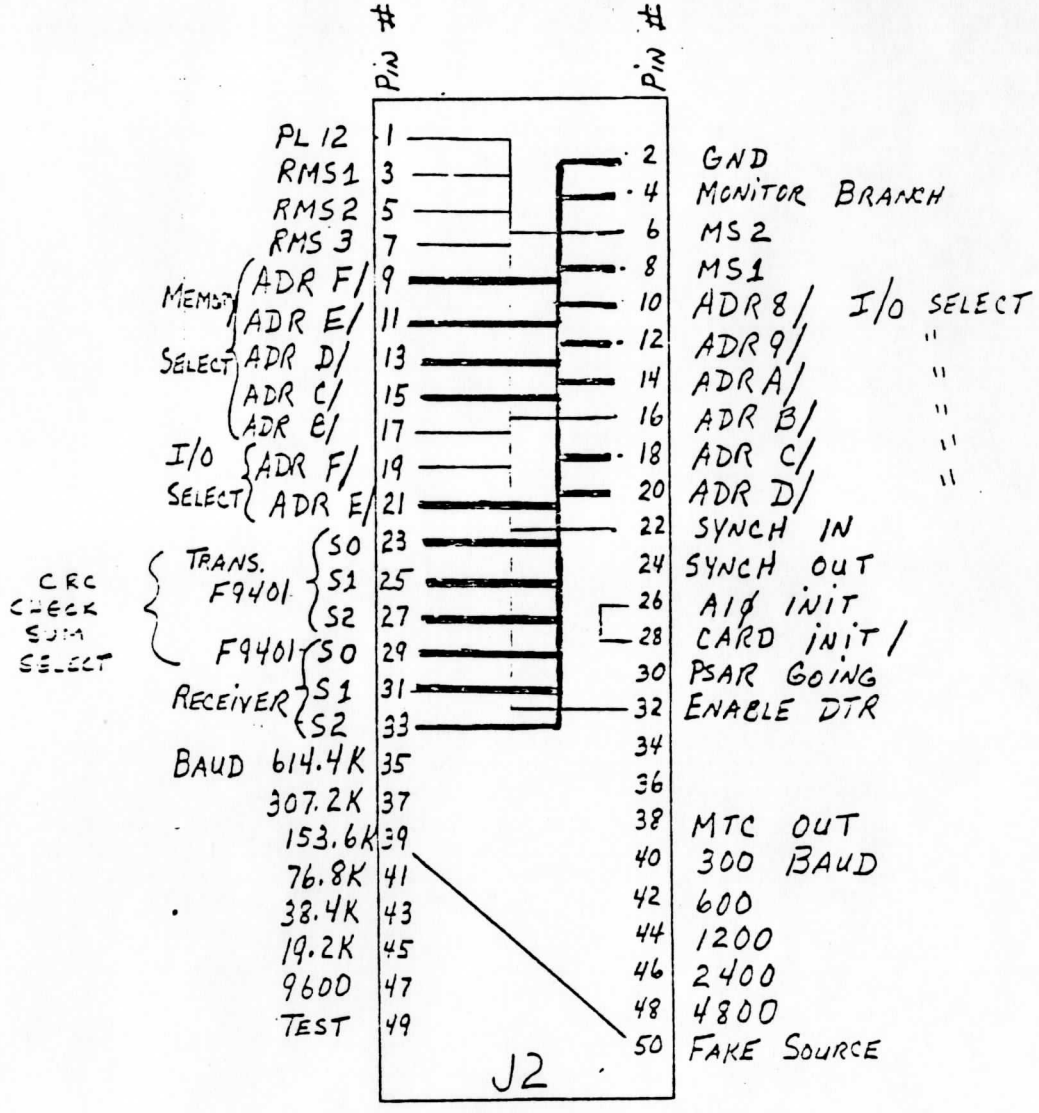
19	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1B	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

TERMINAL BISYNC PERSONALITY CONNECTOR - J2



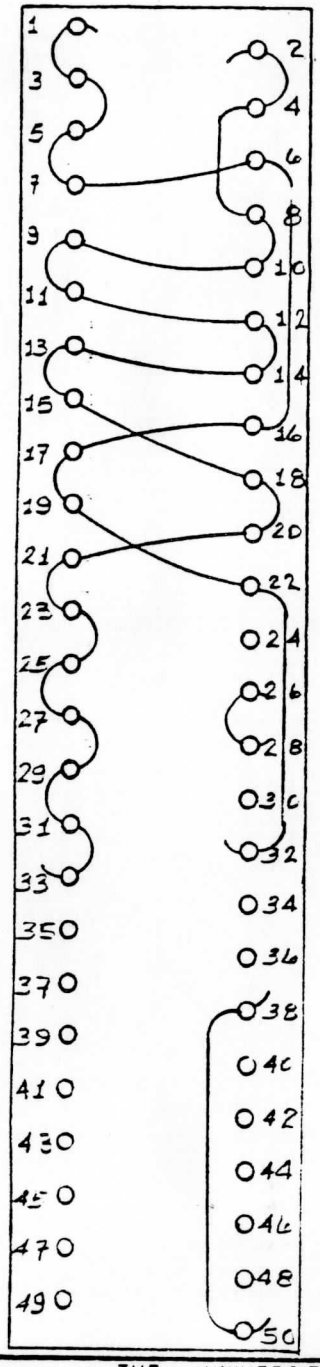
BAUD RATES: NORMALLY PIN 39 OR 41 JUMPERED TO PIN 50. DOES NOT HAVE TO BE SAME AT BOTH ENDS. IF CONNECTED TO TELEPHONE MODEM, JUMPER PIN 38 TO 50. BISYNC THEN USES MODEM CLOCK.

THE UNIVERSITY OF WISCONSIN
SPACE SCIENCE & ENGINEERING CENTER
MADISON WISCONSIN

TITLE
McIDAS KC (for use with 6800 3/24 cards)
BI SYNC J2 CONNECTOR

SCALE	CRAFTSMAN DATE	CHECKER DATE	ENGINEER DATE
NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE DATE	PROJECT APPROVAL DATE	
PROJECT NO 3504	SIZE	SHEET 4 OF 12	DRAWING NO DW 3504-005

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED



JUMPER: 1,3,5,6,7,16, 17,19,22,23.

JUMPER: 2,4,8,9,10,11,12, 13,14,15,18,20,21,23, 25,27,29,31,33.

JUMPER: 26-28

SHOWN FOR MODEM CONNECTION (JUMPER 38-50)

50 PIN CARD EDGE CONNECTOR
3M 3415-0001
FOR USE WITH EC/24 TERMINAL

THE UNIVERSITY OF WISCONSIN
SPACE SCIENCE & ENGINEERING CENTER
MADISON, WISCONSIN

TITLE MCIDAS KC
BI SYNC J2 CONNECTOR
JUMPER DIAGRAM

SCALE	CRAFTSMAN DATE	CHECKER DATE	ENGINEER DATE
	D.FORD 12-10-84		
NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE DATE	PROJECT APPROVAL DATE	
PROJECT NO 7000	SIZE A	SHEET 5 OF 12	DRAWING NO DN 3504-0005

CONTROL BOARD

SECTION 7
DATARAM CONTROL BOARD
TABLE OF CONTENTS

DATARAM CONTROL BOARD
(SSEC DRAWING 645Ø-Ø377, MODIFICATION F, DATED 4/23/84)

INTRODUCTION

Present generation McIDAS Workstations use "off-the-shelf" dynamic RAM storage units manufactured by DATARAM Corporation. Each workstation uses three units, one for each of the two image channels and a third for the graphics channel.

In a typical DATARAM application, a DATARAM BS-102 7-inch chassis contains the following:

- an integral power supply
- a Bulk Interface Card (BI)
- a Bulk Semi Controller (BSC)
- up to four Bulk Semiconductor Array boards (BSA)

A BSC provides drive and addressing for all BSA (memory) boards. The BI card provides the interface between the memory system and the CPU. Because the McIDAS data storage protocol is unique, none of the several versions of BI cards manufactured by DATARAM Corporation satisfy the protocol requirements. As a result, the DATARAM Control Board was custom-designed by SSEC. The custom card plugs into the BI slot of the DATARAM Chassis and no DATARAM Chassis or circuit board alterations are required.

The DATARAM Control Board performs two major functions. It provides the protocol interface between the Intel Multibus used in the McIDAS and the DATARAM Memory System (We use the term "DATARAM Memory System" to include: one chassis with integral power supply, one Bulk Semi Controller Card, a DATARAM Control Board, and one or more BSA boards.), and it provides considerable automation for the data storage and retrieval processes, reducing microprocessor overhead. Because one major function of this board is to interface two very different protocols, a thorough understanding of this board requires an in-depth understanding of both systems' protocols. The DATARAM protocol is documented in the Bulk Semi Memory System Model DR-129/229S technical manual by DATARAM Corporation.

If additional information is required on the Multibus, consult the INTEL SBC 80/24 technical manual.

Because of the complexity of the DATARAM Control Board, the Functional Description is divided into a "Functional Overview," and a "Detailed Function Description." The overview provides the big picture while the detailed description provides approximately the same level of detail as the "Functional Description" sections of other SSEC board documentation.

FUNCTIONAL DESCRIPTION

OVERVIEW

McIDAS is a TV-video-frame-based machine, that is, data storage and retrieval are performed by specifying video frame numbers. A TV video frame consists of 525 horizontal lines containing 78Ø pixels each. Several lines, and several pixels at the ends of each line, are blanked by the vertical and horizontal blanking periods respectively. For memory allocation within the workstation DATARAM memory, a video frame is defined as 512 lines containing 64Ø pixels each. Therefore, each frame contains 327,68Ø pixels. Since an Intel 8Ø85 microprocessor can directly address a maximum of only 65,536 addresses (a fraction of one frame) and the workstation can store up to 192 frames of data (approximately 63 million pixels), an indirect addressing scheme is required. A frame of image data is transmitted from the host computer to the workstation as 327,68Ø six-bit pixels. Each pixel is processed by the microprocessor compression algorithm (described in detail in the "Dual Channel Colorizer" section) into three-bit partitions. The three-bit partitions are stored in (and retrieved from) the DATARAM memory system.

A frame of graphics data is transmitted from the host computer as three-bit values for specified pixel addresses. A graphics frame may require only a few values, since only the foreground is transmitted. Note: the microprocessor does not compress the three-bit values.

The DATARAM BSA boards are each organized as 512K by 32-bit words plus seven bits of error correction code (ECC). The ECC allows the DATARAM memory system to correct internally any single-bit errors during retrieval and to detect multiple-bit errors. Since each of the three DATARAM memory systems can be populated with up to four BSA boards, each unit can store up to 2 million 32-bit words.

To summarize the data formats, the workstation communicates with the DATARAM Control Board in terms of "frames" and "partitions," while the DATARAM Control Board communicates with the memory in terms of direct addresses and 32-bit words.

In the functional description and theory of operation discussions that follow, only one third of the story is told. Unit Ø contains the graphic overlay data while units 1 and 2 contain the image data. The three units function in parallel. To simplify the discussion, only one of the units, representative of unit 1 or 2, is considered. This leaves the you with the responsibility to expand to three units the events described in one of the units, therefore understanding the system as it actually operates.

Figure 1 is a functional overview block diagram of the DATARAM Control board. The following are the three major functional sections in Figure 1:

- Data formatting
- Address Generation
- Control and Handshake

Data Formatting

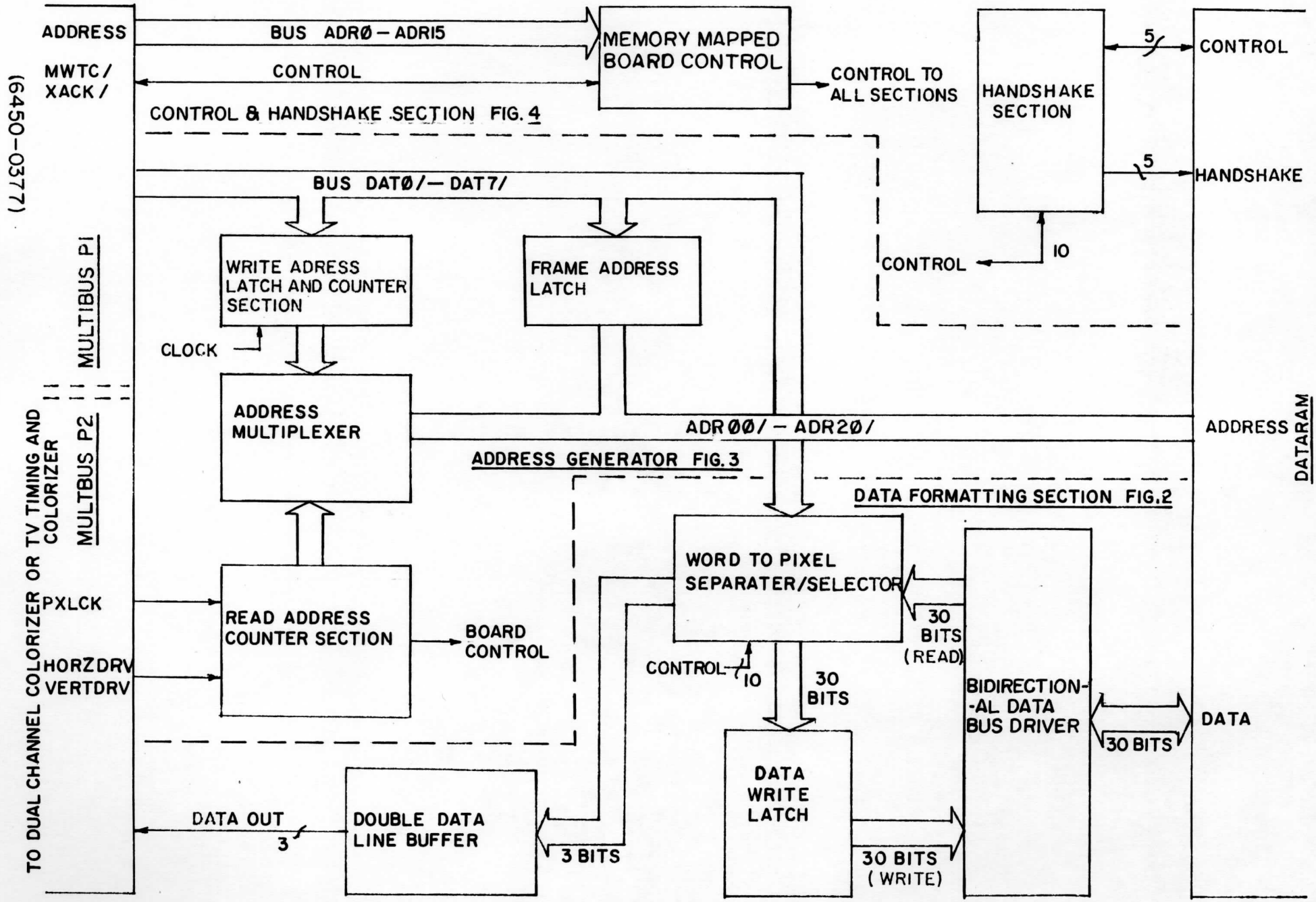
DATARAM manufactures two different word length memories, a 32-bit and a 36-bit version. Both versions use the same 36-bit bus structure. The 36-bit version uses all data bus lines (numbered ØØ-35) while the 32-bit version uses ØØ-15 and 18-33. In the McIDAS, only the 32-bit version is used, and ten 3-bit pixels are packed in each 32-bit word prior to storage. Two data bits are not used (numbers 32 and 33). Thus we use data bus lines ØØ-15 and 18-31. From here on, all reference to "word" means 3Ø bits.

The DATARAM system operates in several modes but only the following three are used in McIDAS:

- 3Ø-bit read
- 3Ø-bit write
- 3Ø-bit read/modify/write (R/M/W)

The 3Ø-bit read reads data, the 3Ø-bit write erases data and the R/M/W mode stores data.

In Figure 1, the Bidirectional Data Bus Driver separates the 3Ø-bit bidirectional data bus into a 3Ø-bit read bus and a 3Ø-bit write bus. The



DATARAM CONTROL
FUNCTIONAL OVERVIEW BLOCK DIAGRAM

FIGURE 1

3Ø bits of read data are unpacked by the Word-to-Pixel Separator/Selector into 1Ø three-bit pixel partitions and exported to the Double Data Line Buffer one pixel at a time. The Double Data Line Buffer consists of two RAM buffers which alternately read and write data. The buffers can store one horizontal line of data (64Ø three-bit pixel partitions). As one buffer is filled with data, the other is emptied. At the end of each horizontal scan, the buffers switch roles. The buffers are necessary because memory read, write and refresh cycles (dynamic RAMs) are multiplexed; by loading in an entire line under these conditions and unloading under control of pixel clock (PXLCK), the data read out flow is smooth and uninterrupted (synchronized to PXLCK). The data output from the buffer is output to the Dual Channel Colorizer (image units only) or to the TV Timing and Colorizer Unit (graphics unit).

The data storage cycle is quite different from the one just described for the read cycle. The data write cycle (R/M/W) consists of reading a 3Ø-bit word into the Word-to-Pixel Separator/Selector and modifying one partition with new write data. The modified word is latched by the Data Write Latch and written back into the same memory location as the original word. Thus, though the data is read in 1Ø-pixel groups, it is written one pixel at a time.

Address Generation

There are 483 visible lines in a 525-line TV frame. The remaining 42 lines are blanked by vertical blanking. Each horizontal line is blanked about 17% of the time by horizontal blanking, resulting in approximately 648 visible pixels (83% of 78Ø) per horizontal line. Because digital memories are addressed in binary, a block of memory must be set aside for each frame that is addressable in exact powers of two and is approximately the size of the visible image. If we pack 1Ø pixels per 3Ø-bit word, we need 64 words per 64Ø-pixel horizontal line. The number of horizontal lines with an exact power of two closest to 483 is 512 (only the first 483 lines are used). Thus, a frame allocation in memory consists of 512x64 words (32,768 words or 327,68Ø pixels). Because there are 512K words of storage on each BSA board, each board can store 16 frames. Each unit will store 16, 32, 48 or 64 frames, depending on the number of BSA boards in the chassis.

The Address Generation Section consists of a Read Address Counter, a Write Address Latch and Counter Section and a Frame Address Latch Section. A Frame read process consists of sequentially reading 32,768 words, starting at some particular address (frame number). As a result, the entire read sequence can be controlled automatically by a counter once the starting address and unit number are known. Thus, a read cycle is performed by addressing the proper unit (unit Ø, 1 or 2) and sending a six bit frame number (becomes upper six bits of the address to the DATARAM). The Write process is similar, but slightly more complicated. Here, counter address (Ø-32767) and pixel address (Ø-9) may be preloaded and the counter mode (increment/decrement and enable/disable) must be selected. The increased complexity and flexibility of the write address section is due primarily to the graphics write process requirements. Only the graphics data points are stored, not the background. Thus, a graphics frame may contain only a few scattered pixels whereas an image frame is made up of all pixels. (It is possible to load images into the graphics channel, but this is usually not done.)

Handshake Section

The Multibus and DATARAM each have their own timing and control sections which would be incompatible without the Handshake Section. The data read, write, and R/M/W cycles are broken down into several subcycles. Only the DATARAM Control Board can initiate a cycle (or subcycle). However, once a cycle is initiated, sequencing to the next subcycle can be accomplished only after the DATARAM indicates that the current subcycle is completed. The received acknowledgement triggers the request for the next subcycle. This process continues until the cycle is completed. The Handshake Section forces both units into synchronism during cycle execution.

Board Control

There is considerable control logic on the DATARAM Control Board. While the source of some of the control logic is easily defined, some is obscure at discussion levels other than the Detailed Circuit Descriptions. In general, however, there are two major sources of board control: the Memory Mapped Board Control and the Read Address Counter Sections (see Figure 1). The former is a block used almost exclusively to control the

Address Generation section of Figure 1. Within the Read Address Section there are two counter units. One of the counters generates several control signals which either directly or indirectly control nearly all remaining blocks in Figure 1.

DETAILED FUNCTIONAL DESCRIPTION

DATA FORMATTING

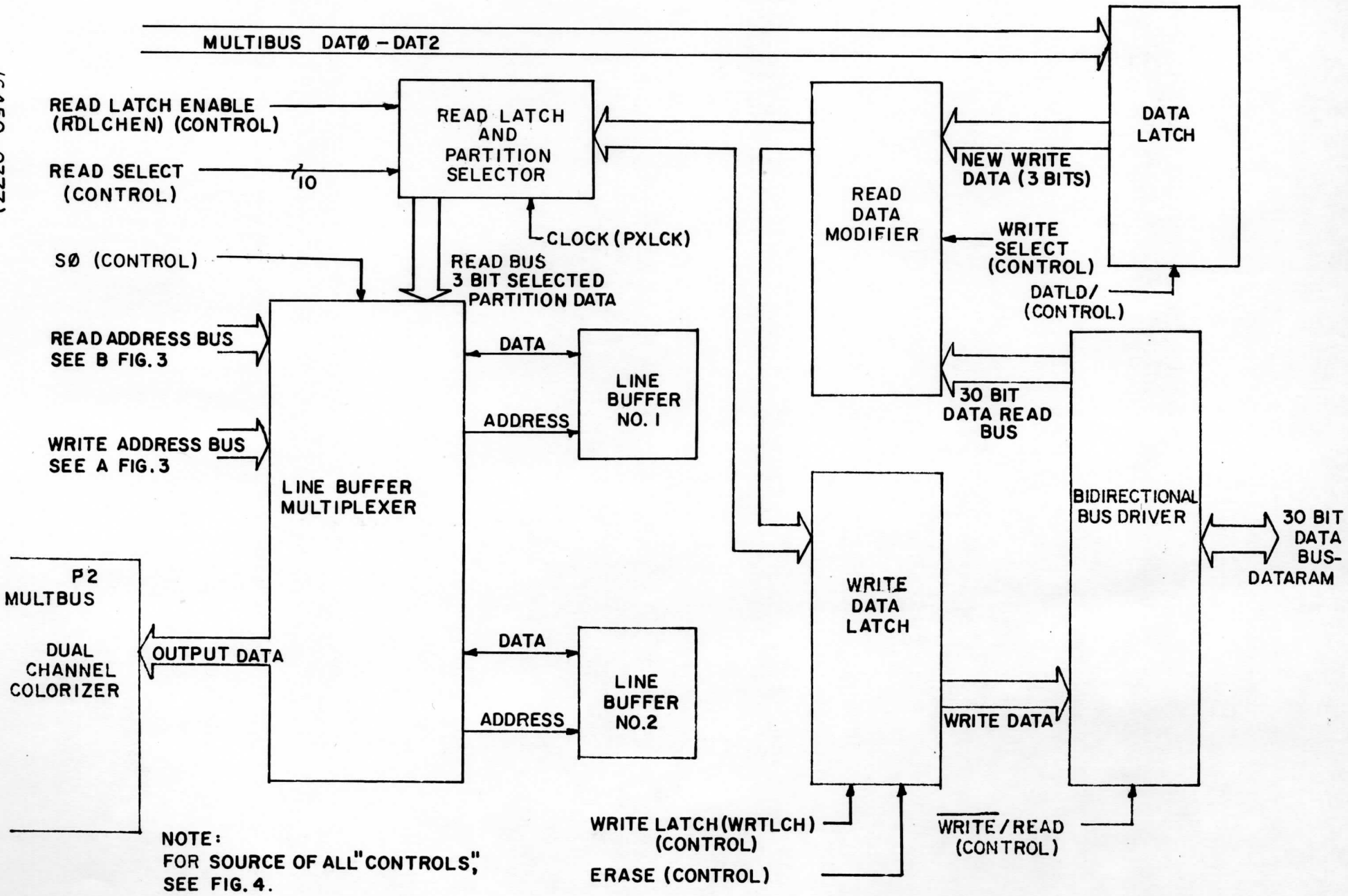
The Data Formatting section described in the Functional Overview is shown in Figure 2.

The Bidirectional Bus Driver is either in the input mode or the output mode, as determined by the control signal $\overline{\text{WRITE}}$/READ. When the control signal is high (read), the 3Ø-bit DATARAM Data Bus is connected to the Read Data Modifier. When the signal is low (write), the 3Ø-bit DATARAM Data Bus is connected to the 3Ø-bit Write Data Latch. During a read process, all Write Select lines going to the Read Data Modifier are inactive high. During this time, the Read Data Modifier passes the 3Ø-bit Data Read Bus to the Read Latch and Partition Separator.

A Read/Modify/Write cycle consists of a read portion followed by a write cycle. The read portion of the cycle is identical to the read cycle description above except a write data partition previously latched into the Data Latch is substituted for one of the read data partitions within the Read Modifier block. The partition to be substituted is determined by which Write Select line is active low. At this time, the output of the Read Modifier exactly matches the 3Ø-bit Data Read Bus input, with the exception of the substituted partition (27 old data bits and three new). While the modified word is present at the output of the Read Modifier, the Write Data Latch is strobed by bringing the Write Latch Control signal active low. When the Write portion of the R/M/W cycle is executed, the output of the Write Data Latch is connected to the 3Ø-bit DATARAM Data Bus by bringing $\overline{\text{WRITE}}$/READ low.

The ERASE/ control is used in the 3Ø-bit write mode only and is used to erase graphics frames. It causes the Write Data Latch to inject all zeros when it is active low, thereby clearing 1Ø pixels per cycle.

Read data, presented to the Read Latch and Partition Separator, is latched by bringing the Read Latch Enable signal active low. Then, each



DATA FORMATTING SECTION
FUNCTIONAL BLOCK DIAGRAM
FIG. 2

(6450-0377)

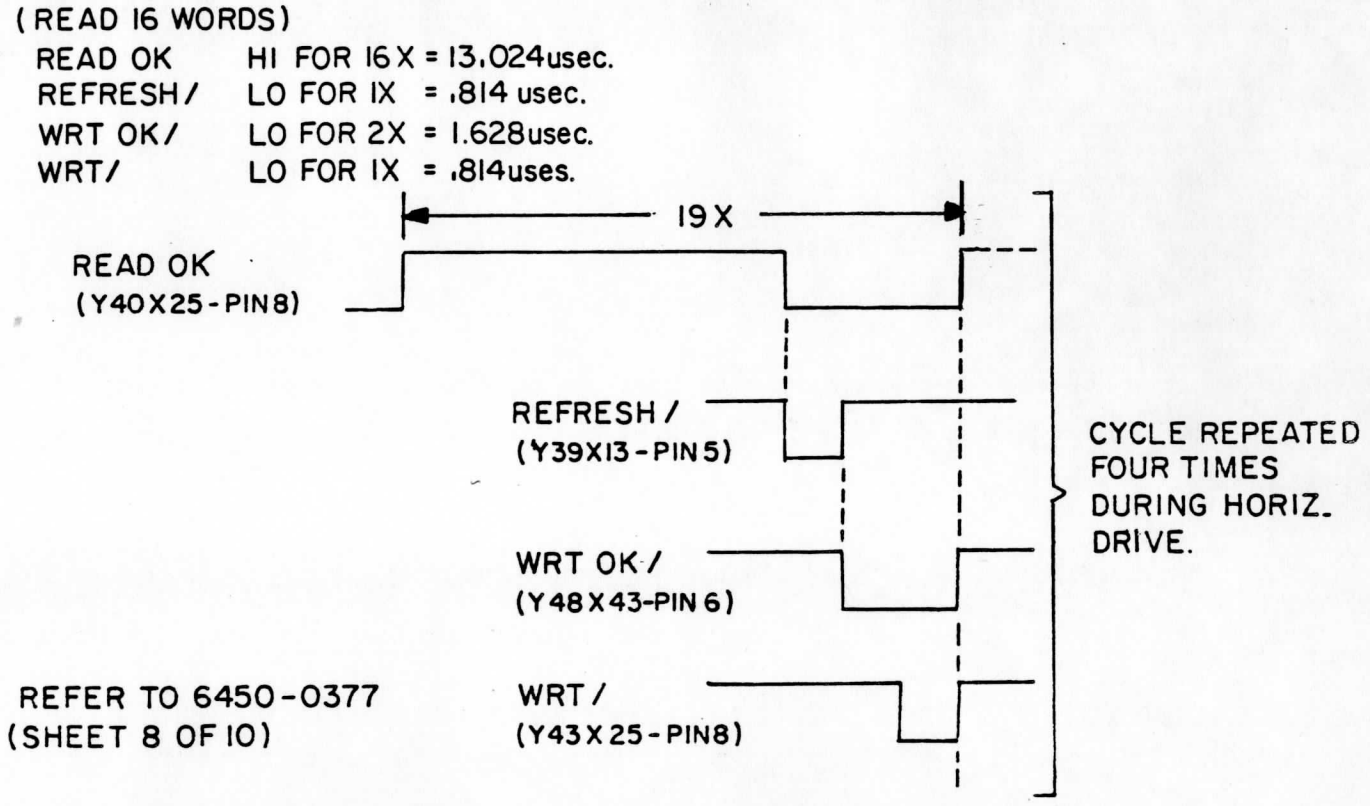
partition is sequentially gated onto the Read Bus by enabling its associated Read Select line. The Read Bus data is sent to the Line Buffer Section. The need for the Line Buffer is explained in the next paragraph.

The relationship between horizontal drive time and pixels is established in the TV Timing and Colorizer board at 78Ø pixels per horizontal drive period. The DATARAM Control Board establishes the number of data pixels per horizontal line at 64Ø, leaving 14Ø pixels as non-data pixels. The 64Ø data pixels are contained in 64 words. The words must be read and disassembled into pixel partitions during each horizontal period. In addition to reading data from memory, two other processes, memory refresh and data writes (an R/M/W cycle), must be performed periodically.

The DATARAM memory requires a refresh cycle approximately every 14 μsec (one-fourth of a horizontal drive period). The DATARAM chassis are supplied to SSEC with a modification which allows the refresh cycle to be controlled externally, from the BSC board. This enables the DATARAM Control board to determine when a refresh cycle will occur.

A refresh and a R/M/W cycle require about 1Ø and 2Ø pixel periods respectively. Therefore, we can break a horizontal period (63.49 μsec) into four repeating cycles, consisting of 16 data reads (16Ø pixels) one refresh (1Ø pixels) and a R/M/W cycle (2Ø pixels). The fourth cycle has 2Ø extra pixels, resulting in 78Ø pixels/horizontal period. Note: if no memory write request is made, a R/M/W cycle simply is not executed, though the time is set aside for it. The timing diagram below should help to summarize the three cycle time relationships.

If a pixel period is 81.4 nsec, then 1Ø pixels = .814 µsec. Let x be defined as 1Ø pixels = .814 µsec = one word time.



If the Read Bus Data was output directly to the Dual Channel Colorizer, there would be four vertical black bars on the screen. By writing the four groups of 16 words each into a buffer, and then reading them out under control of pixel clock, the data is fully synchronized and smooth flowing. To perform this function, two buffers are required. While one buffer is in a write mode the other is in a read mode. At the end of each horizontal line, the buffers swap modes. Each of the buffers are static RAMS organized as 4-bit by 1Ø24-bit. Only three bits are used and only the first 64Ø cells are used. These RAMS have a bidirectional data port. Therefore, the data input/outputs, as well as the address sources must be switched. For example, if Line Buffer #2 is addressed by the Write Address Bus and is receiving input data from the Read Bus, then Line Buffer #1 is addressed by the Read Address bus and is outputting data to the Dual Channel Colorizer (or TV Timing and Colorizer if this is the graphics unit).

DATARAM ADDRESS

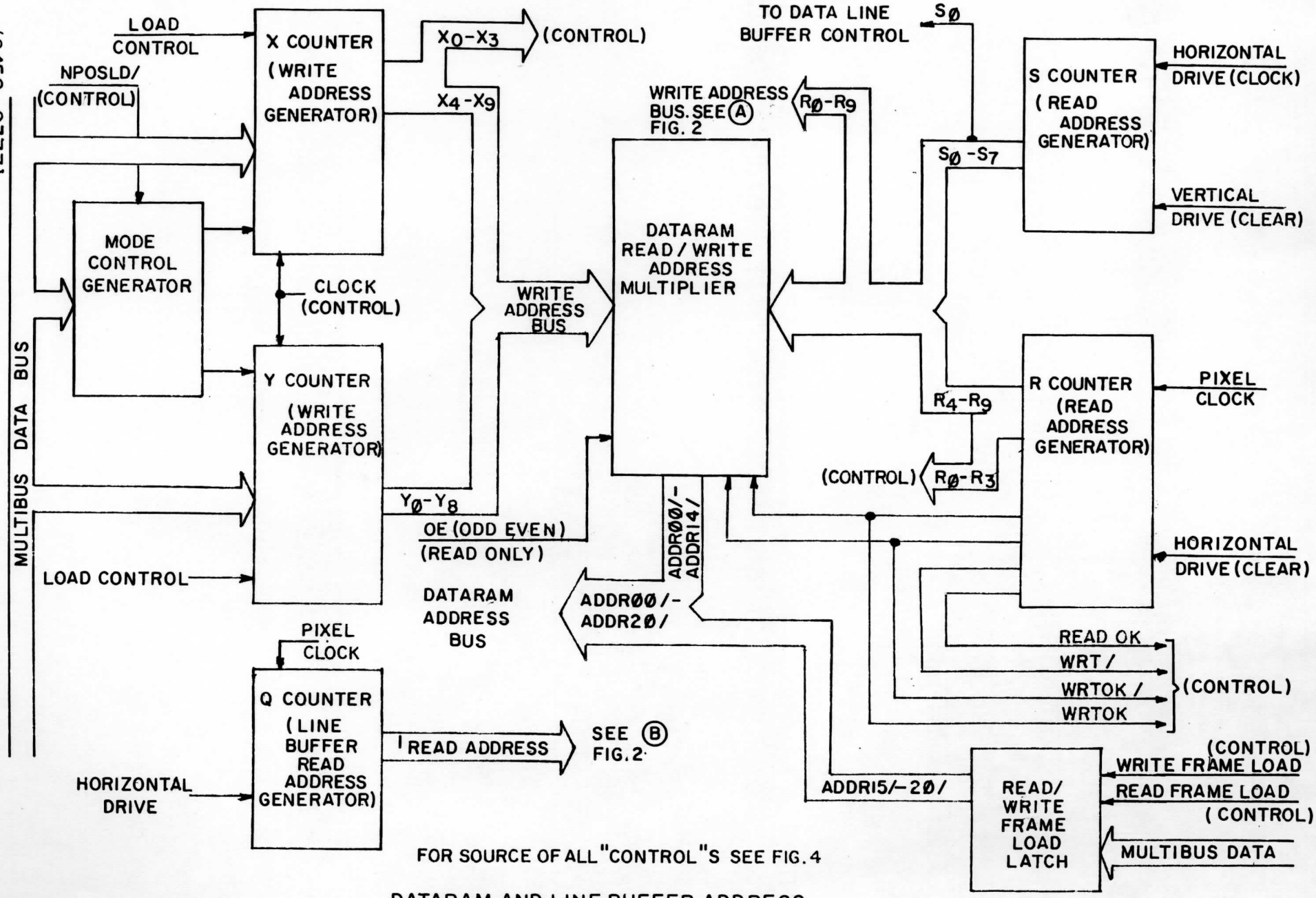
Figure 3 is a function block diagram of the DATARAM address bus generator. While the 21-bit address bus within the DATARAM is common to both the read and write functions, two separate address generation sources are required because of the different read and write functional requirements. The write address generator must be presettable to any pixel address prior to the storage of each pixel, while the read address generator simply needs to be incremented each time a word is read from the DATARAM.

Two counters, X and Y, make up the lower 15 bits of the write address; the S counter, R counter, and OE (odd/even signal from the TV Timing and Colorizer board) make up the lower 15 bits of the read address. The OE signal is used for interlacing the video images during the read process and will be discussed in the Detailed Circuit Description Section.

The Y counter is a nine-stage presettable Up/Down binary counter. The X counter, a 1Ø-stage counter, is similar to the Y counter except that the least significant four bits function as a BCD (binary-coded decimal) counter. The BCD portion of the X counter is used only to form the "Write Select" control signals shown in Figure 2. Both counters are clocked by a common clock generated in the Control Section. The clock is pulsed low each time a data write to the DATARAM is completed. If the X counter is in a count up mode, 1Ø clock pulses are required for each increment of the non-BCD portion of the counter (X_4-X_9). If the Y counter is inhibited while X is in a count up mode, 1Ø data writes to each address occur. This is exactly what occurs during an image storage process. Since only one pixel partition at a time is written to memory, 1Ø data R/M/W cycles are required to write 1Ø partitions (one complete word). X_0-X_3 select the pixel to be written into.

The non-BCD portion of the X counter acts as a six-stage binary word counter. The six stages have a full count of 64, the number of words in a horizontal line. During an image load process, the Y counter is allowed to increment on every 64Øth pixel. Thus, the Y counter is a line address generator.

Both X and Y counters are fully programmable. They can count in either direction or be inhibited; they can be preloaded with any count



DATARAM AND LINE BUFFER ADDRESS GENERATOR SECTION

FIGURE 3

from zero to their maximum count. The memory mapped Mode Control Generator is the source of all X and Y counter mode controls. The Mode Control Generator consists of a PROM whose address inputs are driven by latched Multibus data lines. The latch is enabled by the control signal NPOSLD (Next Position Load). A single eight-bit Multibus data byte, latched by NPOSLD/, controls the modes of both counters. The counters are preloaded with data from the Multibus data bus under the control of signals from the Control Section (memory mapped also).

The R and S counters function as the Read Address Generator. The R and S counters are very similar in function to X and Y respectively. Instead of preset inputs, both the R and S counters have a "clear" input. Since the R counter is the word counter, it is cleared at the beginning of each horizontal scan line and is clocked by pixel clock. Because the only inputs to the R counter are pixel clock and horizontal drive, the counter is always active and always counts up. It is, therefore, an ideal section for generation of all basic sub-line control signals. The following four control signal outputs from the R counter are used by the Control section to produce read/write cycle control as well as refresh gating:

- READOK
- WRT/
- WRTOK
- WRTOK/

The RØ-R3 outputs are used to generate Read Select signals (see Figure 2) while all 1Ø R outputs are used as Line Buffer load addresses (see Figure 2) and inputs to the DATARAM Read/Write Address Multiplexer. The S counter is a line counter, clocked by horizontal drive and cleared at the beginning of each vertical field by vertical drive. The least significant bit from the S counter (SØ) toggles to the opposite state with each input of the clock (horizontal drive). SØ toggles the Line Buffer Multiplexer (see Figure 2).

The DATARAM Read/Write Address Multiplexer selects either the 15 write address inputs or the 14 read address inputs and OE as a function of control signals WRTOK and WRTOK/.

The upper six bits of the DATARAM address bus are provided by the Read/Write Frame Load Latch. The Read and Write Frame Load control signals are used as latching signals by the Read/Write Frame Load Latch section. The address to be latched is supplied by the data bus.

The Q Counter (Figure 3) generates the Line Buffer unload (read) addresses. The only inputs to the counter are a horizontal drive (resets counter) signal and pixel clock. There are a total of 78Ø pixels/horizontal period but only 64Ø are stored and retrieved. Therefore, the 64Ø-pixel field should be centered on the display. To achieve this, the Q counter has an internal programmable delay which may be programmed to position the image as desired.

CONTROL AND HANDSHAKE

Figure 4 is a Functional block diagram of the Control and Handshake Section.

CONTROL

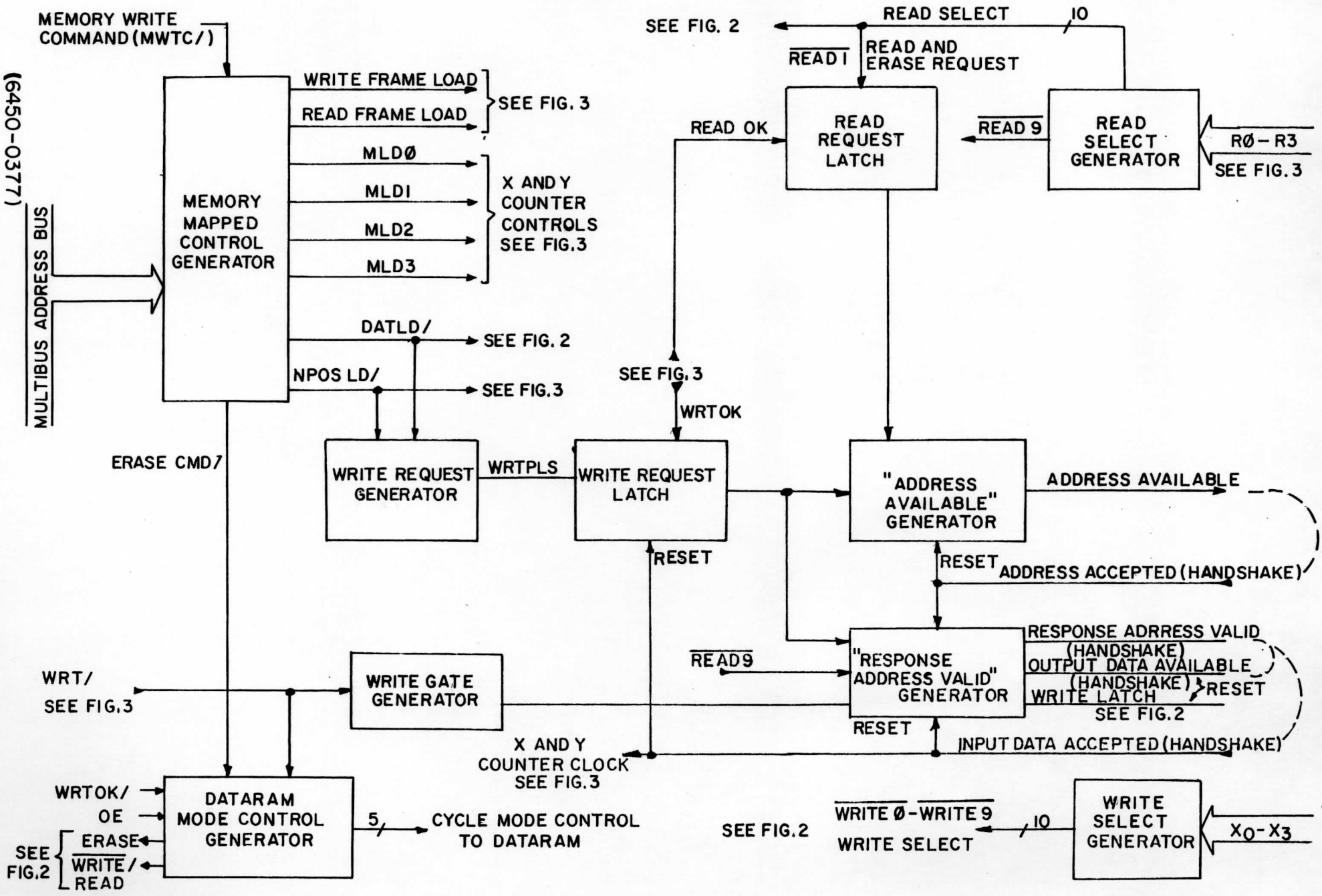
Memory-Mapped Control Generator

The Memory-Mapped Control Generator consists of two PROMS, driven by the entire Multibus address bus. This section also contains a programming carrier which encodes the unit number (unit Ø, 1, or 2). This section produces nine memory-mapped output signals. Signals MLODØ - MLD3 preload the X and Y counters. The Read and Write Frame Load commands are latch enables for latching the frame address (see Figure 3). Signal DATLD/ (Data Load) latches new pixel partition data into the Data Latch (see Figure 2). Signal NPOSLD/ (Next Position Load-active low) activates the X and Y counter memory-mapped Mode Control Generator. Signal ERASE CMD/ (Erase Command) is an input to the DATARAM Mode Control Generator. This signal initiates a frame erase cycle.

DATARAM Mode Control Generator

The DATARAM has several modes of operation. A 32-bit unit can do 16-bit as well as 32-bit data reads, writes, or data read/modify/writes (R/M/W). A total of five cycle mode control signals determine the mode of operation. Four of these lines are driven physically from the same source on the SSEC DATARAM CONTROL board, thus limiting the number of modes used to the following three:

- 32-bit data read (we use only 3Ø bits)
- 32-bit R/M/W
- 32-bit write (erase only)



CONTROL AND HANDSHAKE SECTION - FIGURE 4

The OE signal is used as a clock by the generator to synchronously gate an ERASE CMD/ signal. This causes an erase process to begin only in synchronism with the beginning of a frame field. When the generator is in the erase mode, it effectively replaces the 3Ø-bit data read cycles with 3Ø-bit erase write cycles. Thus 64 words (64Ø pixels) are cleared during each horizontal drive period. This allows an entire frame to be cleared in a single frame period (.033 sec). The $\overline{\text{WRITE}}$/READ signal controls the Bidirectional Bus Driver (see Figure 2). When $\overline{\text{WRITE}}$/READ is high, the driver is in the read mode.

Write Select Generator

The Write Select Generator decodes the BCD inputs ($X_Ø$-X_3) into ten Write Select lines. Each line controls a pixel partition in the Write Data Selector (see Figure 2).

Read Select Generator

The Read Select Generator operation is identical to the Write Select Generator. Because the Read Select Generator is always running, it is a convenient source of cyclic timing waveforms. For example, READ9/ is used by the Response Address Valid Generator and READ1/ is used by the Read Request Latch. Primarily, the Read Select Generator Signals (READØ/ - READ9/) gate the read data pixel partitions onto the Read Bus (see Figure 2).

HANDSHAKE

All remaining blocks in Figure 4 constitute the Multibus side of the handshake system. As explained earlier, the DATARAM Mode Control Generator establishes the mode of operation (read, write or R/M/W) and must be set up before a read, write or R/M/W cycle.

Address Available Generator

All cycles begin by generating the handshake signal ADRAVN (Address Available). The Address Available Generator produces this signal when triggered by the Read Request Latch during read cycles or the Write Request Latch during Write and R/M/W cycles.

Read Request Latch

The output of the Read Request Latch initiates read cycles. Control signal READOK gates request signal READ1/ into the latch.

Write Request Generator

When writing pixels into an image frame, the last setup operation performed is latching the pixel partition data into the Data Latch (see Figure 2). DATLD/ is the latching signal and is also an input to the Write Request Generator. Thus, the action of latching the partition data also prompts a Write Request. When writing pixels to a graphics frame, the Next Position Load (NPOSLD/) command is normally the last setup operation and also initiates a Write Request.

Write Request Latch

The Write Request Latch latches the request signal from the Write Request Generator and prompts the Address Available Generator at the proper time (determined by signal WRTOK).

Response Address Valid Generator

After the ADRAVN signal is initiated by the Read or Write Request Latches, the signal remains on until turned off by the "Address Accepted" (ADRACN) response (a few nanoseconds). This response also initiates the beginning of the next handshake signal "Response Address Valid" (RADVLDN).

RADVLDN is poorly named; it plays varying roles as a function of the mode. During a data read or R/M/W mode, the signal informs the DATARAM that the Multibus is ready to accept the requested input data. During a data write mode, the signal informs the DATARAM that the data on the 3Ø-bit data bus is valid. During an R/M/W cycle, "Response Address Valid" must go true twice. The first time is for the read portion of the cycle and operates as explained above; the second time is for the write portion of the cycle. In all cycles, the DATARAM responds within a few nanoseconds with either an "Output Data Available" (read or read portion of R/M/W cycle) or "Input Data Accepted" (write or write portion of an R/M/W cycle). Either of these signals resets the Response Address Valid Generator. For read or write cycles, this is the final handshake action. For R/M/W cycles however, a write cycle must be completed. To complete the

write cycle, another "Response Address Valid" command must be issued to inform the DATARAM that the "Write" data is ready (valid). When an R/M/W or Write cycle is initiated, the output of the Write Request Latch is passed to the Response Address Valid Generator. This signal functions as an "arming" signal which re-triggers the Response Address Valid Generator during the write portion of an R/M/W cycle. "Output Data Available" (normally a read cycle response) can go true during a requested write cycle only if the requested cycle is an R/M/W cycle at the end of its read portion. This signal is combined with the output of the Write Gate Generator to produce an "arming" signal gate; this re-triggers the Response Address Valid Generator for the Write portion of the R/M/W cycle. The DATARAM responds with "Input Data Accepted," used to reset the Write handshake logic and trigger the X and Y counters (write address counters - see Figure 3).

DETAILED CIRCUIT DESCRIPTION

The schematic diagrams of the DATARAM Control Board are shown on SSEC drawing #645Ø-Ø377 (Modification E, dated 4/23/84) sheets 1-1Ø. The schematic circuit analysis is accomplished by analyzing groups of components which represent single blocks on the respective functional block diagrams.

The SSEC circuit schematics are labelled by the column and row in which pin #1 of that chip resides. This is very helpful for troubleshooting, since the symbol ID is also the chip location; however, IC gates, flips-flops, buffers and inverters usually have several identical logic circuits packaged on the same IC. Therefore, when reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and a section identification letter. The symbol ID number alone is used to refer to single function ICs.

DATA FORMATTING

Refer to Figure 2 for the Functional block diagram of the Data Formatting Section. Most of the circuitry for this section is contained in sheets 1-4 of the schematics.

Bidirectional Bus Driver

The Bidirectional Bus Driver is made up of 1Ø Intel 8216 bidirectional bus driver chips. The 1Ø ICs which constitute the driver are: Y3ØX8, Y27X8, Y24X8, Y21X8, Y18X8, Y15X8, Y12X8, Y9X8, Y6X8 and Y3X8. The first four are located on sheet 1, the second four on sheet 2 and the last two are on sheet 3.

Each chip is capable of handling four bits but only three (bits Ø, 1, and 2) bits on each chip are used. Therefore, each chip handles one pixel partition. The control signal $\overline{\text{WRITE}}$/READ is paralleled to pin 15 (DIEN - Data In Enable) of each chip. When pin 15 is low (write), pins 4, 7, and 9 are connected to bidirectional bus pins 3, 6, and 1Ø respectively. When pin 15 is high (read), bidirectional bus pins 3, 6, and 1Ø are connected to pins 2, 5, and 11 respectively. For detailed information about the control signal, consult the Handshake and Control Section.

Read Data Modifier

The Read Data Modifier (see Figure 2) comprises ten 74LS157 data selector/multiplexer chips. The 1Ø ICs which make up this block are Y3ØX17, Y27X17, Y24X17, Y21X17, Y18X17, Y15X17, Y12X17, Y9X17, Y6X17 and Y3X17.

These ICs are distributed identically to those of the Bidirectional Bus Driver. Each of these chips have two 4-bit data sources and one 4-bit data output. Like the bus driver, only three bits are used and represent a pixel partition. Selection of the data source (A or B) to be channeled to the output (Y) is determined by the control signal applied to pin 1 of each chip. Data input signals (ØDATA, 1DATA, and 2DATA) are applied to the A input (pins 2, 5, and 11 respectively) of all 1Ø chips. The B input (pins 3, 6, and 1Ø) of each chip is driven by the Data Output Lines ($DO_Ø$, DO_1, and DO_2 respectively) of a corresponding bus driver chip. Thus, the B input of each 74LS157 is driven by a read pixel and the A input is driven by new data. A separate control line (WRITEØ/ - WRITE9/) drives each chip. For more information on the control lines, consult the Handshake and Control section. At present, it is sufficient to know that only one control line can be active low at one time. Therefore, if WRITE1/ goes low while a 3Ø-bit word is read in, the latched data (ØDATA - 2DATA) replaces the second pixel partition. At this time, pixels Ø and

3-9 pass from the respective Bidirectional Bus Driver chip to the Y output of the respective Write Data Selector chip. The latched input data appears at the Y output of Y27X17 only. The process just described happens in the Read/Modify portion of the Read/Modify/Write Cycle. During a read cycle, none of the Write Select Lines are allowed to go low, thereby passing all 1Ø partitions on to the Partition Read Latch and Selector block unmodified.

Write Data Latch

The output of the Read Data Modifier is presented to both the Write Data Latch (used in Write or R/M/W modes) and the Read Latch and Partition Separator blocks of Figure 2.

The Write Data Latch consists of five 8-bit latch chips (74LS273) located at Y15X37 (pixels Ø and 2), Y12X37 (pixels 1 and 3), Y9X37 (pixels 4 and 6), Y6X37 (pixels 5 and 7), and Y3X37 (pixels 8 and 9). The first two chips are located on sheet 1, the second two chips are on sheet 2 and the last chip is on sheet 3. The chips are clocked by control signal WRTLCH (Write Latch). These chips latch on the positive-going edge of the clock, while the data is present at the output of the Read Data Modifier. During a write cycle or the write portion of an R/M/W cycle, Bidirectional Bus Driver control signal $\overline{\text{WRITE}}$/READ goes low one pixel clock time after WRTLCH latches the data, gating the Write data onto the 3Ø-bit DATARAM bidirectional data bus. Note that all latch chips have the control signal ERASE/ applied to the clear inputs. Regardless of the input data, if ERASE/ is low, the latch outputs are all binary zeros. For more information on WRTLCH and ERASE, consult the Handshake and Control Section.

Read Latch and Partition Separator

The Read Latch and Partition Separator block of Figure 2 consists of ten 4-bit tri-state D-type register chips located at Y3ØX26, Y27X26, Y24X26, Y21X26, Y18X26, Y15X26, Y12X26, Y9X26, Y6X26, and Y3X26. These chips are distributed on sheets 1-3 in a manner identical to the Bidirectional Bus Driver and Read Data Modifier blocks, and are associated with pixels Ø-9 respectively. The tri-state control for these chips is pins 1 and 2. When both (or either) pins are high, the output is in a high impedance state, though input data can still be loaded and latched. The

output of each chip is connected to a common three-bit (pixel partition) Read Bus. Ten #3 pins, one from each of ten chips, are connected to form ØVID. Pins 4 and 5 do the same for 1VID and 2VID respectively. The 3Ø-bit word is parallel-loaded into the Read Latch and Partition Separator on the first rising edge of PXLCK, following an active low at the latch enable pin (pin 9). RDLCHEN/ (Read Latch Enable - active low) is parallel-connected to all 1Ø chips and is described in detail in the Handshake and Control section. As soon as the data is latched, any pixel can be output to the Read Bus by bringing that pixel's tri-state control pins (pins 1 and 2) low. Pins 1 and 2 of all 1Ø chips are driven by READØ/ - READ9/; they enable pixel partitions Ø-9 respectively. For more information on READØ/ - READ9/, see the Handshake and Control Section.

Data Latch

Input write data is supplied to the input Data Latch via the Multibus data bus bits DATØ - DAT2. The Data Latch is a single 74LS174, shown at the bottom of sheet 6 of the schematics. The latch is enabled by the memory-mapped control signal DATLD/. The output of the latch, ØDATA - 2DATA, is paralleled to the A input of the 1Ø Read Data Modifier chips.

Line Buffer Multiplexer

The Line Buffer Multiplexer, and Multiplexer Control sections are shown on sheet 4 of the schematic.

The Line Buffer Multiplexer performs two major tasks. First, it channels Read Bus data to the Write Buffer (off-line buffer) and channels the Read Buffer (on-line buffer) data to the output. Second, it connects the R counter outputs to the address inputs of the off-line buffer and connects the Q counter outputs to the address inputs of the on-line buffer. At the end of each horizontal line, the multiplexer must exchange the on-line and off-line buffers.

The output of NAND gates Y45X41-A and -B provides the control signals for the multiplexer. The NAND gates combine PXLCK, READOK, SØ, and SØ/ to produce WE1/ and WE2/. Note that PXLCK and READOK go to both NAND gates and that SØ/ goes to the A NAND gate while its complement (SØ/) goes to the B NAND gate. SØ is the LSB output of a horizontal line counter and therefore toggles to its opposite state at the beginning of each horizontal

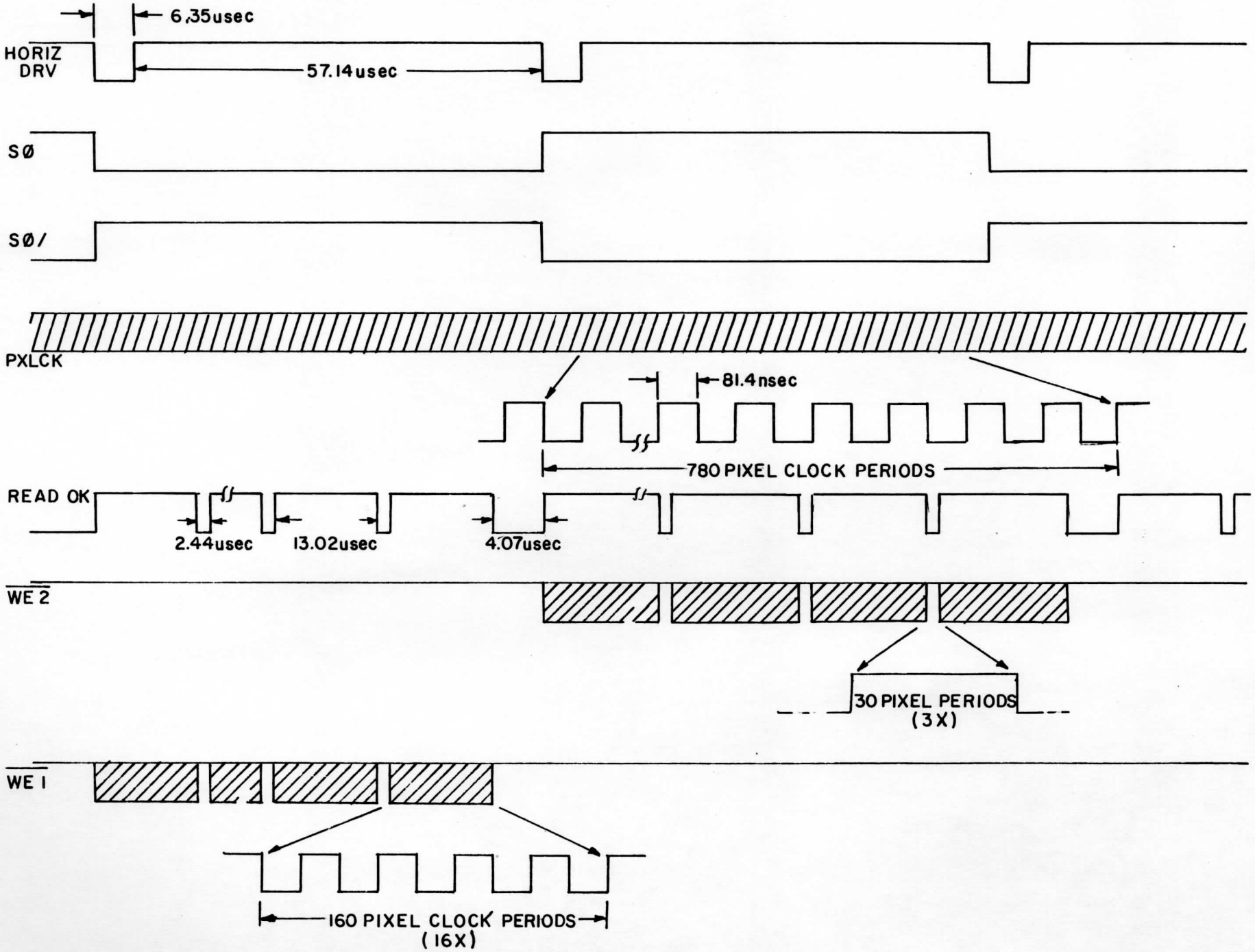
scan. Timing Diagram 1 shows the outputs of the NAND gates. The result of combining these waveforms is a gated pixel clock (PXLCK) which occurs only during read time. The gate that has a logic low at its SØ or SØ/ input has a steady high output while the other gate produces the READOK gated and inverted PXLCK. Signals WE1/, WE2/, SØ, and WE2 constitute the Buffer Multiplexer Control signals shown in Figure 2.

The Line Buffer Multiplexer shown in Figure 2 consists of tri-state octal buffer Y33X38, quad 2 input multiplexer Y39X37, and five quad 2 input data selectors Y3ØX37, Y27X37, Y24X37, Y21X37, and Y18X37. The Line Buffer consists of RAM chips Y33X38 and Y36X38.

The five data selectors function as the address switches for the buffer RAMS. The "load" addresses (RØ - R9) are applied to the A inputs of the selectors, which drive Y36X38, while the "unload" addresses ($Q_Ø$ - Q_9) are applied to the B inputs. The same signals are applied to the opposite inputs of those selectors which drive Y33X38. Since all selector chips are switched by SØ, one buffer is driven by R signals while the other is driven by Q signals. When SØ is low, the A inputs drive the corresponding buffer.

Refer to Timing Diagram 1. Pin 1Ø, the active low write enable input of the buffer RAMS, is driven by WE_1/ on RAM chip Y36X38 and by WE_2/ on RAM chip Y33X38. Note that WE_1/ is active when SØ is low. Thus, Y36X38 is in the Write mode (load) while the A inputs (RØ - R9) are driving the address lines. At the same time, Y33X38 is in the read mode and its address lines are driven by the $Q_Ø$ - Q_9 signals. When SØ goes high, the opposite signals drive the respective buffer address inputs and the buffers swap read/write modes.

Tri-state octal buffer Y33X38 functions as the "write" data switch while the quad 2 input multiplexer (Y39X37) functions as the "read" data switch. Y33X28 is organized as two quad buffer sets, each having a separate tri-state enable input. The multiplexer (Y39X37) uses SØ/ as the word select input. When SØ/ is low, A_1 - C_1 are gated to the output (Q_A - Q_C). When SØ/ is high, A_2 - C_2 are gated to the output. In summary, if SØ/ is low, WE_1/ is active, WE_2 is inactive low, RAM Y36X38 is in the "load" mode, RAM Y33X38 is in the unload mode, ØVID - 2VID are directed to RAM Y36X38, and RAM Y33X38 read data is selected by the multiplexer. Conversely, if SØ/ is high, input data (load) is directed to Y33X38 and "unload" (read) data from Y36X38 is selected by the multiplexer.



TIMING DIAGRAM 1 - LINE BUFFER MULTIPLEXER CONTROL
(6450-0337)

DATARAM ADDRESS AND LINE BUFFER ADDRESS GENERATOR

Refer to Figure 3 for the functional block diagram of the DATARAM and Line Buffer Address Generator sections. Most of the circuitry for this section is contained on sheets 5, 6, and 8 of the schematic diagrams.

DATARAM Write Address Generation Section

The circuitry for this section is shown on sheet 6 of the schematic. The 15 LSBs of the DATARAM write address are generated by the X and Y counters.

Y Counter Section

The Y Counter consists of three cascaded binary counters: Y72X39, Y69X39 and Y66X39. These 74LS191 counters are fully-programmable synchronous binary up/down counters featuring an asynchronous load. The data inputs to the counter are supplied by the Multibus data bus. Control signal MLD2/ is the pre-load strobe for Y72X39 and Y69X39 while MLD3/ serves the same purpose for Y66X39. Clock signal XYINC/ (XY Increment) is applied to all X and Y counter chips. These control and clock signals are covered in the Control Section. Mode control signal YDU (Y Down/Up) controls the direction of counting (incrementing or decrementing). Mode control signal YEN/ (Y Enable) enables (active low) or disables counting. YEN and YDU controls are generated by the Memory Mapped Control Generator (see Figure 4) located in the Control Section.

X Counter Section

The X Counter is similar to the Y Counter with the exception of the least significant counter chip and the data pre-loading scheme. The counter consists of Y72X48, Y69X48 and Y66X48. Y72X48, the least significant counter chip, is a BCD counter chip while the other two are binary counters. The ripple carry output from the BDC counter is used as the input to an eight-stage binary counter consisting of Y69X48 and Y66X48.

Since the overall counter counts in a combination of BCD and binary, preloading would be complicated (for programming) unless a binary-to-BCD/binary converter is incorporated. The converter consists of EPROM Y37X12 and latches Y6ØX32 and Y6ØX21. Control signal MLDØ, the latching signal for Y6ØX32 latches the eight least significant pre-load bits while MLD1/ pre-loads the two MSBs (Y6ØX21). The inputs to the latches are

supplied by the buffered Multibus data bus. The latched data, along with MLD2/ are used as address inputs to the EPROM. The EPROM, a 2716, functions as a look-up table. When MLD2/ is inactive high, the EPROM is switched to its BCD decode section and the four LSB output bits represent the BCD portion of the pre-load term. At this time, MLD3/ is brought active low, latching the BCD pre-load data into Y72X48. Next, the pre-load control (MLD2/) for the binary portion of the counter is brought low (MLD3/ returns to inactive high). The MSB address input to the EPROM is low, switching it to the binary decode section. The eight EPROM output bits now contain the pre-load data for the binary portion of the counter. Note that MLD2/ acts as both the EPROM MSB input and the pre-load control for the binary portion of the counter. Mode control signals XEN/ and XDU are generated by the Mode Control Generator which also generates the Y Counter mode controls. The X and Y counters use the same clock (XYINCR/). As explained in the Functional Description Section, data is written into memory in the R/M/W mode of the DATARAM, one pixel partition (three bits) at a time. X Counter output bits XØ-X3 (BCD portion) are used as the pixel partition address since 1Ø pixel partitions reside at each word address. This is the reason for a BCD counter chip in the X Counter. X Counter output bits X4-X9 form the five LSBs of the word address (Ø-63). Therefore, the X Counter provides the addressing of any pixel on a 64Ø pixel horizontal line. The nine-bit Y address generator output (YØ-Y8) allows a full count of 512, the number of horizontal lines in a frame. Thus, the Y Counter addresses the horizontal line.

Mode Control Generator

The Mode Control Generator consists of data latch Y65X3Ø and PROM Y63X48. The latch is driven by DATØ-DAT2, the three LSBs of the buffered Multibus data bus. The latch is controlled by control signal NPOSLD/, generated by the Memory Mapped Control Generator, located in the Control Section. The four PROM outputs are used as mode (up/down) and enable control signals for both counters. The table below shows the inputs, outputs, and meanings of the PROM.

Data Input (binary)	Data Output (binary)	Results
ØØØ	1ØØØ	Y disabled, X counts up
ØØ1	1ØØ1	Y disabled, X counts down
Ø1Ø	Ø1ØØ	Y counts up, X disabled
Ø11	Ø11Ø	Y counts down, X disabled
1ØØ	ØØØØ	both count up
1Ø1	ØØØ1	X counts down, Y counts up
11Ø	ØØ1Ø	X counts up, Y counts down
111	ØØ11	both count down

If the CPU is directed, under firmware control, to write a zero to the address assigned to NPOSLD/, the Y Counter is disabled and the X Counter is in a count-up mode. Until changed by a new mode command, the X counter increments each time an active low clock pulse (XYINCR/) is received.

DATARAM Read Address Generation Section

The circuitry for this section is shown on sheet 8 of the schematic. The 15 LSBs of the DATARAM read address are generated by the R and S Counter.

R Counter Section

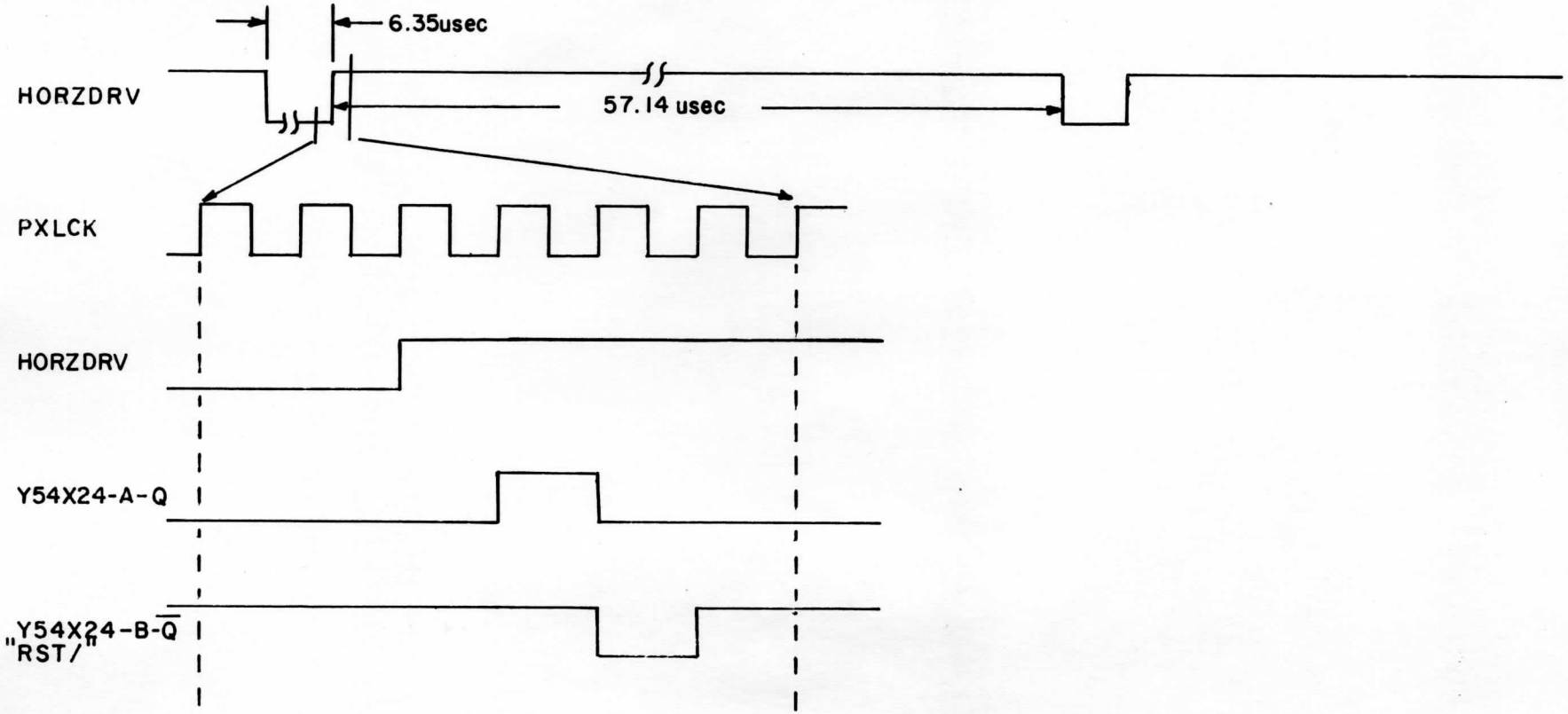
The R Counter is shown on the bottom third of sheet 8 of the schematic diagram. As explained in the Functional Description, the counter not only produces address inputs used for DATARAM "reads," it also produces many primary control signals used in refresh and write timing. The counter essentially generates four repeating timing cycles. A timing cycle consists of addressing 16Ø consecutive pixel partitions (16 word times), followed by a 1Ø-pixel-wide refresh cycle (1 word time) and concluded with a 2Ø-pixel-wide R/M/W cycle (2 word times). Therefore, a timing cycle is 19 word times in length and is referred to as a 19X cycle (where X = one word time = Ø.814 μsec). The fourth cycle is slightly longer (21X) than each of the first three cycles, but is still referred to as a 19X cycle.

The primary components of the R Counter are BCD counter Y42X48 and binary counters Y48X48 and Y36X48. The only external drive signals to the counter are horizontal drive (HORZDRV) and pixel clock (PXLCK). All 19X cycle waveforms are produced by controlling the counter enables and clear inputs. HORZDRV is a master clear for the counter. PXLCK is the 12.285-Mhz clock applied to all R counter chips.

HORZDRV is applied to a positive-edge detector consisting of data latches Y54X24-A and -B. The static conditions of the A and B sections are set and reset respectively. Refer to Timing Diagram 2. The rising trailing edge of HORZDRV latches a "one" into the Q output of section A. Since the B section is clocked by PXLCK, the first rising edge of PXLCK following a high input from section A causes the Q/ output of section B to go to "zero". The Q/ output of section B acts as the reset for the counters and Y54X24-A. Since a 74LS74 features an asynchronous clear, the Q output of section A returns to "zero" a few nanoseconds after the Q/ output of section B goes to zero. This places a "zero" input to the B section; the next PXLCK returns the Q/ output of section B to a "one". Thus, the reset is one PXLCK period long.

Y42X48, the BCD counter, counts continuously between reset pulses. The ripple carry output (pin 15) is applied to triple input AND gate Y42X39-C. The ripple carry is active high while the counter has an output of 9 (1ØØ1B). The other two inputs to Y42X39-C are the inverted ripple carries from both binary counters.

These counters have an active high ripple carry any time they are at their maximum count (15D or 1111B). Therefore, the BCD counter's ripple carry output is allowed to pass to the first binary counter as long as neither binary counter is at a full count. Since counter Y39X48 increments only once for each 1Ø count cycle from the BCD counter, the ripple carry output from Y39X48 goes high on the $15Ø^{th}$ count (1Ø•15), disabling AND gate Y42X39 and providing a high input to pin 5 of AND gate Y42X39-B. The ripple carry of the BCD counter and the inverted ripple carry from counter Y36X48 are also applied to AND gate Y42X39-B. Thus, the ripple carry outputs from the BCD counter are now channeled into counter Y36X48. When the BCD counter output goes to 9 (total count = 159), counter Y36X48 is enabled. The next clock pulse overflows the BCD counter to "zero" and increments Y36X48 to a count of "one" (QA active high). Counter Y39X48



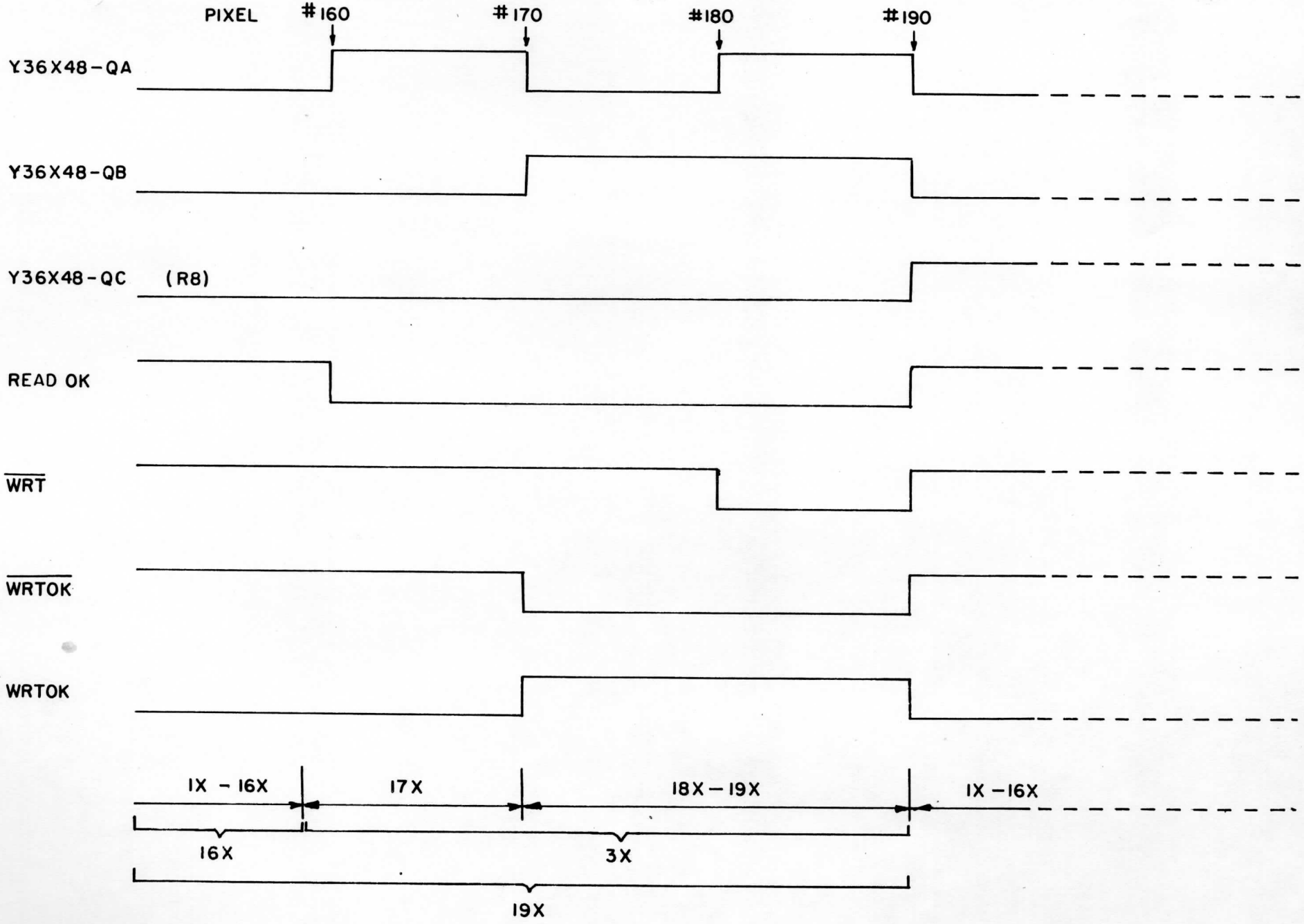
TIMING DIAGRAM-2 "R" COUNTER RESET

(6450-0377)

does not change and still has a high ripple carry output. At this time, RØ-R9 indicate a count of 15ØD. The BCD counter repeats the cycle with counter Y36X48 incrementing to "two" (QB active high). Again, RØ - R9 count from 15Ø-159 and reset to 15Ø. The BCD counter repeats its cycle again, incrementing Y36X48 to "three" (QA and QB active high) and the RØ-R9 output cycles from 15Ø through 159 and back to 15Ø. Note that, at this time, pins 2 and 13 of AND gate Y42X49-A are qualified. When the BCD counter reaches a count of 9 and generates a ripple carry output, counter Y36X48 increments to "four" (QC active high) and AND gate Y42X39 is qualified, resetting counter Y39X48. The RØ-R8 outputs indicate a count of 16Ø ($1Ø \cdot 2^4$).

In summary, RØ-R9 count normally from Ø-159, reset to 15Ø, count up to 159, reset to 15Ø, count to 159, reset to 15Ø, count up to 159, reset to 15Ø, and count up to 16Ø. The three partial resets require 3Ø pixels to increment from 159 to 16Ø. This completes one 19X cycle (19Ø pixels or 19 word times). This process repeats four times in each horizontal cycle.

QA and QB outputs of counter Y36X48 provide a convenient source of timing signals for the refresh and R/M/W cycles. Timing diagram 3 shows the relationships between READOK, WRT/, WRTOK/, Y36X48-QA and -QB, and the 19X cycle. Inverters Y45X39-D and Y48X4Ø-F and AND gate Y42X31-C function as a negative logic NOR gate and produce an inactive low output if QA, QB, or both QA and QB are active high. The output of this gate is READOK. Before the generation of WRTOK/ and WRT/ is explained, J-K flip-flop Y45X48-A should be addressed. Remember that the 4th 19X cycle is actually 21 word lengths long. At the end of the 19th word, counters Y36X48 and Y39X48 both have full counts of 15D (1111B). Therefore, the ripple carry from both counters is active high, preventing any further counting by these counter stages, because AND gates Y42X39-C and Y42X39-B are both disqualified. Until a new master reset (RST/) is received, the only counter chip which continues to count is Y42X48 (counts from Ø-9 and overflows back to zero). Therefore, QA and QB outputs from Y36X48 both remain active high for two word times (2Ø and 21) longer than normal. The purpose of flip-flop Y45X48 is to terminate WRTOK/ and WRT/ at the end of 19X on the fourth cycle in each horizontal time. To accomplish this, the K input is driven by RST/ and is low for only one pixel clock period during the master reset. During the master reset, all counters go to zero



TIMING DIAGRAM 3 - R COUNTER-CYCLE RESET

(6450-0377)

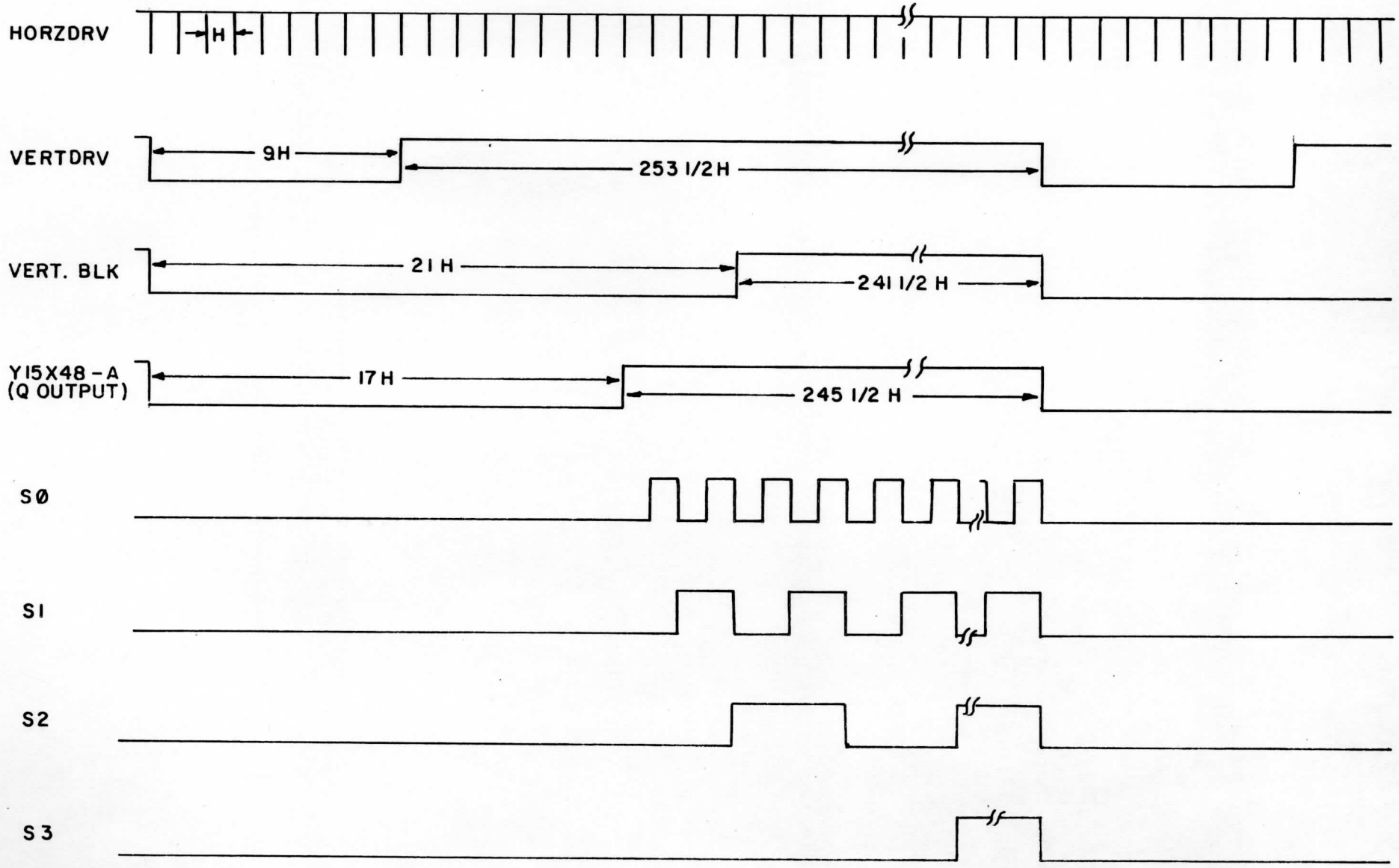
and AND gate Y42X41-B is disqualified, placing a low on the J input of the flip-flop. Now, when the next rising edge of PXLCK arrives (coincident with trailing edge of RST/) the flip-flop resets, placing a high on the Q/ output. When both Y36X48 and Y42X48 generate coincident ripple carries (end of 19Øth pixel of 4th cycle only), AND gate Y42X31-B places a high on the J input (the K input is also high). On the next PXLCK clock cycle, flip-flop Y45X48-A sets, placing a zero on the Q/ output. Since the Q/ output is NANDed with QA and QB, WRT/ and WRTOK/ are always 1X and 2X in duration, respectively, regardless of which 19X cycle is being generated.

Since RØ-R3 are BCD outputs, they are used to select the pixel partitions within a 3Ø-bit word, while outputs R4-R9 are used to address the words in a horizontal line (Ø-63). RØ-R9 are used to address the Line Buffers (Write Address Bus - see Figure 2).

S Counter Section

The S Counter Section is used as the horizontal line address generator. It is shown at the top of sheet 8 and consists of binary counters Y6X48, Y3X48 and Y9X48 and J-K flip-flop Y15X48-A. The actual counter consists of Y6X48 and Y3X48. Counter Y9X48 and J-K flip-flop Y15X48-A form an eight-horizontal-scan delay which centers the image on the display screen.

To understand the need for the delay, a brief review of the TV timing waveforms may be useful (see Timing Diagram 4). First, let's review VERDRV. This signal goes low at the beginning of each 262.5-horizontal-line field and stays low for nine horizontal scans. Next, there is a vertical blanking signal (part of composite blanking) which blanks the CRT for 21 horizontal scans, beginning with the start of VERTDRV. Thus, there are 12 horizontal lines blanked between the time that VERTDRV goes high and the end of the vertical retrace blanking period. VERTDRV is used as a pre-set for counter Y9X48 whose MSB preset input is tied high. Note that VERTDRV is used to clear the flip-flop. Therefore, VERTDRV causes counter Y9X48 to preset to a count of eight and flip-flop Y15X48-A to clear, causing counters Y6X48 and Y3X48 to clear. Seven horizontal drive pulses are required (after VERTDRV goes high) for Y9X48 to reach a full count and generate a ripple carry out. The eighth HORZDRV pulse sets Y15X48-A and removes the clear pulse from Y6X48 and Y3X48. Therefore, the S counter



TIMING DIAGRAM 4 -"S" COUNTER
(6450-0377)

begins counting with the 9th HORZDRV pulse following the positive-going edge of VERTDRV. Inserting the eight-horizontal-line delay moves the image down, reducing the number of blanked data lines from 12 to four. Once the clear is removed from the counter, it counts each horizontal drive pulse until it is cleared again by the flip-flop. The counter reaches a maximum count of about 245 decimal.

Q Counter

The Q Counter generates the Line Buffer Read Address Bus (see Figure 2). The Q counter is a BCD counter whose ripple carry output drives a six-bit binary counter. The BCD counter is counter chip Y33X48 and the binary counter consists of counter chips Y3ØX48 and Y27X48. All counter chips are clocked by PXLCK. The "clear" input of counters Y33X48 and Y3ØX48 is connected to the pre-set input of counter Y27X48 and driven by VIDEN (video enable - AND gate Y54X32-D). Thus, when VIDEN goes low, the counter is preset to a count of 192ØD (full count = $1Ø \cdot 2^8$ = 256Ø). Therefore, the counter develops a one-pixel-wide ripple carry on the 64Øth count of PXLCK.

There are 648 visible pixels (plus or minus a few) in each horizontal line (132 are blanked by horizontal blanking), but only 64Ø pixels of data. An adjustable delay, consisting of binary counters Y21X48 and Y18X48, programmed by carrier Y24X48, allows the image to be centered on the screen. The nominal delay for image units is 53 pixels while for graphics it is 55. The slight difference is due to differences in channel processing delays. Both channels have inherent delays of about 8Ø pixels. Thus, the total delay is about 133-135 pixels, slightly more than enough to prevent display of data during the blanking period and thereby centering the image.

The ripple carry output from the delay counter (pin 15 of Y18X48) is applied to the J input of J-K flip-flop Y15X48-B. The K input of this flip-flop is driven by the inverted ripple carry output of the Q Counter and remains high until the terminal count of the Q Counter and (64Øth pixel) is reached. Therefore, when the J input of Y15X48-B goes high and a rising edge of PXLCK occurs at the clock input, the flip-flop sets, bringing VIDEN high and enabling the Q Counter. The flip-flop remains set until the Q Counter ripple carry output causes the K input of Y15X48-B to

go low. When this happens, the flip-flop resets on the next clock pulse because the J input is also low. Therefore, the signal VIDEN is active high and 64Ø pixels long, centered in the unblanked horizontal scan time. VIDEN is applied to latch Y51X4Ø-A, which is clocked by PXLCK. Thus, the output of Y51X4Ø-A (VIDENA) is identical to VIDEN but delayed by one PXLCK period (81.4 nsec). VIDENA gates the Line Buffer partition data to the output line drivers (see Y54X32 and Y57X8 on sheet 4).

DATARAM Read/Write Address Multiplexer

The DATARAM Read/Write Address Multiplexer is shown on sheet 5 of the schematic diagram. The multiplexer consists of inverting tri-state octal bus drivers Y48X21, Y48X1Ø, Y51X21, and Y51X1Ø. The X and Y write addresses are applied to Y48X21 and Y51X21 enabled by WRTOK/ (WRTOK/ is shown in Timing Diagram 3). The R and S read addresses are applied to Y48X1Ø and Y51X1Ø, enabled by WRTOK.

Momentarily, let's focus our attention on S8, the A7 input of Y41X1Ø. S8 is generated on sheet 8 of the schematic. The signal OE (Odd/Even) originates on the TV Timing and Colorizer board. It has a frequency of 6Ø hz and is always active high during the first field of every frame. The bipolar output of the line drivers on the TV Timing and Colorizer board are applied to the inputs of line receiver Y54X8-D. Note, however, that the inverted drive is applied to the non-inverting input of the receiver while the non-inverted drive is applied to the inverting input. Thus, S8, the output of Y54X8-D is inverted and is <u>low</u> during the first field of each frame.

S8 forms the 7th LSB of the read address. The six LSBs form the word address for each horizontal line of data (Ø-63). Remember that RØ-R3 are used to address the pixel within each word. Since S8 remains low for the entire first field (256½ lines), data is read from every other 64-word block. For example, assume we are reading a frame (even and odd field) which begins at address ØØØØØØH. We read words Ø-63, 128-191, 256-319, 384-447, ...3Ø,72Ø - 3Ø,783. Now, S8 goes high (second field) and all R and S address lines reset to "zero". This time, we address 64-127, 192-255, 32Ø-383, ...3Ø784-3Ø847. Thus, we read out of memory in an interleaving fashion. Therefore, the data must be written in an identical manner. During data storage, the pixels are converted to partitions and

written into memory one partition at a time. When a line (64 words), is completed the X and Y addresses are re-indexed so that the next line will be in the proper 64-word block for interleaved data read out.

Read/Write Frame Load Latch

The Read/Write Frame Load Latch section is shown on the top half of sheet 5 of the schematics. Refer to sheet 6. The Multibus data bus enters the board from the P1Ø connector and is inverted by inverting tri-state octal buffer Y69X1Ø. The non-inverted data bus is applied to another tri-state inverting octal buffer (Y51X32) located on sheet 5.

The inverted data bus (DATØ/ - DAT7/) is applied to Write and Read Frame Latches (Y45X21 and Y45X1Ø respectively) which are latched by corresponding memory-mapped control signals WRITE FRAMLD/ and READ FRAMLD/. For more information on these control signals, see the Control and Handshake Section. The latched outputs are placed on the ADDR15/ - ADDR2Ø lines by enabling one of the latch's tri-state controls. The write and read latches are enabled by WRTOK/ and WRTOK respectively. For more information on these signals, see the R Counter description and/or Timing Diagram 3.

WRITE FRAMLD/ is applied directly to Y45X21 via inverter Y57X32-D. READ FRAMLD/ is applied to Y45X1Ø via data latch Y51X4Ø-B, inverter Y57X32-B, and AND gate Y42X31-D. Since READ FRAMLD/ is inactive high at all times except during an actual frame address load, and is applied to both the D input of Y51X4Ø-B and the inverter, AND gate Y42X31-D normally has both inputs low. When READ FRAMLD/ goes active low, pin 13 of the AND gate is qualified immediately by the inverter output. The CPU continues to hold READ FRAMLD/ low until it receives a transfer acknowledge (XACK/) or times out. Latch Y51X4Ø is clocked by the rising edge of WRTOK which occurs at the end of a 19X cycle (same as the beginning of the next 19X cycle, the beginning of the 16-word read section). The rising edge of WRTOK latches the active low D input, causing the Q/ output (pin 8) to go high. This qualifies the AND gate, latching the Read Frame Latch and initiating the XACK/ response. Thus, a new Read Frame Load command is processed only at the beginning of a 19X cycle.

THE CONTROL AND HANDSHAKE

The circuitry for this section is contained primarily on sheets 7 and 9 of the schematic diagrams. Figure 4 is the functional block diagram for this section.

Control Section

Memory Mapped Control Generator

The entire Multibus address bus is applied to two PROMs, via two octal buffers, for address decoding (refer to sheet 7). This section decodes the address mapped control signals into one of three sets of controls. The particular set of controls is a function of the unit number (Ø, 1 or 2). A board produces one of the following sets of control signals: FCØ1H - FCØ9H, FC1ØH - FC19H, or FC2ØH - FC29H. The particular set is selected by carrier Y57X16, as explained in the next paragraph.

Multibus address lines ADR5/ - ADRC/ are applied to buffer Y63X1Ø, whose outputs drive A1-A8 of PROM Y66X21. AØ of the PROM is driven by ADR4/ via buffer Y66X1Ø. The function of PROM Y66X21 is to "activate" PROM Y63X21 by placing a logic low on A8 of PROM Y63X21. PROM Y66X21 screens out all binary addresses which do not meet the criteria: XXX1 11ØØ ØØAA XXXX, where X = don't care and AA = unit code (ØØ = unit Ø, Ø1 = unit 1, and 1Ø = unit 2). Address XXX1 11ØØ ØØØØ XXXX generates a low at pin 12 (O_1), XXX1 11ØØ ØØØ1 XXXX generates a low at pin 11 (O_2), and XXX1 11ØØ ØØ1Ø XXXX generates a low at pin 1Ø (O_5). Carrier Y57X16 selects one of the active low outputs and passes it on to PROM Y63X21. As an example, assume this is unit 1. Pin 2 of the carrier is jumpered to pin 13, providing a low to PROM Y63X21 for addresses XXX1 11ØØ ØØØ1 XXXX only.

All of the active low outputs from PROM Y63X21 occur in the first (lowest addressed) 32 words in memory. Therefore, to address this area, A5-A7 of PROM Y63X21 must be "zero"s. Since these inputs are driven by the inverted address lines ADRE/ - ADRF, the corresponding non-inverted address lines must be all "one"s. Therefore, the only addresses that can produce control signals are FCØXH, FC1XH, and FC2XH, where X = don't care. ADRØ - ADR3/ are decoded by PROM Y66X21 to produce the following active low outputs:

O_1 = FCX1 - FCX7

O_2 = FCX8 - FCX9

O_3 = FCX1 - FCX9

where X = unit number (Ø, 1 or 2 for graphics, image #1 or image #2 respectively)

Output O_1 (PARLD/) is further decoded by 3-to-8 line decoder Y69X3Ø, O_2 (GLOAD/) is further decoded by 2-to-4 line decoder Y66X3Ø, and O_4 (STBGEN/) initiates the transfer acknowledge and limits the duration of the Y66X3Ø outputs.

PARLD/ enables 3-to-8 line decoder Y69X3Ø. Inverted address lines ADRØ - ADR2/ are uninverted by inverters Y67X32-A, -B and -C and applied to the A, B and C inputs of the 3-to-8 line decoder. The decoder provides five memory-mapped outputs, defined as follows:

Output	Address	Control (see sheet 7 except as noted)
Y_1	FCX1	WRITE FRAMLD/ (see sheet 5)
Y_4	FCX4	MLDØ/ 8 LSB X Counter Preload Latch
Y_5	FCX5	MLD1/ 2 MSB X Counter Preload Latch
Y_6	FCX6	MLD2/ X and Y Counter binary load strobe
Y_7	FCX7	MLD3/ X Counter BCD load strobe

STBGEN/ is normally high and is applied to the 1D input of quad D latch Y72X3Ø. This latch is clocked by PXLCK and results in a low at 1Q/ and 2Q/, and a high at 1Q and 2Q (note that output 1Q is connected to the 2D input). Thus, NAND gate Y51X48-A is normally disqualified (high), forcing a high at OR gate (shown as inverted input NAND gate) Y6ØX4Ø-D. Since STBGEN/ goes low when either PARLD/ or GLOAD/ goes low, assume GLOAD/ went low, qualifying the pin 12 input of the OR gate. At this same time, the 1D input of the latch is also low. On the rising edge of the next PXLCK, 1Q/ goes high, qualifying NAND gate Y51X48-A and placing a qualifying low at the pin 13 input of the OR gate. The OR gate now produces a low output, enabling 2-to-4 line decoder Y66X3Ø. This decoder is qualified

for one PXLCK only, because the next PXLCK latches a "zero" into the 2Q output of Y72X3Ø, disqualifying NAND gate Y51X48-A and OR gate Y6ØX4Ø-D. At this time, latch output 2Q/ is high, enabling NAND gate Y61X48-C (pin 1Ø input was already high, as we will see later). The low outputs of Y51X48-C and STBGEN/ produce a low at the output of OR gate Y57X57-A, causing pin 12 of AND gate Y57X4Ø to go low (XXACK/). XXACK/ is applied to line driver Y57X8-D, where it becomes XACK/, the transfer acknowledge signal. When PARLD/ goes low, the XACK/ is generated in an identical manner, however, the 2-to-4 line decoder never qualifies.

In the previous paragraph, we saw how XACK/ was generated and how the 2-to-4 line decoder Y66X3Ø becomes enabled. Now, we will see how GLOAD is decoded. The decoder is enabled by GLOAD/ (FCX8 or FCX9) for one PXLCK pulse. Note that ADRØ is applied to the A input and UNITØ/ (O_1 output of PROM Y66X21) drives the B input. The B input is low for unit Ø addresses. Therefore, $Y_Ø$ and Y_1 outputs of the decoder are used by graphics units and Y_2 and Y_3 are used by image units. ADRØ/ is used to separate those addresses ending in "8" (Y_0, Y_2) from those ending in "9" (Y_1, Y_3). The four Y outputs from Y66X3Ø are applied to three inverting input NOR gates (Y57X48-A, -B and -C). Gate A combines Y_1 and Y_3 (addresses ending in 9), gate C combines Y_0 and Y_3 (addresses ending in 8) and gate B combines Y_0 and Y_3 to produce WRTSTRT/ (Write start). The output of the gates are summarized as follows:

GATE	ADDRESS	UNIT	2-4 OUTPUT	SIGNAL
Y57X48-A	FCØ9, FC19, FC29	Ø, 1, 2	Y_1, Y_3	DATLD/
Y57X48-B	FCØ8, FC19, FC29	Ø, 1, 2	$Y_Ø$, Y_3	WRTSTRT/
Y57X48-C	FCØ8, FC18, FC28	Ø, 1, 2	$Y_Ø$, Y_2	NPOSLD/

WRTSTRT/ initiates the request for an R/M/W cycle. Therefore, all required setup steps (address, X and Y counter modes, data loading etc.) must be completed prior to any action which generates a WRTSTRT/. As shown above, WRTSTRT/ is initiated by a NPOSLD/ to unit Ø (graphics) or a DATLD/ to units 1 or 2 (image). A DATLD/ to units 1 or 2 or a NPOSLD/ to unit Ø are the final CPU action in a pixel storage activity. DATLD/ is

the latching signal used to latch a three-bit data partition into the Data Latch (see Figure 2 and sheet 6 of the schematic). When loading an image, three-bit data partitions are stored consecutively within a 3Ø-bit word; each 64-word packet, which makes up a horizontal line, is consecutive. Once set up, the X and Y address counters automatically index to the next address each time a partition is written (the Y counter is indexed at the end of each horizontal line of data). This means that writing the next pixel, to units 1 or 2, is initiated by DATLD when the pixel partition is latched.

Since the data, which is written into a graphics frame, is generally constant (points of equal intensity which form lines etc.), the data is written initially by doing a DATLD/ command. Thereafter, a new pixel is written automatically by doing a NPOSLD/. NPOSLD/ is used to latch X and Y counter mode controls (see Figure 3 and sheet 6 of the schematics). Note that several other commands (MLDØ/ - MLD3/) may be required before actually performing the NPOSLD/ command.

The two signals from the Memory-Mapped Control Generator that have not been addressed yet are READ FRAMLD/ (Read Frame Load) and ERASE CMD/ (Erase Command). These signals are developed by PROMs Y72X21 and Y69X21, and carrier Y57X16. Y72X21 is driven by the eight MSBs of the Multibus address bus and is programmed to produce an active low at output O_1 for addresses FCØØH - FCFFH only. The active low from Y72X21 drives the MSB input of PROM Y69X21. The lower eight address inputs of PROM Y69X21 are driven by the eight LSBs of the Multibus address bus. PROM Y69X21 is programmed to produce active outputs for the following four addresses only:

- O_1 = FCØØH
- O_2 = FC1ØH
- O_3 = FC2ØH
- O_4 = FCØ3H

The outputs are applied to the unit programming carrier (Y57X16) where O_1, O_2, or O_3 are selected for the READ FRAMLD/ command. If this is unit Ø (graphics unit), pin 7 of the carrier also is connected to pin 8 and is used as the ERASE CMD/ signal. Thus, only unit Ø can be erased. Also note that the erase command is used as an input to the XACK/ generator.

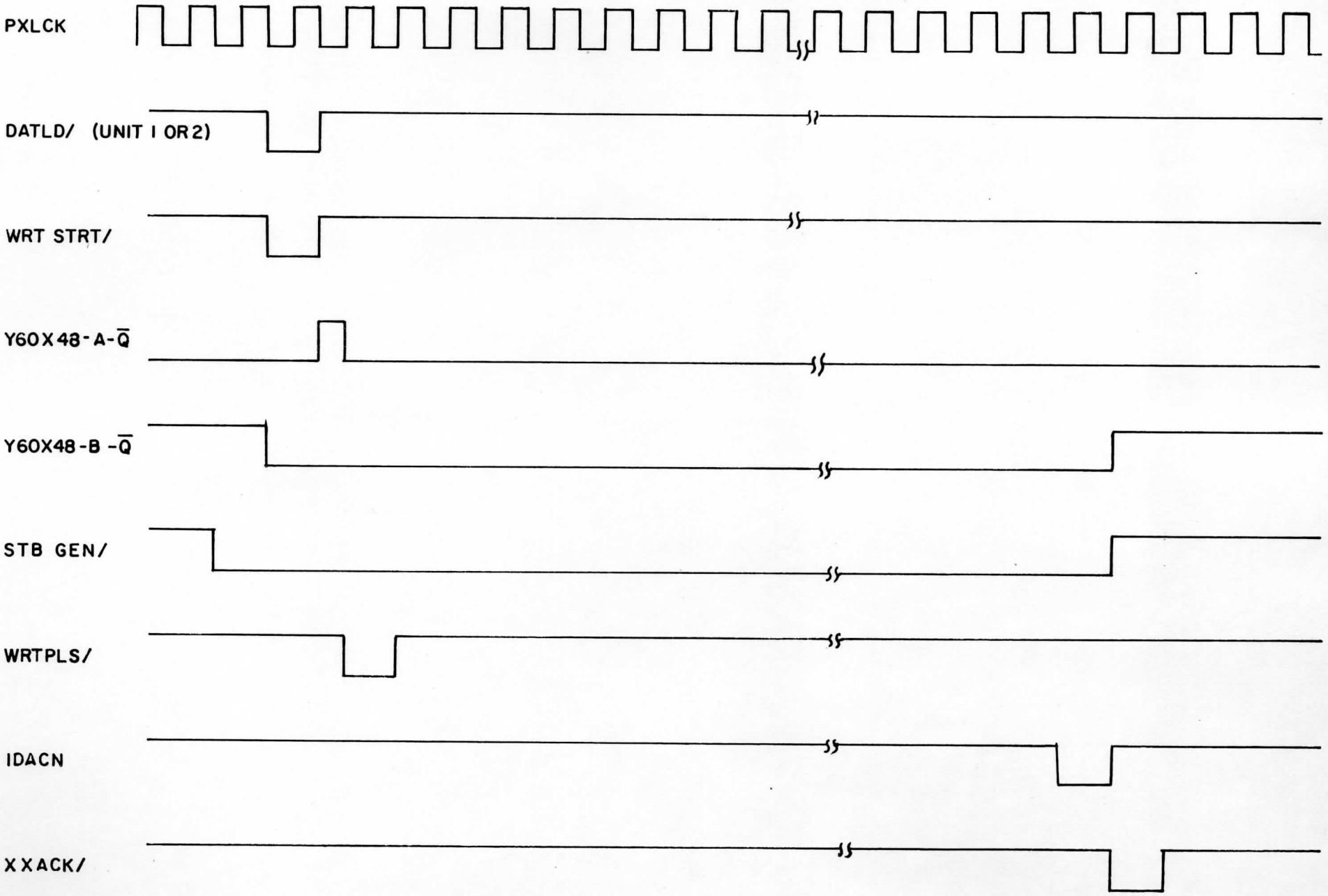
Table 1, below, summarizes the outputs from the Memory-Mapped Control Generator.

FCØØ = READ FRAMLD/	unit Ø
FCØ1 = WRITE FRAMLD/	unit Ø
FCØ2 = Not used	
FCØ3 = ERASE CMD/	unit Ø
FCØ4 = MLDØ/	unit Ø
FCØ5 = MLD1/	unit Ø
FCØ6 = MLD2/	unit Ø
FCØ7 = MLD3/	unit Ø
FCØ8 = NPOSLD/, WRTSTRT/	unit Ø
FCØ9 = DATLD/	unit Ø
FC1Ø = READ FRAMLD/	unit 1
FC11 = WRITE FRAMLD/	unit 1
FC12 = Not used	
FC13 = Not used	
FC14 = MLDØ/	unit 1
FC15 = MLD1/	unit 1
FC16 = MLD2/	unit 1
FC17 = MLD3/	unit 1
FC18 = NPOSLD/	unit 1
FC19 = DATLD/, WRTSTRT/	unit 1
FC2Ø = READ FRAMLD/	unit 2
FC21 = WRITE FRAMLD/	unit 2
FC22 = Not used	
FC23 = Not used	
FC24 = MLDØ/	unit 2
FC25 = MLD1/	unit 2
FC26 = MLD2/	unit 2
FC27 = MLD3/	unit 2
FC28 = NPOSLD/	unit 2
FC29 = DATLD/, WRTSTRT/	unit 2

Table 1

Read and Write Select Generator Sections

The Read and Write Select Generators are shown on sheet 3 of the schematics. The Read Select Generator outputs drive the 1Ø Read Select input lines to the Partition Read/Latch Selector block shown in Figure 2. The generator consists of Y33X17, a BCD-to-Decimal decoder, driven by RØ - R3. Timing Diagram 5 shows the outputs of the Read Select Generator. Outputs READ1/ and READ9/ are also used as control inputs to the Handshake Section.



TIMING DIAGRAM - 5 - WRITE REQUEST INITIATION
(6450-0377)

The Write Select Generator consists of BCD-to-Decimal decoder Y36X17 and is driven by XØ - X3. The outputs from this section drive the Write Data Selector block shown in Figure 2. Note that WRTOK/ is ORed with X2 and X3 to produce the C and D inputs of Y36X17 respectively. WRTOK/ is high at all times except during the 18X - 19X time shown in Timing Diagram 3. Therefore, only during this time can there be a valid BCD input to the BCD to Decimal decoder. Invalid inputs result in inactive high outputs from Y_0 - Y_9. Thus, WRTOK/ is used to disable the Write Select Generator at all times except during a write cycle.

DATARAM Mode Control Generator

There are five mode-control signals that the DATARAM uses to determine whether an operation is a Read, Write or R/M/W. In addition, these same five lines determine whether the operation is to be performed on a 16- or 32-bit word.

The generator is shown at the bottom of sheet 9 of the schematics and consists of Y48X32-A and -B, and AND gates Y42X23-A and -B. Four of the five control lines are tied together and driven by a common source. These signals are MWRLBN (Memory Write Lower Byte), MWRUBN (Memory Write Upper Byte), MWRLBAN (Memory Write Lower Byte Upper Word) and MWRUBAN (Memory Write Upper Byte Upper Word). Tying these lines together results in 32-bit operations only. Whether an operation is a 32-bit read, write or R/M/W is determined by the relationship between this group of controls and the control signal MRDRN (Memory Read). The relationships between these signals and the operations which result are shown below:

MRDRN	Four Line Group	Operation
Low	Low	R/M/W 3Ø-bit word
Low	High	READ 3Ø-bit word
High	Low	WRITE 3Ø-bit word (erase)
High	High	Invalid, not used

D latch Y48X32-A is clocked by ERASE CMD/ and the D and CLR inputs of the latch are driven by the Q/ output of D latch Y48X32-B. Since latch Y48X32-B normally is reset, the D input of Y48X32-A normally is high. Therefore, if an ERASE CMD/ is generated, a high is latched into Y48X32-A, driving its Q output high. This high output is latched into Y48X32-B by S8, the odd/even (OE) signal. S8 is positive going at the beginning of the second field of each two-field frame. On the rising edge of S8, Y48X32-B sets, driving the Q output high and the Q/ output low. The Q/ output resets Y48X32-A, which places a low at the input of Y48X32-B. On the next rising edge of S8, Y48X32-B also resets, removing the clear input to Y48X32-A. Thus, when an ERASE CMD/ is generated, Y48X32-B sets on the next rising edge of S8 and resets on the following S8 rising edge. The Q/ output is applied to the Write Data Latch (see Figure 2) which causes all "zero"s to be written into all ten pixel partitions simultaneously. Note that Q/ is also applied to AND gate Y42X23-A and -B. Gate Y42X23-A ANDs the Q/ output of Y48X32-B with WRTOK/ to produce the four control line group. Therefore, the Q signal is low during a frame erase and during the 18X - 19X time shown in Timing Diagram 3 (Write phase of an R/M/W cycle). This gate produces a high output during Read time only. Y42X23-B ANDs the Q/ output of Y48X32-B with WRT/ to produce $\overline{\text{WRITE}}$/READ. This signal controls the direction of data flow through the Bi-Directional Data Bus Driver (see Figures 1 and 2). This signal is high during read time, placing the bus driver in the input mode. WRITE/READ, ERASE/ and the four control line group all go low during a frame erase. The Q output of Y48X32-B drives the MRDRN control signal and is low only during the erase cycle. It is high during Read and R/M/W cycles.

Handshake Section

The Handshake Section consists of the six blocks in Figure 4 not yet discussed. With exception of the Write Request Generator block, all circuitry is located on sheet 9 of the schematics. The Write Request Generator is contained on sheet 7.

Write Request Generator

The Write Request Generator consists of D-latches Y6ØX48-A and -B, AND gate Y51X48-B, and sections 3 and 4 of quad D latch Y72X3Ø. In

addition, NAND gate Y51X48-C and OR gate Y57X57-A are used to generate a Write XACK/ response signal. Timing waveforms for this section are shown in Timing Diagram 5. The timing diagram assumes that a DATLD/ command has just been issued to an image unit (unit 1 or 2), resulting in a one-PXLCK-clock-wide WRT STRT/ pulse which presets latch Y6ØX48-B. This latch remains set until the completion of the R/M/W cycle and is used to generate an input to the XACK/ (transfer acknowledge) generator. Input to the XACK/ generator informs the CPU that the storage operation is complete.

WRT STRT/ is also applied to the clock input of Y6ØX48-A and resets the latch on the trailing positive edge of WRTSTRT/. When the latch resets, it outputs a logic "one" from the Q/ output which is then applied to the 3D input of quad D-latch Y72X3Ø. On the following rising edge of PXLCK, the logic one is latched, resulting in a high at pin 4 of NAND gate Y51X48-B, and the 4D input of Y72X3Ø. At this time, the NAND gate is qualified because the previous input to 4D was a "zero", resulting in a high at 4Q/. The logic zero output from NAND gate Y51X48-B presets Y6ØX48-A. WRTPLS/ (Write Please), the output of the NAND gate, is the Write request. When Y6ØX48-A is preset by WRTPLS, it outputs a zero from the Q/ output. The logic zero output is applied to the 3D input of the quad latch and is latched on the next rising edge of PXLCK. This disqualifies the NAND gate, limiting the length of WRTPLS/ to 81.4 nsec (one clock period).

Write Request Latch

Refer to sheet 9 of the schematics. The Write Request Latch consists of D-latches Y54X48-A, Y42X15-B, and Y39X17-B, and inverter Y54X4Ø-A. The inverter applies the inverted WRTPLS/ to the clock input of Y54X48-A. Therefore, the leading edge of WRTPLS/ causes a "zero" to be latched into Y54X48-A, driving the Q output WRTGNT/ (Write Granted) low. WRTGNT/ is applied to the clock input of Y6ØX48-B (see sheet 7) and to the D input of Y42X15-B. The negative going input to Y6ØX48-B has no effect because the latch only responds to rising edges. The logic low input to Y42X15-B is latched by WRTOK, which goes positive at the beginning of the 18X word time (see Timing Diagram 3). The logic low Write Request at the output of Y42X15-B is applied to the D input of latch Y39X17-B. The purpose of this latch is to delay processing of the request until the beginning of READ2/

(same as the end of READ1/). The positive-going, trailing edge of READ1/ is used as the clock input to Y39X17-B. The Q output of Y39X17 is applied to pin 1Ø of NAND gate Y48X48-C. This NAND gate is part of the Address Available Generator block shown in Figure 4. The other input to the NAND gate is the output of the Read Request Latch (D-latch Y54X48-B).

Read Request Latch

The Read Request Latch consists of D-latch Y54X48-B, clocked by PXLCK and preset by READOK. When READOK is high (1X-16X word times), an active low READ1/ is latched into Y54X48-B by PXLCK. The output of this latch is applied to pin 9 of NAND gate Y48X48-C, part of the Address Available Generator.

Address Available Generator

The Address Available Generator consists of NAND gate Y48X48-C and D-latch Y42X15-A. The NAND gate multiplexes the requests from the Read and Write Request latches. Because the D input of the latch is grounded, it outputs a "zero" on each rising edge of the NAND gate output. ADRAVN (Address Available), the Q output of Y42X15-A, informs the DATARAM BSC board that an operation is requested (Read, Write or R/M/W), and the data on its address bus is valid. Within about 80 nsec, the DATARAM BSC board responds by bringing ADRACN (Address Accepted) low. ADRACN presets Y42X15-A back to a high output on Q and is applied to AND gate Y42X23-C (pin 9), part of the Response Address Valid Generator Section.

Response Address Valid Generator

Refer to sheet 9 of the schematics. The Response Address Valid Generator consists of:

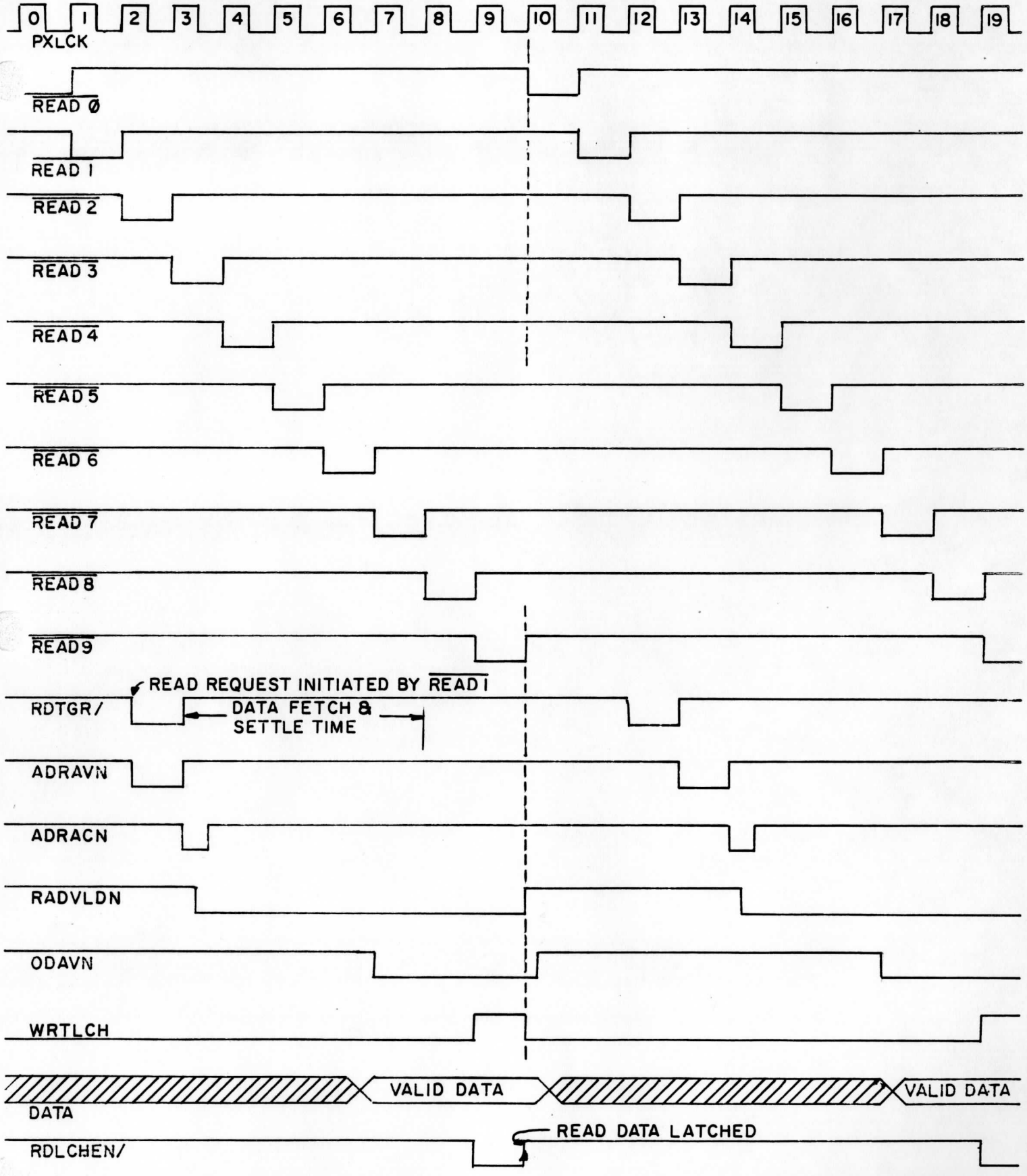
- latches Y42X7-A and -B (center right of sheet)
- latch Y39X25-B (bottom center of sheet)
- inverters Y48X4Ø-C and -D (center of sheet)
- inverter Y54X4Ø-F (bottom left of sheet)
- NAND gate Y48X48-D (center of sheet)
- AND gate Y42X23-C (center right of sheet)

As discussed earlier in the Functional Description, RADVLD/ (Response Address Valid) plays a different role in each of the three modes (read,

write or R/M/W). In the read mode, the RAVLD/ signal tells the BSC board to send the requested data as soon as possible. During the write mode, this signal tells the BSC board that the data on the input data lines to the BSC board are valid. During the R/M/W cycle, this signal performs both of the above functions. Thus, it must go active low twice during an R/M/W cycle, once for the read portion and once for the write. The handshake response from the BSC board is ODAVN (Output Data Available) or IDACN (Input Data Accepted) for read and write cycles respectively. These handshake signals terminate the RADVLD/ signal. RADVLDN is initiated by ADRACN for read, write, and the read portion of the R/M/W cycles. During the Write portion of the R/M/W cycle, RADVLDN is initiated by WRTG.

Refer to Timing Diagram 6. During a read cycle, AND gate Y42X23-C (pin 10) is high and an incoming active low ADRACN causes a low at the CLR input of Y42X7-B. This clears the latch and generates an active low RADVLDN. When the requested data is available in the BSC board, the BSC board generates ODAVN. ODAVN informs the DATARAM Control Board that the requested data is available. ODAVN enters the board at P9-41 and is applied to OR gate Y6ØX4Ø-C. Because ODAVN remains active low until RADVLDN goes high, ODAVN is ORed with READ9/ to produce an active low coincidence pulse. This active low pulse drives NAND gate Y48X48-D low. That is the clock input to Y42X7-B. At the end of READ9/, the output of the OR gate (and therefore the clock input of Y42X7-B) goes high. This latches a logic one into Y42X7-B and ends RADVLDN. When RADVLDN goes high, the BSC board brings ODAVN high, ending the cycle. The signal WRTLCH is used to latch data into the Write Data Latch (see Figure 2) but serves no useful function during the Read cycle.

The Write cycle (used in erase only) is very similar to the Read cycle, except that we receive an active low IDACN in response to RADVLDN. In fact, the Write cycle is conducted only during the 1X-16X word times. Sixteen words are erased (instead of read) during each 19X cycle. The IDACN pulse enters the board at P9-37 and drives the output of AND gate Y42X23-D low. This presets all of the D-latches in the Write Request Latch section and terminates RADVLDN. It also functions as a clock for the X and Y counters (XYINCR/). Thus, an X/Y clock pulse is generated each time the DATARAM acknowledges a data write.

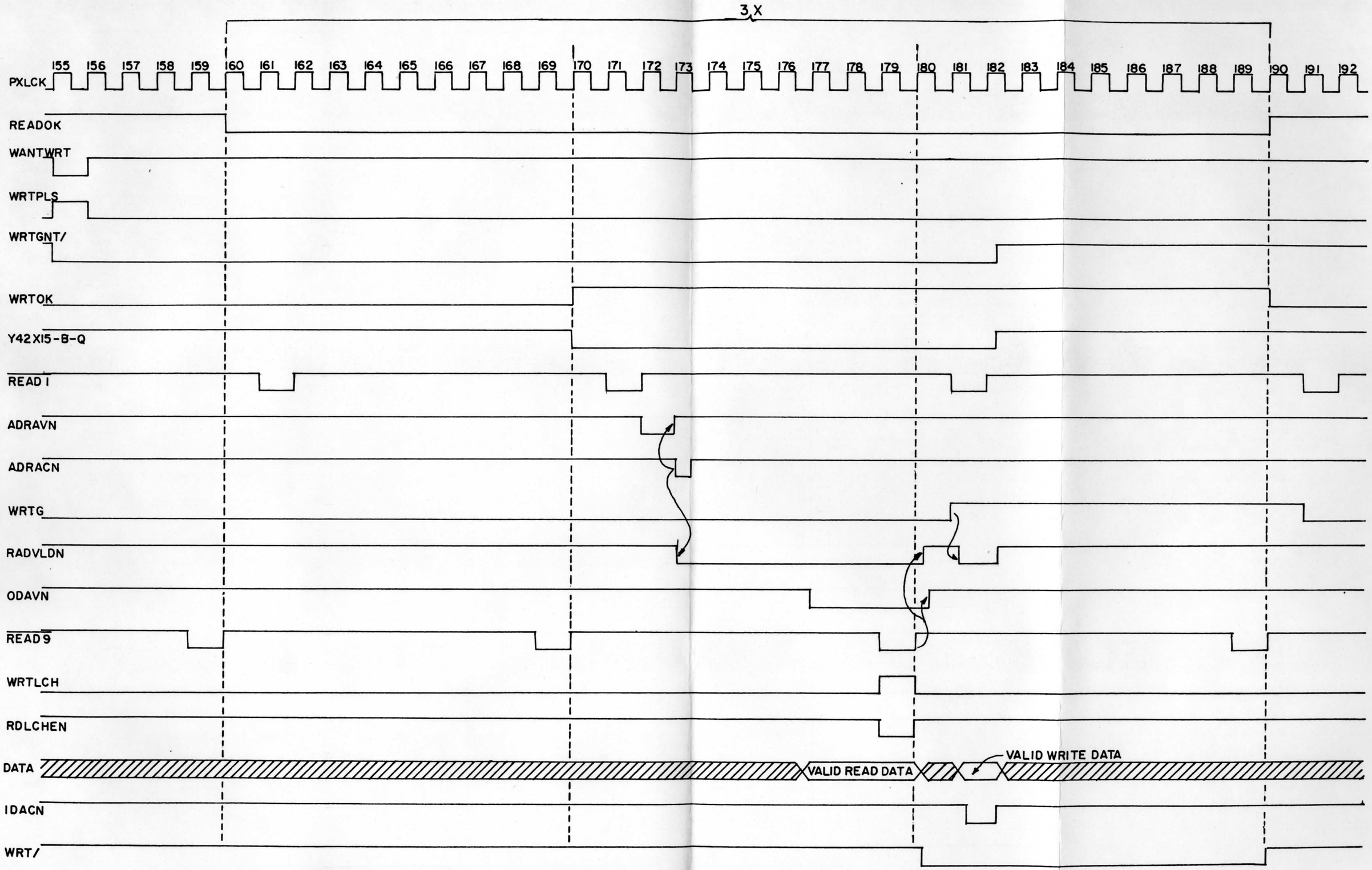


TIMING DIAGRAM-6 - DATA READ CYCLE
(6450 - 0377)

Refer to Timing Diagram 7. The R/M/W cycle is identical to the Read cycle until RADVLDN returns to an inactive high. At this point, the data has been received and one of the partitions has already been substituted with new write data. The modified word was latched into the Write Data Latch by WRTLCH. Now, RADVLDN must be driven low to initiate the Write phase of the R/M/W cycle. Since this cycle is initiated by the Write Request Generator, latches Y54X48-A and Y42X15-B are reset, providing an active low input to Y42X7-A. To generate another RADVLDN signal, a clock pulse is needed at the clock input of Y42X7-A. WRT/ is active low during the 19X cycle time only. Therefore, when inverted, WRT/ produces a rising edge in coincidence with the beginning of the 19X word time. WRT/ is inverted by inverter Y54X4Ø-F and applied to the D input of latch Y39X25-B. Therefore, the output of the latch is positive-going one PXLCK after the beginning of the 19X cycle. The Q output of Y39X25-B is used as the clock input of Y42X7-A, thereby generating the second active low RADVLDN.

Miscellaneous Control Signals

The control signal "Read Latch Enable" (RDLCHEN/) has not been described elsewhere. This signal is shown on sheet 3 of the schematic and consists of D-latch Y39X25-A. The signal latches the read data output of the Read Data Modifier (see Figure 2) into the Read Latch and Partition separator. Refer to Timing Diagram 6. Because READ8/ is applied to the D input and the latch is clocked by PXLCK, RDLCHEN/ goes active low in synchronism with READ9/; the latch must wait until PXLCK goes positive. It is the positive-going edge of RDLCHEN/ which actually latches the data, coincident with the beginning of READØ.



TIMING DIAGRAM -7- DATA READ/MODIFY/WRITE CYCLE (6450-0377)

SECTION 8
DATARAM/MULTIBUS INTERFACE
TABLE OF CONTENTS

DATARAM/MULTIBUS INTERFACE
(SSEC DRAWING 645Ø-Ø379, MODIFICATION E, DATED 3/17/86)

INTRODUCTION

The DATARAM/Multibus Interface provides the hardware interface between the Multibus and the three DATARAM dynamic RAM storage units. The protocol interfacing is accomplished on the DATARAM Control Board located in each DATARAM chassis.

FUNCTIONAL DESCRIPTION

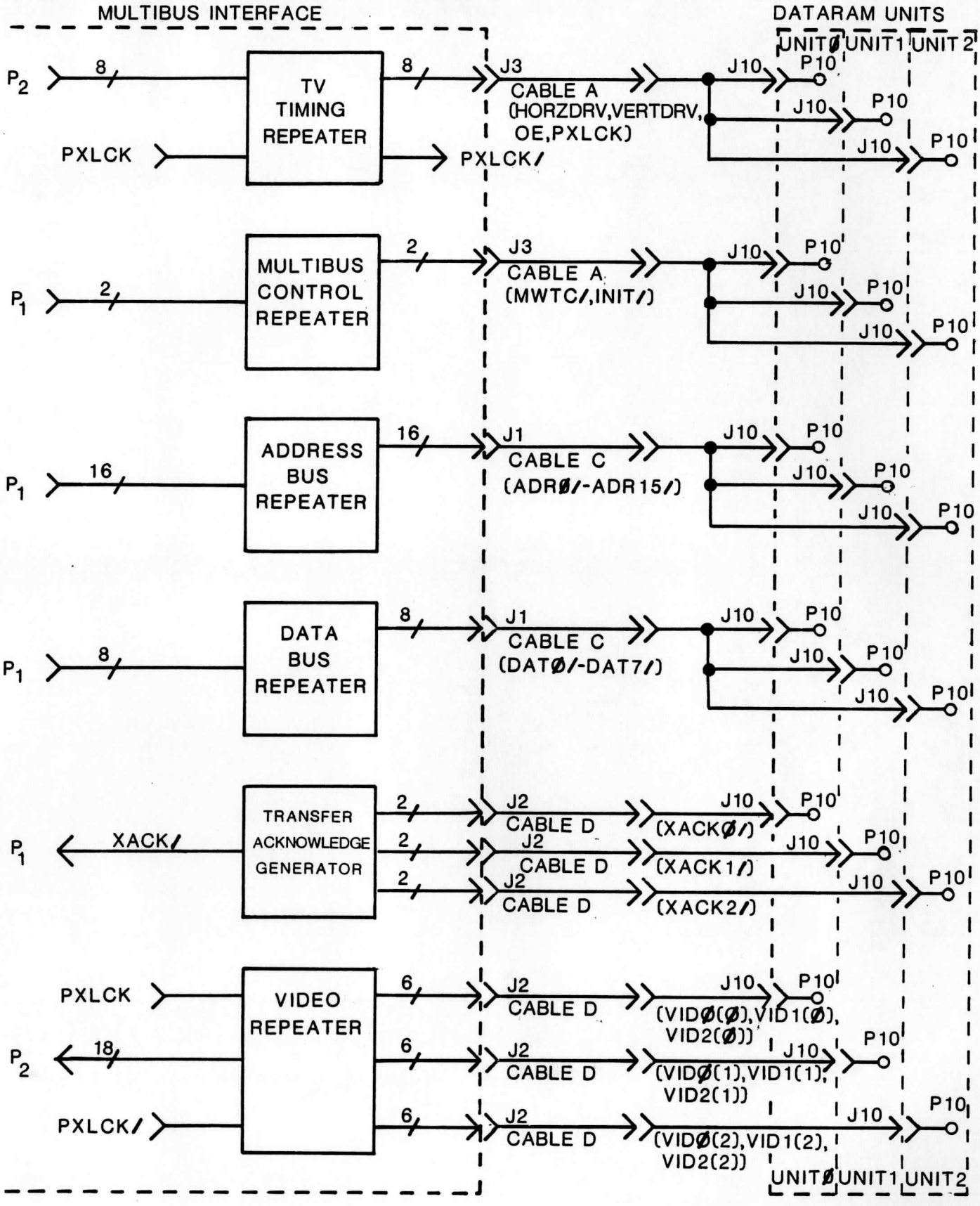
Refer to Figure 1, the functional block diagram of the DATARAM/ Multibus Interface. The following six groups of functional signals are transmitted either from the Multibus to the DATARAMs or from the DATARAMs to the Multibus:

- TV timing signals
- Multibus control signals
- address bus signals
- data bus signals
- the transfer acknowledge signal
- DATARAM digital video output signals

The first four groups of signals are originated by the Multibus while the last two are originated by the DATARAMs.

TV TIMING REPEATER

The TV Timing Repeater receives PXLCK, HORZDRV, VERTDRV, and OE signals from the Multibus P2 bus. These signals are received and re-transmitted as differential signals. The re-transmitted signals leave the interface board via J3 through a 5Ø-conductor ribbon cable (cable A). The ribbon cable is piggy-backed to the A-cable connector on each DATARAM chassis. Within each DATARAM chassis, the A, B, C, and D cables are hard-wired to the J1Ø connector. The P1Ø connector pins on the DATARAM control board connect directly to J1Ø, completing the path from the interface board to the DATARAM control board.



DATARAM/MULTIBUS INTERFACE FUNCTIONAL BLOCK DIAGRAM

FIGURE - 1

(6450-0379)

MULTIBUS CONTROL REPEATER

The Multibus control signals MWTC/ and INIT/ enter the interface board from the Multibus P1 bus and are re-transmitted by the Multibus Control Repeater. These signals pass through the same connectors and cables as the TV timing signals (see TV Timing Repeater section above).

ADDRESS BUS REPEATER

Multibus address bus lines ADRØ/-ADR15/ are originated by the Multibus P1 bus and are re-transmitted by line drivers. The re-transmitted signals exit the interface board via the J1 connector, which is connected to the C cable. The C cable is connected to the C connector on the DATARAM chassis. The C connector is wired to J1Ø.

DATA BUS REPEATER

Multibus data bus signals DATØ/-DAT7/ originate in the Multibus P1 bus. The signals are processed exactly as the address bus signals and travel through the same connectors and cables.

TRANSFER ACKNOWLEDGE GENERATOR

When the microprocessor performs a memory read or write to the DATARAM units, it enters a wait state (maximum of 10 msec) until the appropriate unit acknowledges completion of the operation. Because there are three DATARAM units, there are three separate acknowledge outputs (XACKØ/, XACK1/, and XACK2/, output from DATARAM units Ø, 1, and 2 respectively). The three separate acknowledge signals are combined into one signal by the Transfer Acknowledge Generator that drives the tri-stated Multibus transfer acknowledge signal XACK/.

Each of the DATARAM transfer acknowledge signals exit the DATARAM Control Board via a dedicated pin on the P1Ø connector. From the P1Ø connector, the signals pass through the J1Ø connector to the D-cable connector and cable. The D cable is connected to the J2 connector on the interface card. XACK/, the Multibus transfer acknowledge signal, exits the interface board via the Multibus P1 bus.

VIDEO REPEATER

Each DATARAM outputs video data as parallel three-bit words. The data enters the interface via the same connectors and cables as the transfer acknowledge signals described above. The three sets of 3-bit words are re-transmitted by the video repeater and transferred to the Multibus P2 bus. VIDØ(Ø)-VID2(Ø) (unit Ø data) are transported, via Multibus P2, to the TV Timing and Colorizer board. The remaining signals (units 1 and 2) are transported, via P2, to the Dual Channel Colorizer.

DETAILED CIRCUIT DESCRIPTION

TV TIMING REPEATER

Refer to schematic diagram 645Ø-Ø379, dated 3/17/86. PXLCK, HORZDRV, VERTDRV, and OE are applied to differential line receiver AF37 sections A, B, C, and D respectively. Note that the OE minus and plus drive signals are applied to the AF37-D plus and minus inputs respectively. Thus, OE is inverted at AF37 pin 13 (D output). The four outputs of AF37 are applied to differential line driver AF12. Note that PXLCK is also applied directly to AD23, AH23, and AK23; it is applied indirectly via inverter AF27-A to AD12, AH12, and AK12. These components use PXLCK and PXLCK/, covered in the Video Repeater section.

MULTIBUS CONTROL REPEATER

MWTC/ and INIT/ are applied to octal line driver AB33, pins 17 and 15 respectively. Pin 19 enables the MWTC/ and INIT/ drivers at all times. The driver connected to pin 2 is enabled by pin 1 which is active low during a transfer acknowledge (see Transfer Acknowledge Generator below).

ADDRESS AND DATA BUS REPEATERS

The address bus is buffered and re-transmitted by octal line drivers Z7 and Z2Ø. The data bus is treated identically by Z33.

TRANSFER ACKNOWLEDGE GENERATOR

The unit transfer acknowledge signals XACKØ/, XACK1/, and XACK2/ (units Ø, 1, and 2 respectively) are applied to the differential line receivers AB12-A, -B, and -C respectively. The differential line receivers convert the differential inputs to TTL outputs. The three

outputs are applied to the inputs of AND gate AB23-B. Therefore, the output of the AND gate goes active low if any inputs go active low. The AND gate output drives one of the tri-state controls (pin 1) on tri-state line driver AB33. On this chip, the only driver used is controlled by pin 1 and has input pin 2 and output pin 18. Because the input is grounded, a low on pin 1 causes XACK/ to go low, informing the microprocessor that the requested read or write operation is completed.

VIDEO REPEATER

There is a separate video repeater for each of the three units. Because all three are identical, only unit Ø is discussed. VIDØ(Ø) (LSB), VID1(Ø), and VID2(Ø) are applied to differential line receivers AD1-A, -B, and -C respectively. The three TTL outputs of the line receivers are applied to D-latch AD12, which resynchronizes the video data with the rising edge of PXLCK/. The three output bits of AD12 are then applied to D-latch AD23, which resynchronizes the data with the rising edge of PXLCK. Finally, the outputs of AD23 are applied to the A, B, and C sections of differential line driver AD37. The line driver outputs are transported to the TV Timing and Colorizer via the P2 bus.

SECTION 11
JOYSTICK BOARD
TABLE OF CONTENTS

MINIATURE JOYSTICK BOARD

(SSEC DRAWING 645Ø-Ø484, DATED 1Ø/22/85)

INTRODUCTION

The dual joystick module allows the user to maneuver a cursor symbol on the workstation monitor. It can also be used as a general I/O device. The joystick module provides analog voltages to the Miniature Joystick board. This board digitizes the four analog input voltages from the joystick module, converts the data to standard RS-232 levels and serially asynchronously transmits this data to the Cursor/Joyboard and Graphics Tablet board, where it is available to the microprocessor.

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the Miniature Joystick board. Movement of each joystick handle is sensed by two potentiometers (hereafter referred to as "pots"). One pot senses only the vertical component of the motion while the other senses only the horizontal. Diagonal motion creates inputs to both. There are two joysticks, so four pots are required to sense the positions of the handles. The outputs of the pots are sent to the pot multiplexer block of Figure 1. The pot multiplexer is an addressable analog switch. That is, each pot can be connected to the output of the multiplexer by applying the proper address.

The Timing Generator in Figure 1 produces three clock frequencies:

- 153.6-Khz output clock
- 4ØØ-hz control clock
- 96ØØ-hz data rate clock

For proper interpretation of the 96ØØ-baud serial output data, a clock signal 16 times the data frequency must be sent (153.6-Khz output clock). The 96ØØ-hz data rate clock is the source for all other timing; it includes an 8ØØ-hz strobe.

The Pot Address Generator uses the 8ØØ-hz strobe to produce a 4ØØ-hz clock. The 4ØØ-hz clock drives a counter that sequentially generates pot addresses for the Pot Multiplexer block.

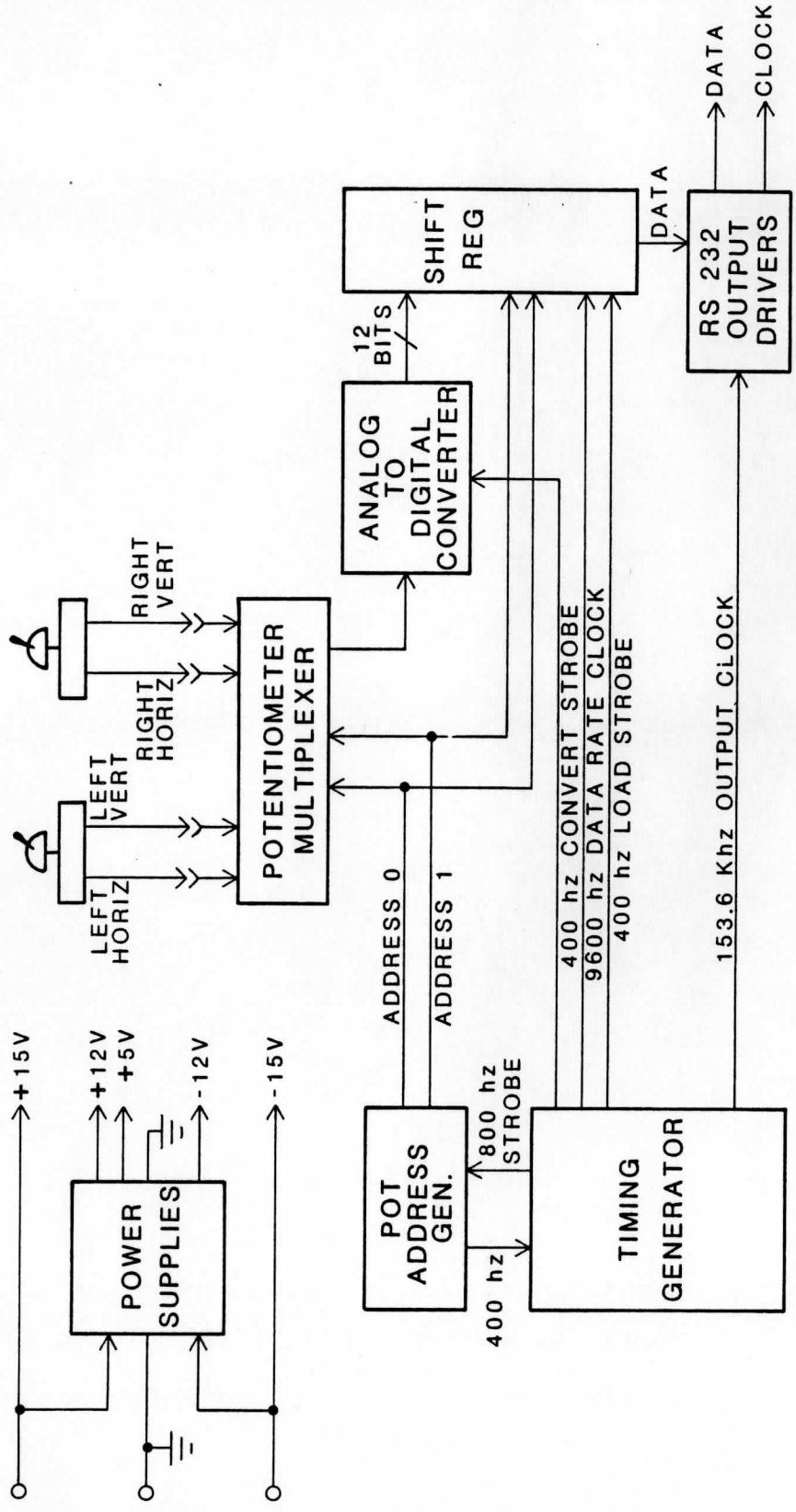


Fig. 1. Kraft Digital Joystick Functional Block Diagram.

The Analog-to-Digital Converter converts the selected analog voltage to a 12-bit binary number and sends it to the Shift Register.

The Shift Register performs the following four functions:

1) latches the Analog-to-Digital (A-to-D) output data into the input registers
2) encodes the pot address and byte identification codes
3) formats the data for serial transmission
4) serially clocks the data out to the RS-232 Output Drivers at a rate of 96ØØ bits/sec (baud)

The RS-232 Output drivers convert the Output Clock and Data to standard RS-232 logic levels for asynchronous 96ØØ-baud transmission.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the Miniature Joystick is shown on SSEC drawing #645Ø-Ø484 (dated 1Ø/22/85). The schematic circuit analysis is accomplished by analyzing groups of components represented by a single block in Figure 1 above.

SCHEMATIC CONVENTIONS

When reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and the letter designator. The symbol ID number alone is used to refer to single function ICs.

BAUD RATE GENERATOR

The Baud Rate Generator is represented by A1Ø and its associated components, A11-D, A4-C, A4-B, A4-A, A12-A, A4-D, A5, and A12-B. A1Ø is a crystal-controlled baud-rate generator capable of producing 64 subsets of the fundamental crystal frequency of 1.8432 Mhz. Through strapping of A1Ø and the selection of only F5 (pin 3) and F11 (pin 8), only two output frequencies are provided, 153.6 Khz and 96ØØ hz, respectively. The 153.6-Khz frequency (pin 3) is simply buffered by inverter A11-A before going to the RS-232 output driver A18.

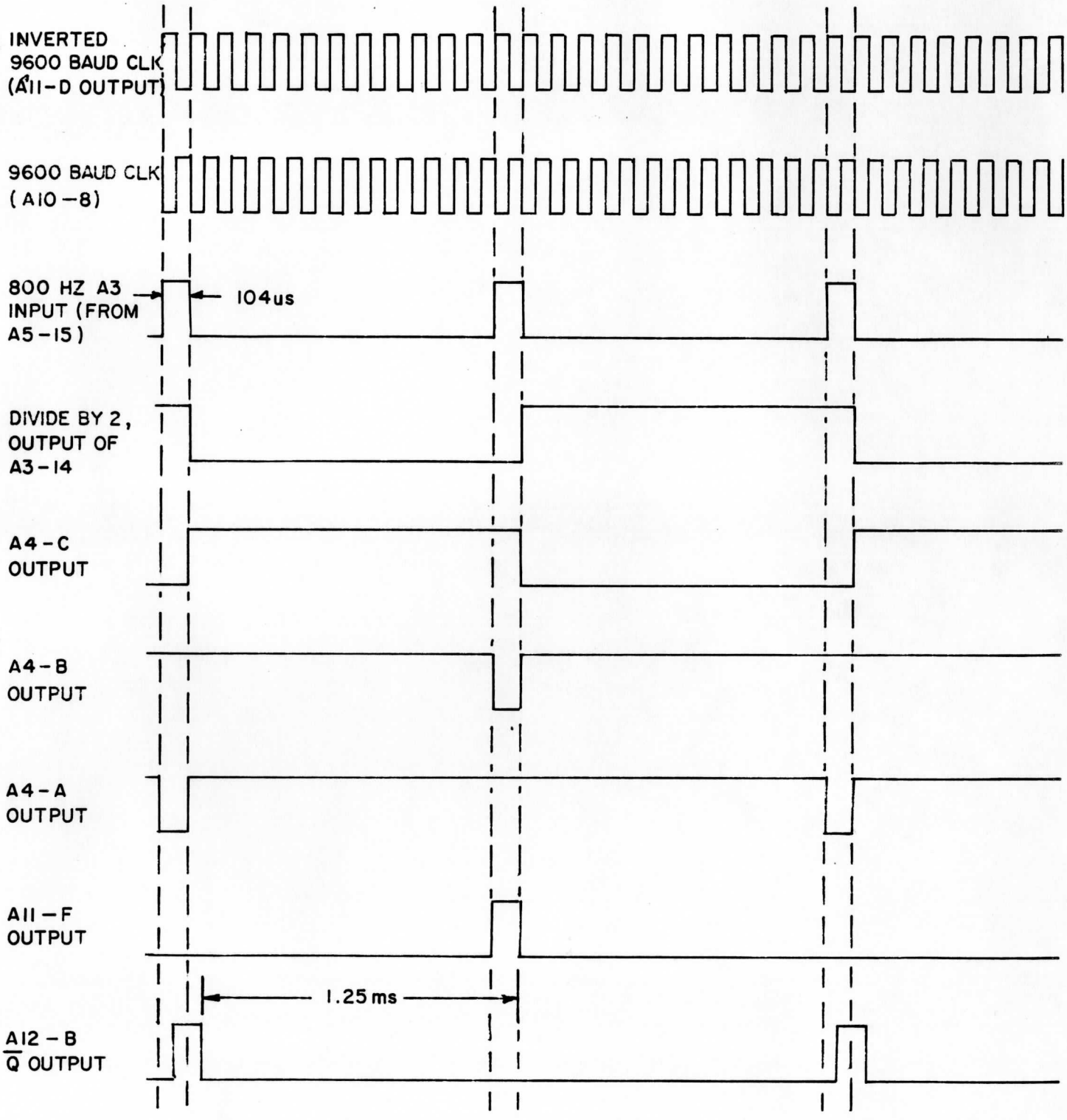
The 96ØØ-hz frequency is inverted by buffer A11-D for use by the Pot Address Generator A3 to clock the data from the shift register and drive counter A5. A5 is a four-stage binary counter forced to divide the

9600-hz buffered input clock by 12. This is accomplished by use of the overflow pulse to generate a preset count of 4, thereby generating a 104-μsec positive pulse in synchronism with each 12th rising edge of the inverted clock (see Timing Diagram 1). This produces an 800-hz strobe pulse, used by the Pot Address Generator (A3) and logic gates A4-B and A4-A. One output of the Pot Address Generator is a divide-by-two of the input 800-hz strobe, resulting in 400 hz. The logic state of the divide-by-two counter toggles to its opposite state upon receipt of each 800-hz strobe pulse (see Timing Diagram 1).

The state of the divide-by-two counter is inverted by inverter A4-C and applied, along with the 800-hz strobe, to NAND gate A4-B. When the output of the divide-by-two counter is a logic "zero" and the strobe is a logic "one" (see Timing Diagram 1), this results in a logic "zero" input to latch A12-A. The state of the divide-by-two counter and the 800-hz strobe are also applied to NAND gate A4-A (this time the divide-by-two output is <u>not</u> inverted). This results in a logic "zero" input to latch A12-B. When the output of the divide-by-two counter and the 800-hz strobe are a logic "one" (see Timing Diagram 1), the output of latch A12-A is buffered by inverter A11-F and applied to A-to-D converter A6. The inverted output from latch A12-B is applied to shift register A7, A8 and A9. These waveforms are shown in Timing Diagram 1. Note that the two output waveforms (A11-F and A12-B) are displaced from each other by 1.25 msec. The output of inverter A11-F generates conversion strobes for A-to-D converter A6, while the output of latch A12-B generates load and shift strobes for the shift register. This allows the A-to-D converter to convert the analog data to digital data, and make the digital data available to the shift register while the shift register is outputting the previous data.

POT ADDRESS GENERATOR

The Pot Address generator is A3, a divide-by-sixteen binary counter used as a divide-by-eight binary counter. As the counter counts the 800-hz input, it goes through a full cycle 100 times per second. The pot address is taken from the QB and QC outputs (pins 13 and 12, respectively). Table 1 below shows how QB and QC change as a function of the 800-hz input. QB and QC select which Multiplexer input pot is applied to the



TIMING DIAGRAM I

KRAFT DIGITAL JOYSTICK BOARD
(6450-0400)

A-to-D converter and supply pot address information to the shift register. During a counter cycle, each pot is selected and converted to digital data at a rate of 1ØØ times/sec.

Table 1

Pot Address State Table

QC	QB	QA	Pot	A to D	Shift Reg
Ø	Ø	Ø	right	convert	load
Ø	Ø	1	vert	load	shift
Ø	1	Ø	right	convert	load
Ø	1	1	horiz	load	shift
1	Ø	Ø	left	convert	load
1	Ø	1	vert	load	shift
1	1	Ø	left	convert	load
1	1	1	horiz	load	shift

POT MULTIPLEXER

The Pot Multiplexer is A1, a 75Ø3 circuit. This circuit, an eight-input analog multiplexer, is configured as a four-input device by grounding the high four inputs and the MSB address line. The Joystick module voltage outputs (-3v to +3v) are applied via J2 (pins 1, 2, 3, and 4) to A1 (pins 13, 11, 1Ø, and 9, respectively).

Addressing inputs from the Pot Address Generator are applied to A1 pins 16 (LSD) and 1 (MSD). The selected output is applied to the input of the A-to-D converter A6. Note that each input to the multiplexer is filtered for noise reduction by a low pass RC T filter.

ANALOG-TO-DIGITAL CONVERTER (A-TO-D)

The Analog-to-Digital Converter (A-to-D) is comprised of A6 and associated discrete components (all are capacitors used for decoupling and noise reduction). A6 is a 12-bit, successive-approximation, A-to-D converter. The circuit contains its own on-chip clock and internal voltage reference, thereby reducing support circuits. The circuit requires a positive pulse at the convert pin (21) to initiate or arm the conversion cycle. The conversion does not begin until the falling edge of the convert pulse. A complete conversion requires only 1Ø µsec. Thus, all

digital outputs are at their correct state 1Ø µsec after the falling edge of the convert pulse. During the 1Ø4-µsec positive portion of the convert pulse, the converter is armed. During the first 1Ø µsec of the 2396-µsec rest period, conversion takes place and data is presented to the shift register.

SHIFT REGISTER

The Shift Register comprises A7, A8 and A9. Each of these three ICs is an eight-bit, parallel-input shift register. When the PE pin (pin 9) is high, parallel data is loaded into the registers. When pin 9 is low, data is shifted serially out of the registers (LSB bit first) by the 96ØØ-hz inverted clock. Note that the output from A7 shifts into the input of A8 and the output from A8 shifts into the input of A9.

Twelve data bits from the A-to-D converter, two bits of pot address encoding and two bits of character identifier must be formatted for serial asynchronous RS-232 transmission (16 data bits total).

The data bits are loaded into the three 8-bit shift registers (A7, A8, and A9) along with the start, stop, and parity bits required by RS-232 receiving hardware on the Cursor/Joyboard and Graphics Tablet board. The start, stop, parity, and character identifier bits are hard-wired by grounding or strapping appropriate shift register inputs to +5 volts. One start and two stop bits is standard RS-232 convention; however, the parity bits are used only as a filler and are ignored on the receiving end (always transmitted as a high). The pot address information is applied to A8 pins 6 and 7. Table 2 below summarizes the conditions of A7, A8 and A9 after a register load has been performed.

The data is shifted out of the shift registers, one bit at a time, by the 96ØØ-hz data rate clock. Note that four sets of loads and shifts are required to transmit the positions of all four pots.

Table 2

Shift Register Data Format

A7								A8								A9								
PØ	P1	P2	P3	P4	P5	P6	P7	PØ	P1	P2	P3	P4	P5	P6	P7	PØ	P1	P2	P3	P4	P5	P6	P7	
1	1	1	D	D	D	D	D	D	D	1	Ø	1	1	1	D	D	D	D	D	D	D	Ø	Ø	*value
SP	SP	P	D	D	D	D	D	AD	AD	ID	ST	SP	SP	P	D	D	D	D	D	D	D	ID	ST	**function
2nd character								1st character																

* 1 = high, Ø = low, D = variable
**ID = identification, Ø = 1st character, 1 = 2nd character
ST = start
SP = stop
D = data
AD = address
P = parity

RS-232 OUTPUT DRIVERS

A18 is a dual RS-232 line driver. The line drivers convert the TTL logic levels from A1Ø pin 3 (output clock) and A9 pin 3 (via A11-B and A11-C) to RS-232 levels. A high input causes an output of approximately -1Ø volts and a low input causes an output of approximately Ø volts.

POWER SUPPLIES

The power supplies consist of A16, A17, A18, and an associated filter capacitor. These IC regulator chips produce the -12 volt, +12 volt, and +5 volt, sources from the +15 volt and -15 volt inputs.

SECTION 12
NTSC TV SYNC UNIT II
TABLE OF CONTENTS

NTSC TV SYNC UNIT II

(SSEC DRAWING 6450-0431, MODIFICATION G, DATED 6-22-84)

INTRODUCTION

The NTSC TV Sync Unit has two purposes; it provides the necessary TV Sync signal for NTSC encoders, TV cameras, recorders and other TV equipment, and it provides pixel clock and sync reset signals to "gen lock" (generator frequency lock) a McIDAS terminal. The operating modes are:

- internally-generated sync and sub carrier signals
- "gen locked," where the NTSC Sync Unit is locked to an externally-generated master composite sync signal.

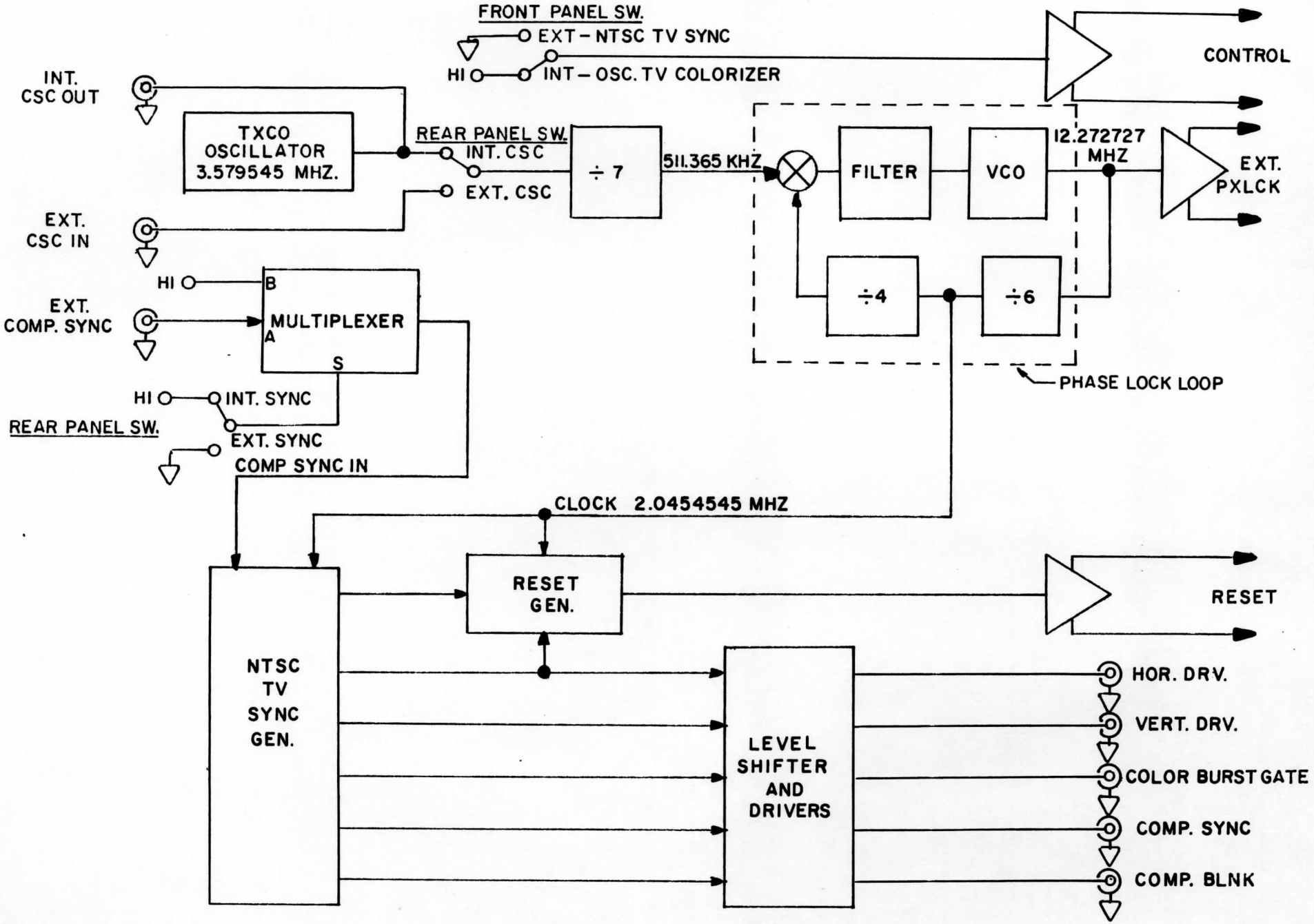
FUNCTIONAL DESCRIPTION

Refer to Figure 1, the function block diagram of the NTSC TV Sync Unit II. All signals generated by this unit are either a multiple or sub-multiple of a 3.579545-Mhz reference frequency. This reference frequency is generated either internally by a high-quality, temperature-compensated crystal oscillator (TXCO) or by an external source. A rear-panel-mounted switch selects the source of the reference.

The reference frequency is divided by seven to produce a 511.365-Khz reference for a phase-locked loop. The phase-locked loop produces the 12.272727-Mhz pixel clock by multiplying the reference frequency by 24. It also produces a 2.Ø45454-Mhz clock for use by the NTSC TV Sync Generator block, by dividing the pixel clock frequency by six. The following five blocks constitute the phase-locked loop:

- Phase Comparator (digital)
- Filter
- Voltage-Controlled Oscillator (VCO)
- Divide-by-six block
- Divide-by-four block

The Phase Comparator compares the 511.365-Khz reference signal to pixel clock divided by 24 (511.365 Khz). If there is a difference in frequency or phase, the Phase Comparator produces a DC error voltage. The



FIGURE·1 NTSC TV SYNC UNIT II FUNCTIONAL BLOCK DIAGRAM
(6450-0431)

Filter smoothes the noisy DC-error output from the Phase Comparator. The Voltage-Controlled Oscillator (VCO), a DC-controllable oscillator, has a natural frequency of about 15 Mhz. The DC error input to the VCO forces it to operate at exactly 12.272727 Mhz. The Divide-by-four and Divide-by-six blocks, together, form a divide-by-24 block. If the VCO drifts off frequency, the output from the divide-by-24 block is no longer 511.365 Khz. The Phase Comparator output shifts in the proper direction (up or down) to pull the VCO back on frequency. The output is applied to a line driver for output to the McIDAS workstation (TV Timing and Colorizer board).

The 2.Ø45454-Mhz output from the Divide-by-four block is a clock input to the NTSC TV Sync Generator block. This block is a single IC chip, containing the necessary dividers and logic to produce all of the standard TV sync signals from the single clock input. The Sync Generator block chip can be synchronized to a master unit via the external composite sync input (CMP SYNC IN). This feature is used in an installation involving multiple workstations equipped with the NTSC TV Sync Units. The external composite sync is coupled into the unit via a BNC connector located on the rear panel. The unit can be switched from internal sync to external sync via a rear-panel, switch-controlled multiplexer.

The NTSC TV Sync Generator block outputs the following signals:

- Composite Sync
- Composite Blanking
- Color Burst Gate
- Vertical Drive
- Horizontal Drive

These signals are applied to the Level Shifters and Drivers block which directly drives the rear-panel-mounted BNC output connectors. Composite Sync, Composite Blanking, and the Internal Color Subcarrier Output signals drive an NTSC Encoder Unit which combines these signals with the Red, Blue and Green video drive signals to produce the NTSC monitor drive signal. The Horizontal Drive, Vertical Drive, and Color Burst Gate are presently unused. They are, however, convenient oscilloscope sync points for troubleshooting video-related problems.

The Reset Generator block provides a "gen lock" synchronizing pulse to the TV Timing and Colorizer board. The need for this signal is explained in detail in the TV Timing and Colorizer description. Essentially, however, the TV Timing and Colorizer board has a sync generator

chip, very similar to the NTSC TV Sync Generator chip. When using the NTSC Sync Generator as the system master timing generator, you must replace the TV Timing and Colorizer board's internally-generated pixel clock (PXLCK) with the pixel clock output from the NTSC Sync Unit II. You must also synchronize the vertical and horizontal drive signals. The drive signal synchronization is accomplished by locking the TV Timing and Colorizer generator chip to the NTSC Sync Unit II generator. To do this you must generate a sync pulse which occurs at the proper rate and time to synchronize the TV Timing Unit. This pulse must occur at approximately the sixth horizontal scan after the beginning of the even field vertical drive pulse.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the NTSC TV Sync Unit II is shown on SSEC drawing #645Ø-Ø431 (Modification G dated 6/27/84). The schematic circuit analysis is accomplished by analyzing groups of components, represented by a single block in Figure 1 above.

SCHEMATIC CONVENTIONS

When reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and the section letter designator. The symbol ID number alone is used to refer to single section ICs.

TXCO OSCILLATOR

Refer to Sheet 2 of the schematic. The color sub-carrier (CSC) signal is generated by a temperature-compensated crystal oscillator (TXCO) module that is chassis-mounted. The 3.579545-Mhz reference signal is approximately 2.Ø V peak-to-peak (p-p) in amplitude, and is RC-coupled to voltage amplifier BG4Ø, which provides a 4.Ø V p-p output signal. The output of BG4Ø is applied to the input of current amplifier BG37. The output impedance of BG31, in series with a 68-ohm registor, is approximately six ohms.

Together, these two resistances form a 75-ohm output impedance for driving the 75-ohm "INT CSC OUT" line at approximately 2.Ø V p-p.

DIVIDE-BY-SEVEN

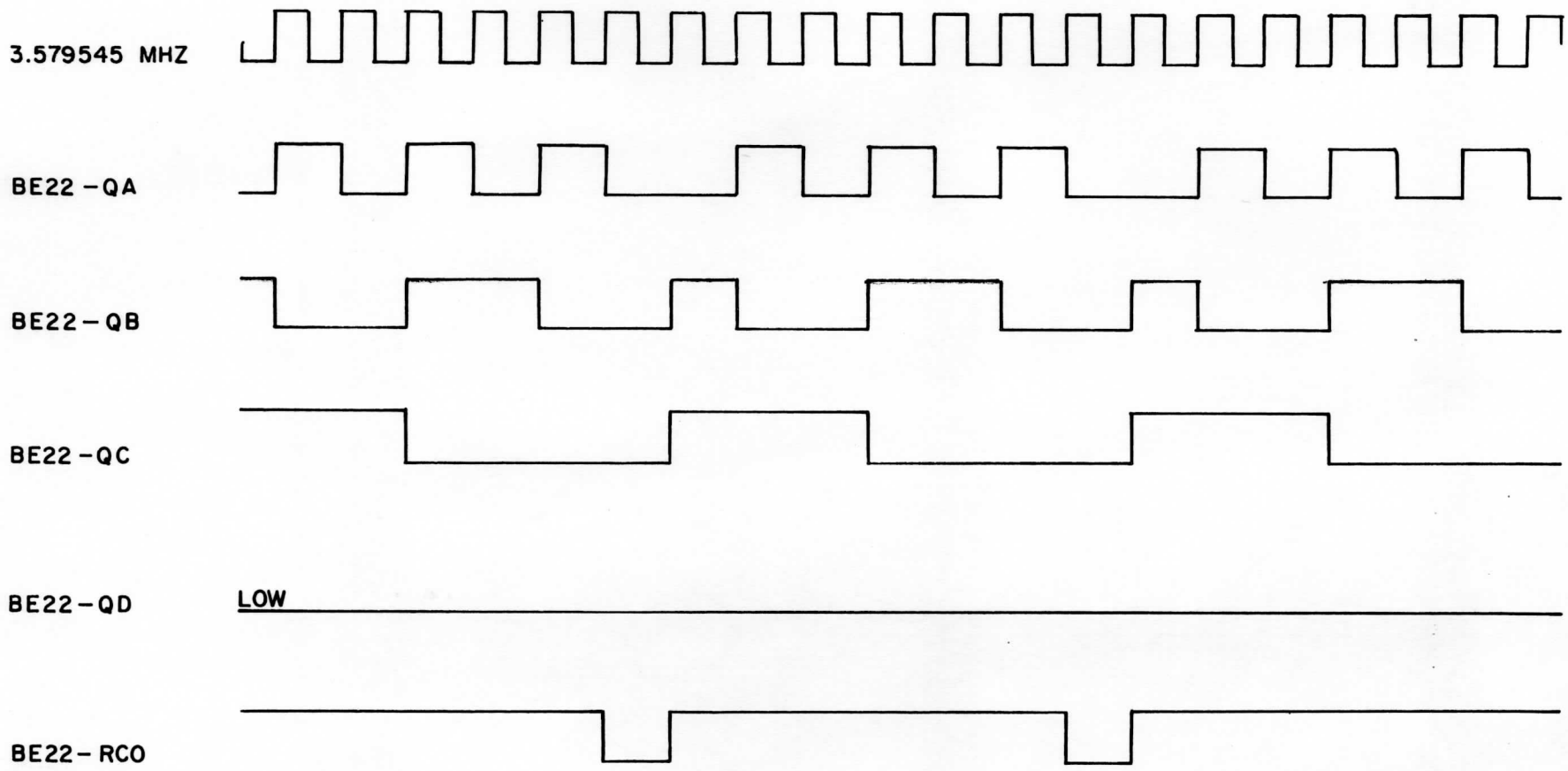
The output of current amplifier BG37 is also applied to switch S1 (see sheet 1). S1 selects either the internal Color Sub-Carrier (CSC) or the external CSC signal source. The selected source is applied to line receiver BG2Ø, which converts the sine wave to a square wave. The 1ØØK-ohm potentiometer controls the symmetry of the square wave output. The line receiver output is used as a clock by BE22, a four-bit binary counter, wired as a divide-by-seven circuit.

BE22 is wired as a down counter and has pre-set inputs of Ø11ØB (six). The ripple carry output (pin 15) is wired to the load input (pin 9). Refer to Timing Diagram 1. Because the counter features a synchronous load, six clock cycles count the counter down to ØØØØB and produce a ripple carry (underflow), but the counter does not actually pre-load until the 7th clock pulse arrives. Thus, the counter divides by seven. Pin 12 of BE22, the QC output, drives the phase-locked loop Phase Comparator reference input. It is not important that QC is non-symmetrical, because the Phase Comparator is sensitive only to negative-going edges.

PHASE COMPARATOR

The Phase Comparator is BC25, a Motorola MC4Ø44B. This circuit consists of three parts: a digital phase comparator, a charge pump, and a darlington amplifier. The reference 511.365-Khz signal is applied to the "RC" (pin 1) input of the Phase Detector while the VCO signal is applied to pin 3 (y_1). There are two outputs from the comparator, a pump-up output and a pump-down output. The comparator section is designed so that both outputs are high when the input phases are exactly equal. If the VCO input lags in phase, active low pulses appear at the pump-up output (pin 13). The width of these pulses increase with an increase in phase difference until a maximum of 5Ø% duty cycle is reached (18Ø° phase difference). If the VCO output leads in phase, the pump-down output (pin 2) performs exactly as the pump-up output during a phase lag. The pump-up and pump-down outputs are coupled to the charge pump inputs by connecting pin 13 to pin 4 (pump-up input of the charge pump) and connecting pin 2 to pin 11 (pump-down input of the charge pump).

The Charge pump consists of two electronic switches. A logic high at the charge pump inputs <u>opens</u> the switches. The pump-up switch is



NTSC TV DIVIDE-BY-SEVEN TIMING

TIMING DIAGRAM – 1

6450-0431

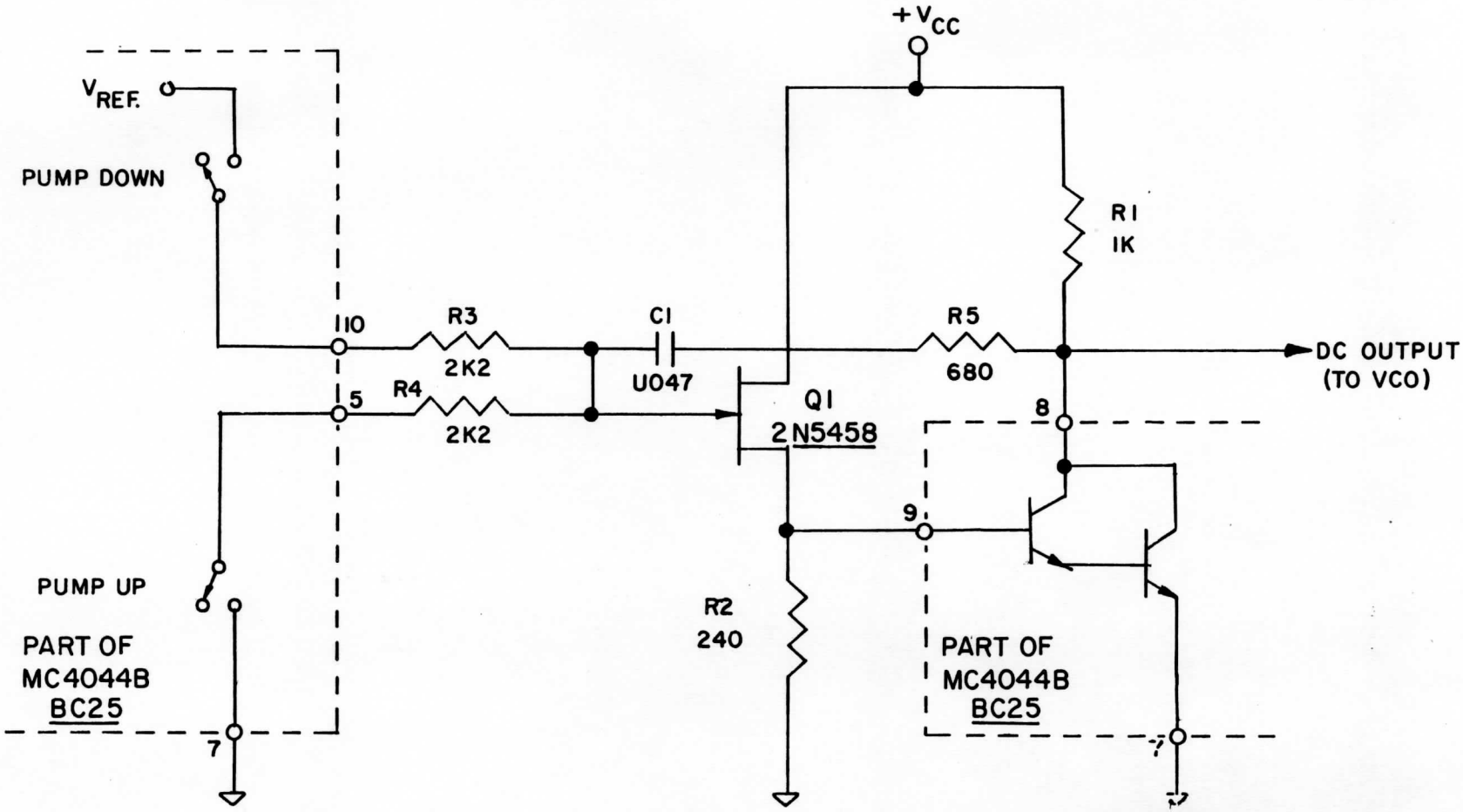
connected between ground and resistor BC35 (2.2 K ohm connected to pin 5), while the pump-down switch is connected between an internal voltage source and resistor BC36 (2.2 K ohm connected to pin 1Ø). These resistors are part of the Filter block discussed in the next paragraph.

FILTER

Figure 2 was redrawn from SSEC drawing 645Ø-Ø431 and the MC4Ø44B schematic. The circuitry in Figure 2 functions as a Miller integrator or low-pass active filter. The value of C_1 is effectively multiplied by the very high beta of Q_2. If the pump-up switch is closed (VCO has lagging phase), a charge path for C_1 is completed from ground through R_4, C_1, R_5, R_1, and VCC. The charge current for C1 flows through R_4, making the junction of R_4C_1 positive (with respect to ground). This positive voltage is amplified Q_1, a junction FET (Field Effect Transistor), operating as a source follower. The positive going output of Q_1 is applied to darlington common emitter amplifier Q2, resulting in a decrease in collector voltage. The collector output of Q2 is coupled back to the gate of Q_1, via R_5 and C_1, as a negative feedback, cancelling nearly all the original input. This results in a very low charge current for C_1 and a very long time constant. When the pump-down switch is closed, the capacitor attempts to discharge through Q_2 to ground, causing the collector of Q_2 to decrease in voltage. In summary, a lagging VCO phase results in an increasing voltage at Q_2's collector and vice versa.

VCO

The VCO is BE33, a dual TTL voltage-controlled oscillator. The oscillator's base frequency is established by the variable capacitor soldered between pins 4 and 5. Pin 3 is the range control for the VCO and is connected to a decoupled +5 volt supply, yielding maximum range. The DC error voltage output from the filter is applied to pin 2 as the control voltage. The output from pin 7 is a symmetrical 12.272727-Mhz square wave and is applied to differential line driver BC3-A and quad D-latch AG1. BC3-A provides the NTSC pixel clock drive for the TV Timing and Colorizer board.



PHASE COMPARATOR FILTER SCHEMATIC

FIGURE-2

6450-0431

DIVIDE-BY-SIX

The quad D-latch, AG1, is wired as a divide-by-six circuit by cascading stages 1-3 and connecting the Q/ output of stage 3 back to the input of stage 1. The VCO output is used as a clock. The Q output of the third stage drives the Divide-by-Four circuit and the clock input of the TV Sync Generator. The output of AG1-Q3 is a symmetrical 2.Ø454545-Mhz square wave.

DIVIDE-BY-FOUR

The Divide-by-Four block consists of BC12-A and -B. Each section of BC12 is wired as a divide-by-two stage; the two stages are cascaded, resulting in a divide-by-four of the 2.Ø45454-Mhz input (511.265 Khz). The output of this block is applied to the VCO input of the Phase Comparator.

NTSC TV SYNC GENERATOR

The NTSC TV Sync Generator is chip AE1. This chip provides all of the basic sync functions for either color or monochrome 525 line/6Øhz interlaced camera and vídeo recorder applications.

The chip divides the clock input by 13Ø to produce the horizontal drive frequency of 15,734.3 hz. The vertical drive frequency is generated by dividing the horizontal frequency by 262.5, resulting in a vertical drive frequency of 59.94 hz. All remaining output signals from this chip are composites of these two frequencies. For further information on this device, refer to a Fairchild Semiconductor MOS/CCD data book.

MULTIPLEXER

The NTSC TV Sync Unit II is a general-purpose NTSC generator. A master generator's composite sync output may be used as a synchronizing signal for the NTSC TV Sync Generator chip. The master generator's synchronizing signal is applied to the EXTERNAL COMP SYNC IN jack on the rear panel, where it is coupled into line receiver BG2Ø-A.

The output of line receiver BG2Ø-A drives the "A" input of the Multiplexer (chip AG12). The "B" input of the chip is driven by a pull-up. The sync selector switch places a logic low on the multiplexer's "select" input (pin 1) when switched to the EXT.SYNC position. A logic

low on pin 1 selects the "A" input (external composite sync). The output of the Multiplexer is applied to the CMP SYNC IN (pin 11) of the NTSC TV Sync Generator chip.

LEVEL SHIFTERS AND DRIVERS

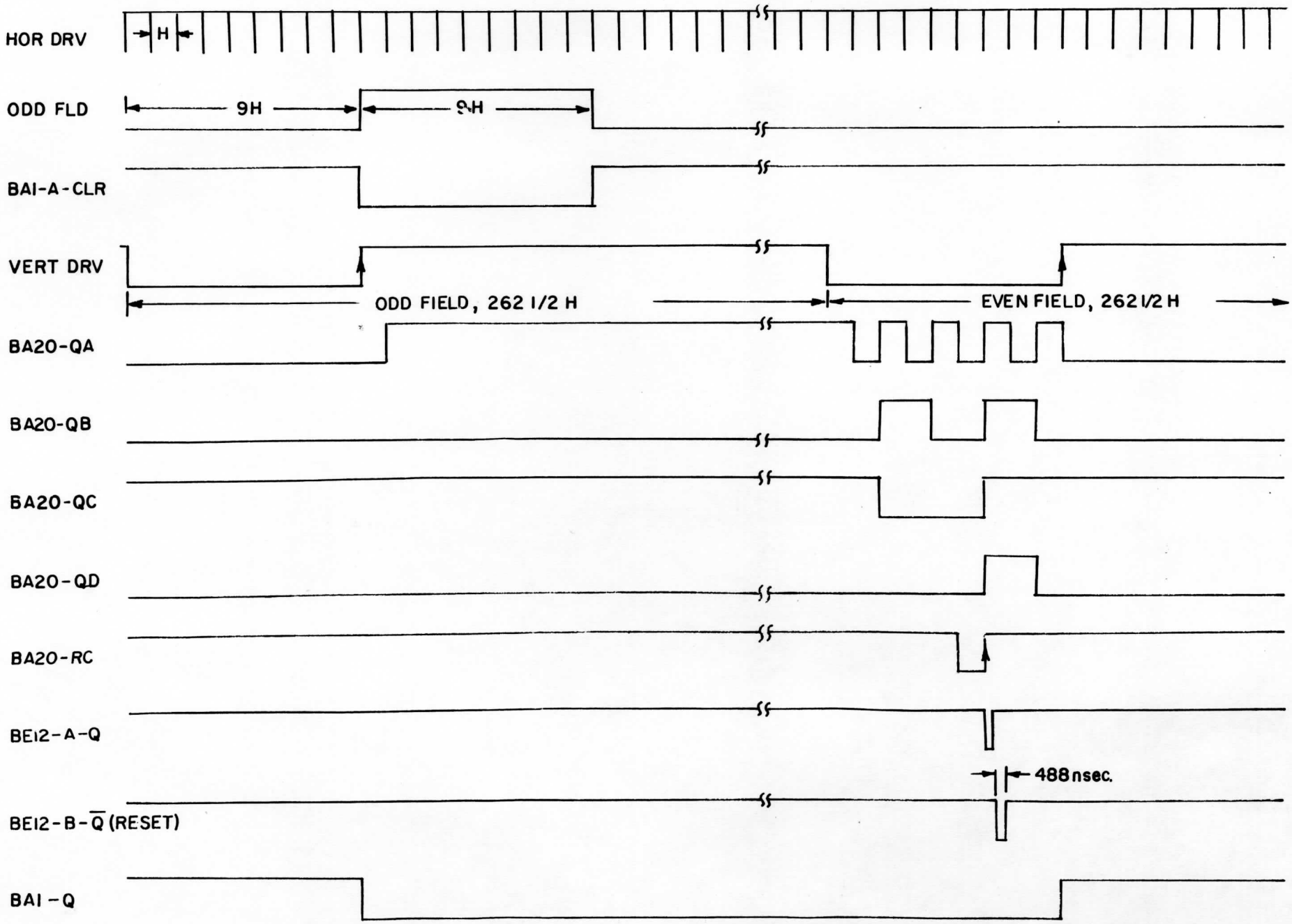
Except for the ODD FLD (pin 3) output of the NTSC TV Sync Generator chip, all outputs are inverted by sections of hex inverter AE1Ø and applied to dual 2-input NAND gate TTL-to-MOS voltage shifters. Each output of the sync generator chip drives both inputs of a single NAND gate. Composite Sync out and Horizontal Drive are shifted by AC21, Composite Blanking is shifted by AE21; and, Color Burst Gate and Vertical Drive are shifted by AG21. Because the NAND gates invert the signals that were already inverted by the hex inverter, the outputs of the NAND gates are in phase with the outputs of the Sync generator chip. A logic "one" at the output of the shifters is approximately Ø.Ø volts and a logic "zero" is approximately -7.5 volts.

RESET GENERATOR

To properly synchronize the TV Timing and Colorizer Sync generator chip, a reset pulse must be generated about six horizontal drive pulses after the falling edge of the even field vertical drive signal. Refer to Timing Diagram 2.

Working backwards, BE12-A and -B generate a Ø.49 µsec active low reset pulse, beginning Ø.49 µsec after a positive-going edge is applied to the clock input of BE12-A. Because the reset pulse is active low prior to the reset, the D input of BE12-A is inactive high. When clocked, the "one" is presented to the D input of BE12-B. The next rising edge of the 2.Ø4545 Mhz clock input drives the Q/ output of BE12-B low, starting the reset pulse and clearing BE12-A. BE12-B resets on the next clock pulse, ending the reset pulse. Therefore, to generate a reset pulse, BE12-A must be triggered at the sixth horizontal scan after the beginning of the even-field vertical drive pulse.

Programmable synchronous up/down counter BA2Ø generates trigger pulses for BE12-A. The counter is preset to a binary count of Ø1Ø1 (five) and is clocked by the leading rising edge of the horizontal drive signal. The counter operates in the count-down mode and generates a positive-going



RESET TIMING GENERATION

TIMING DIAGRAM-2

6450-0431

Ripple Carry (RC-underflow) on the sixth horizontal drive pulse after the counter is gated on. The counter is gated on during the active-low, odd-field vertical drive pulse only, as described in the next paragraph. Therefore, counter BA2Ø serves as a programmable delay device which generates a clocking output, six horizontal drive periods after the beginning of the odd-field vertical drive.

BA2Ø operation is controlled by T/ (pin 1Ø), P/ (pin 7), and LD (Load-pin 9). Pins 7 and 9 are driven by the Q and Q/ outputs of D-latch BA1. When BA1 is set, P/ is high and LD is low, placing BA2Ø in the load mode. During this time, BA2Ø is inhibited from counting regardless of the level on T/; BA2Ø is preset to a count of five by the levels programmed at the A, B, C, and D inputs. When BA1 is reset, BA2Ø counts down <u>if</u> T/ is also low. T/ is driven by the vertical drive signal and is therefore active low during the <u>even</u> and <u>odd</u> field drive times. Therefore, BA1 inhibits the counting process during the odd drive time. This results in a reset pulse, occurring during the even-field drive time. A reset pulse, received by the TV Timing and Colorizer board during the even-field vertical drive time, is delayed by the TV Timing generator on the TV Timing and Colorizer board so that the composite sync output signals of both chips are synchronized.

BA1 is cleared by the inverted ODD FLD (Odd Field) output of AE1 and remains reset until clocked by the trailing edge of the next vertical drive signal (even field). Thus, BA1 enables counting by BA2Ø only during the even-field drive time.

Refer to sheet 1. The reset output from BE12-B and the pixel clock signal (12.272727 Mhz) are exported to the TV Timing and Colorizer board via complementary output line drivers BC3-C and -B respectively. In addition, a control signal is output via BC3-A. The control signal is used as a switching signal by the TV Timing and Colorizer board.

APPENDIX A

APPENDIX A

SSEC DELIVERED REFERENCE DOCUMENTATION

The listing below is a typical list of reference manuals and may not match your particular installation. This is due to custom installations and system component interchangeability.

A. iSBC 8Ø/24™ SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL by Intel Corporation

B. iSBX 351™ SERIAL MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL by Intel Corporation

C. BULK SEMI MEMORY SYSTEM MODEL DR-129/229/S by DATARAM Corporation

D. BS-101/102 by DATARAM Corporation

E. NTSC CODER TYPE 203/2 by Michael Cox Electronics Limited

F. BIT PAD ONE by Summagraphics Corporation

G. TELEVIDEO 924 by Televideo Systems Inc.

H. CONRAC 7211 by Conrac Division, Conrac Corporation
CONRAC 6242 by Conrac Division, Conrac Corporation (RGB/NTSC)

I. OKIDATA PERSONAL PRINTER USER'S MANUAL by OKIDATA
(MICROLINE 93)

J. McIDAS HOST TO TERMINAL - TERMINAL TO HOST SYSTEM PROTOCOL DESCRIPTION dated 11 September 1984 by SSEC

K. CONRAC 6242 (preliminary) by Conrac Division, Conrac Corporation (RGB/NTSC)