McIDAS

Man computer Interactive Data Access System

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IBM PC/AT® BASED WORKSTATION HARDWARE DESCRIPTION

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PREFACE

This manual was prepared by the Space Science and Engineering Center (SSEC), University of Wisconsin-Madison, to assist you with hardware maintenance of the IBM PC/AT-based Man-computer Interactive Data Access System (McIDAS) workstation.

This manual specifically covers IBM PC/AT-based workstations built since late 1986. Older McIDAS workstations that have been upgraded with an IBM PC/AT may contain several circuit boards (TV Timing, 12-Bit Colorizer, and Joystick) that are different than those described in this manual. Owners of workstations built prior to late 1986 should have received, or should request two copies of the McIDAS Workstation Hardware Description and Appendix B - McIDAS Workstation Hardware Schematics and Assembly Drawings; this documentation should be retained if any of your workstations have been upgraded. If there is a question of documentation applicability, check circuit board modification levels against the modification level cited on the first page of each section of your hardware reference manual(s).

In each workstation, some units are off-the-shelf devices, while others are designed and developed by SSEC. This manual is designed to provide primary documentation for SSEC-developed units and to complement off-the-shelf unit documentation. Therefore, an important part of this manual is a list of reference manuals you should have received with your McIDAS. Appendix A is a typical McIDAS reference manual list.

A brief system overview and detailed workstation overview are followed by unit or circuit board documentation. Each unit or circuit board section includes an introduction, a functional description, and either applicable references for off-the-shelf units or detailed circuit descriptions for custom units.

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McIDAS PC/AT-BASED WORKSTATION OVERVIEW

INTRODUCTION

The McIDAS PC/AT-based workstation is the link between the user and the McIDAS. It provides the animated display of satellite imagery and weather data. An IBM PC/AT computer allows the user to issue commands to the workstation and the host IBM mainframe, and receive alphanumeric information from the host. A large memory system stores image and graphics data; a color monitor is used to view this data, and a mouse or a pair of joysticks is used to position the cursor on the data display. Optionally, a printer is connected to the PC/AT to produce a hardcopy of the alphanumeric information.

A brief description of SSEC's version of the McIDAS is provided to describe how the workstation fits into the total system. Users' systems range from single McIDAS workstations, linked remotely to SSEC's McIDAS, to complete systems like the SSEC McIDAS, to more elaborate systems, similar to SSEC's McIDAS, but with more or different components. The McIDAS workstation description follows the McIDAS system description.

McIDAS SYSTEM DESCRIPTION

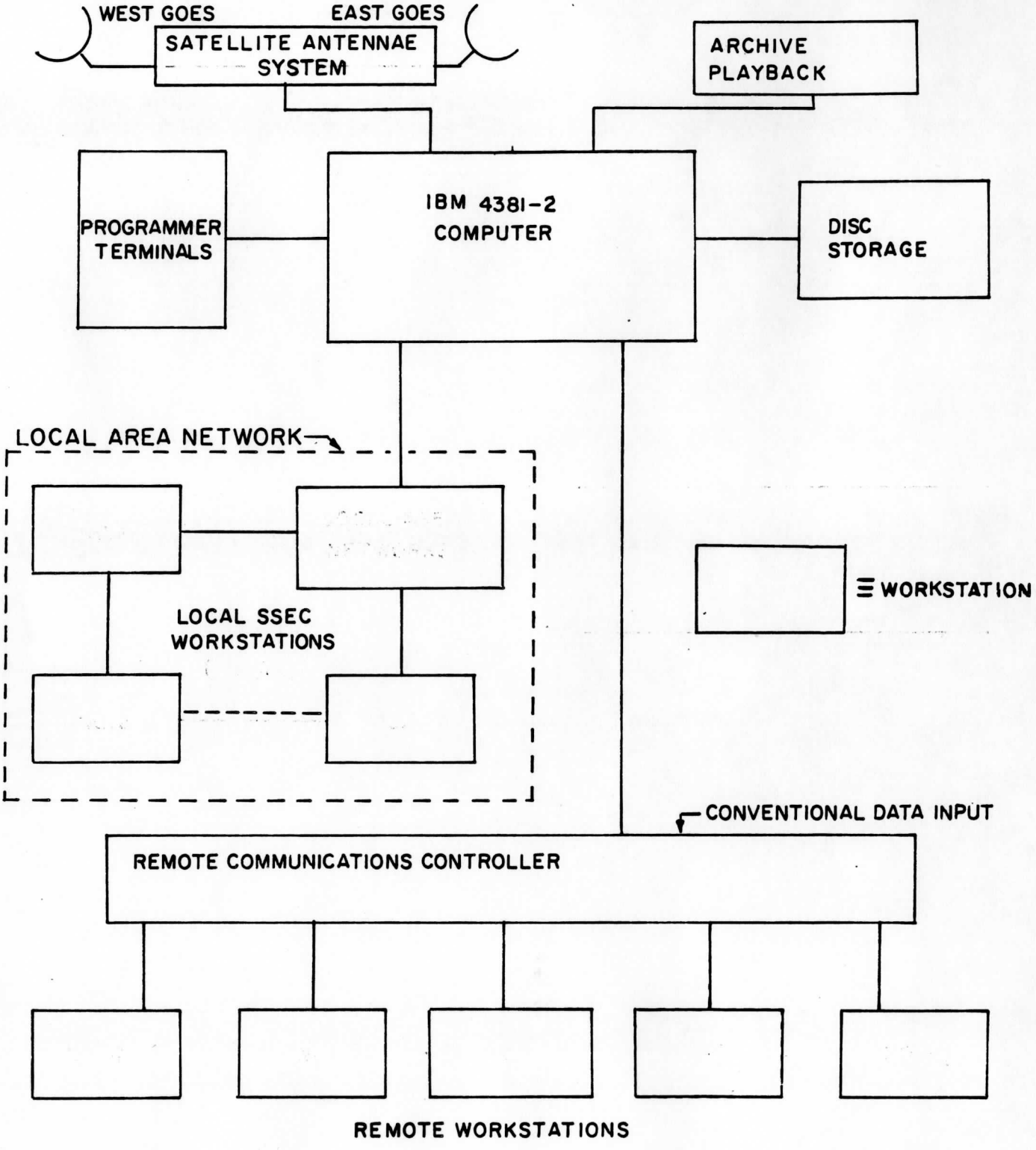
Figure 1 is a block diagram of the SSEC McIDAS. Each block or group of blocks is reviewed in terms of its function within the system.

EAST AND WEST GOES ANTENNAS

The GOES (Geosynchronous Operational Environmental Satellite) antennas receive visible and infrared digitally-encoded images from the East and West GOES satellites.

ARCHIVE/PLAYBACK

The raw GOES data are stored digitally on videocassette cartridges. The playback unit allows GOES raw data to be read into the system, at any time, for user analysis.



McIDAS SYSTEM BLOCK DIAGRAM

FIGURE-1

IBM COMPUTER (4381-2)

The IBM mainframe computer receives imagery data from the GOES antenna group or from archived tapes. The computer contains the operating system, application programs, and subroutines; it functions as a data processor, data base management system, and data analyzer.

DISK STORAGE

Currently, the SSEC McIDAS has a storage capacity of approximately 12.8 gigabytes (12.8 billion bytes). The disk storage is divided into 6999 digital areas in which several data bases reside. The following are three of the major data bases:

- Image Files
- Meteorological Data (MD Files)
- Grid Files

An Image File (area) contains digitized satellite visual data or infrared sensor data.

A Meteorological Data File is a generic file for single-location observations (non-image), designed to accommodate many types of data under one generalized structure.

A Grid File contains fields analyzed at regularly-spaced latitude and longitude locations (grids) from observational data.

PROGRAMMER TERMINALS

The programmer terminals are used for development of system software.

LOCAL AREA NETWORK

The local area network (LAN) provides a high-speed (1Ø Mbits/sec) data link between McIDAS workstations and the IBM computer. McIDAS uses an "off-the-shelf" local area network system, called proNET™, manufactured by Proteon Inc., and an SSEC-fabricated IBM channel interface.

REMOTE COMMUNICATIONS CONTROLLER

The Remote Communications Controller performs the same functions as the LAN but serves remote users. Workstations are usually connected to the Remote Communications Controller by dedicated telecommunication lines maintained by commercial firms such as AT&T. The data speeds (baud rates)

are generally much lower (19.2K bits/sec or less) than those of the LAN. The terms "Local" and "Remote," as applied to workstations in Figure 1, refer to the data link type rather than geographical location. SSEC may have both local and remote workstations within a single room.

CONVENTIONAL DATA INPUT

The McIDAS can ingest a wide variety of conventional weather data. This conventional data input is referred to as "point source" data and is used to maintain the Meteorological Data (MD) data base. Sources for conventional data include radiosondes, rocketsondes, ship reports, aircraft, and radar.

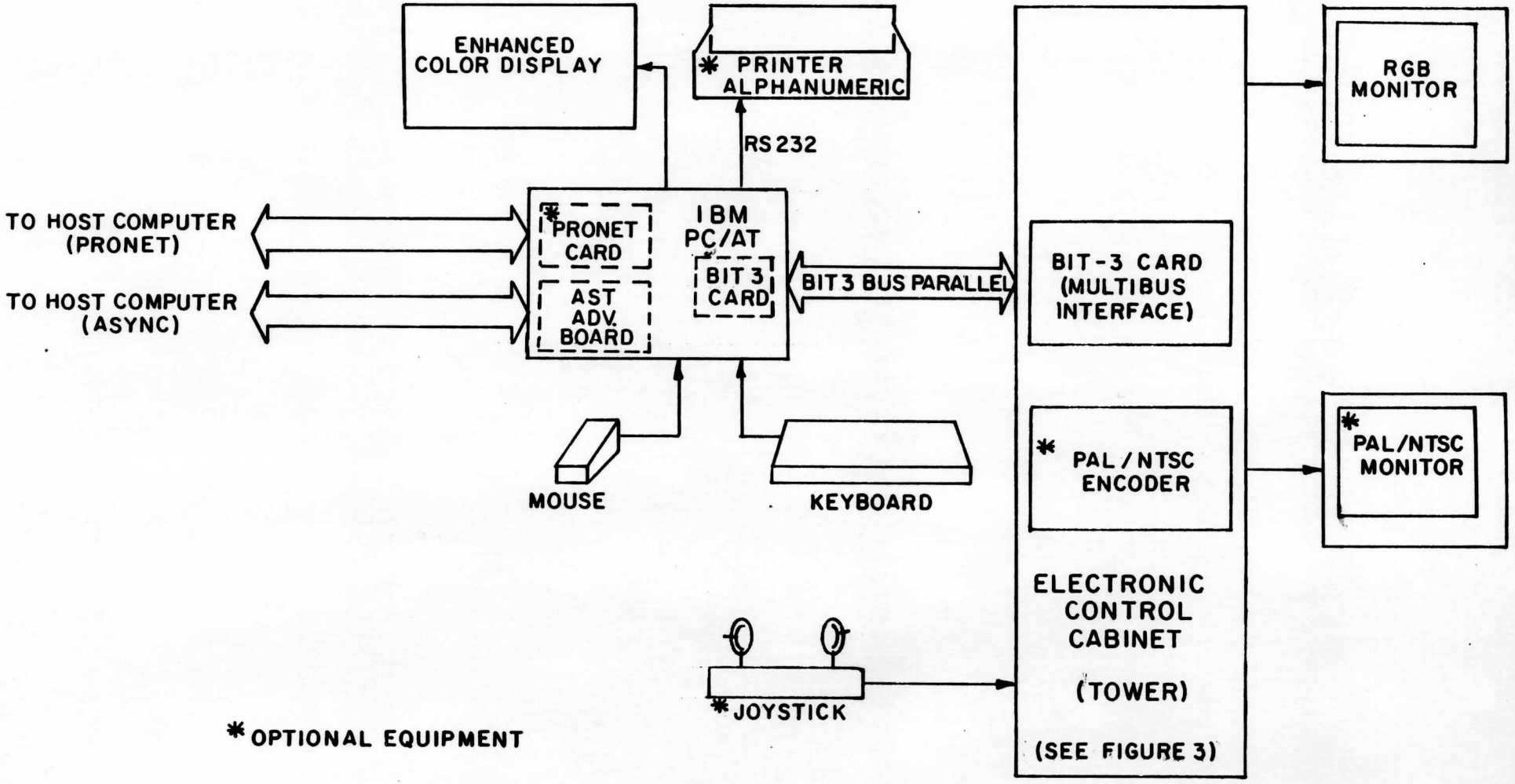
McIDAS WORKSTATIONS

The McIDAS workstation is designed for animated display of satellite imagery and weather data. The following features are included in the workstation:

- real-time access to image and conventional data
- graphics overlays of images without image destruction
- animated displays of image or graphics frames at user-selectable looping rates of up to 15 frames/sec
- pseudocoloring of imagery
- user-selected graphics colors
- manual graphics drawing with joysticks or mouse
- satellite image combinations, forming three-dimensional, color-enhanced images

McIDAS WORKSTATION DESCRIPTION

The Figure 2 block diagram shows the components that constitute a complete workstation. Blocks containing an asterisk (*) may be omitted in some workstations, with a corresponding reduction in workstation capability and flexibility.



MCIDAS-PC/AT WORKSTATION BLOCK DIAGRAM

FIGURE-2

WORKSTATION COMPONENTS

The blocks (components) in Figure 2 are individually addressed according to their functions within the workstation. Some components are standard "off-the-shelf" items and may be substituted with components of similar specifications. When these components are described, component specifications are included, because make and model descriptions are more likely to change frequently.

IBM PC/AT (6- AND 8-Mhz VERSIONS)

The McIDAS workstation evolved over a period of many years. Until recently, the workstation was interfaced directly to the host computer. In this configuration, all computations and meteorological analysis is performed by the host computer, and all user interaction is performed via a CRT terminal.

The IBM PC/AT computer was integrated into the workstation to reduce the host's workload, by performing some of the workstation-related tasks at the workstation. The PC/AT integration process is an evolutionary development process.

The IBM PC/AT equipment group consists of:

- IBM PC/AT computer
- Enhanced Color Display (ECD)
- Keyboard
- Mouse
- BiT-3 MULTIBUS Adapter

IBM PC/AT Computer

Currently, the PC/AT is used in two workstation configurations, a stand-alone configuration, and a full-function configuration. In either configuration, the PC/AT integrates the keyboard, the Enhanced Color Display (ECD), and the mouse into a user interaction terminal.

The PC/AT communicates with the host computer and, in the full-function configuration, with the Electronic Control Cabinet (Tower). Also, the PC/AT reformats data intended for the Tower (full-function configuration) to a Bisync protocol.

The stand-alone PC/AT workstation uses its ECD to display satellite images, graphics, image cursor, and alphanumeric data. To operate in this mode, the PC/AT requires additional memory and an Enhanced Graphics

Adapter (EGA). This type of workstation is frequently referred to as an "EGA-style" workstation. The EGA is required for increased image resolution beyond the IBM Color Graphics Adaptor display resolution. The image resolution is still much less than the full-function workstation. Also, the EGA-style workstation can store a total of 16 image/graphics frames while the full-function system can store up to 128 images, plus a maximum of 64 graphics frames. However, the EGA-style workstation has no image enhancement or combinational abilities. Finally, the EGA-style workstation relies entirely on the mouse for image cursor control. This arrangement is satisfactory for most cursor requirements.

The full-function PC/AT workstation contains the Electronic Control Cabinet (Tower). The Tower provides mass storage for image and graphics storage, color and monochrome monitor interfaces, cursor generation and control, and a monochrome interface.

The IBM PC/AT computer hardware is documented by the manufacturer. Refer to Appendix A for applicable manuals.

Enhanced Color Display (ECD)

The ECD is driven by the PC/AT computer, and can function as an image/graphics monitor as well as an alphanumeric display, when the PC/AT functions as an EGA-style workstation. When the PC/AT is connected to the tower (full-function), the ECD is primarily used to display alphanumeric data. The ECD is documented by the manufacturer (IBM). Refer to Appendix A for additional references.

Keyboard

The keyboard provides the user interaction with the McIDAS. It is a standard keyboard supplied with the IBM PC/AT. The keyboard is documented by the manufacturer. Refer to Appendix A for additional reference information.

Mouse

The mouse provides the PC/AT with cursor control. The mouse performs the same functions as a single joystick in the full-function workstation. Because certain wind measurement processes (WINDCO) require two cursors, controlled by two joysticks, the mouse cannot emulate all cursor functions at this time. The mouse is also used during alphanumeric menu displays for cursor (flashing underline symbol) position.

BiT 3 MULTIBUS Adaptor Card

The full-function workstation consists of the IBM PC/AT equipment group, interfaced to a Tower. Subassemblies and PC cards within the Tower are interconnected by the industry-standard MULTIBUS™ (MULTIBUS is a registered trademark of INTEL Corporation). The IBM PC/AT requires an adapter to make it compatible with the MULTIBUS.

BiT 3 Computer Corporation manufactures a two-card adaptor set which interfaces the PC/AT to the MULTIBUS. One card plugs into the PC/AT, while the other plugs into the MULTIBUS. The two cards are interconnected by two 5Ø-conductor flat cables. The MULTIBUS Adaptor cards are documented by BiT 3. Refer to Appendix A for references.

COLOR MONITOR (RGB)

The CONRAC 7211 is a standard RGB (red, green, blue) color monitor, used to display color and monochrome images and graphics. The inputs to the monitor are red, green, and blue drive signals and composite sync signals from the electronic control cabinet. The monitor is driven to a resolution of 64Ø visible picture elements (pixels) by approximately 48Ø visible scan lines. The CONRAC 7211 is commercial equipment, documented by the manufacturer. Any high-resolution RGB monitor can be substituted for the CONRAC 7211.

NTSC/PAL MONITOR

The full-feature workstation (Tower) contains a PAL (Phase Alternating Line) encoder or an NTSC (National Television Standards Committee) encoder. An NTSC or PAL monitor can be used to display the composite video output of this encoder. The monitor is not essential for workstation operation and therefore may be eliminated.

PRINTER

The printer produces hardcopy maps, tables, or listings. The printer is not essential for workstation operation and therefore may be eliminated. The printer is interfaced to the workstation via an RS-232 port in the IBM PC/AT, typically at a baud rate of 48ØØ bits per second. Currently, an OKIDATA Microline® 293 printer is used. The OKIDATA Microline® 293 is a standard commercial printer, documented by the manufacturer.

JOYSTICKS

The Joystick module positions the cursor on the monitor. The module consists of two joysticks, containing two potentiometers and an electronics board. The potentiometers supply analog position information to the electronics board. The electronics board transforms the analog input data to digital data and serially transmits this data to the Electronic Control Cabinet. Typically, the right joystick provides coarse position control while the left provides vernier (fine) control. The data is transmitted as 8-bit ASCII, with two stop bits, parity, and one start bit. The parity bit is always transmitted as a logic "one". The electronic mouse can perform most joystick functions; thus, the joysticks are optional in some applications.

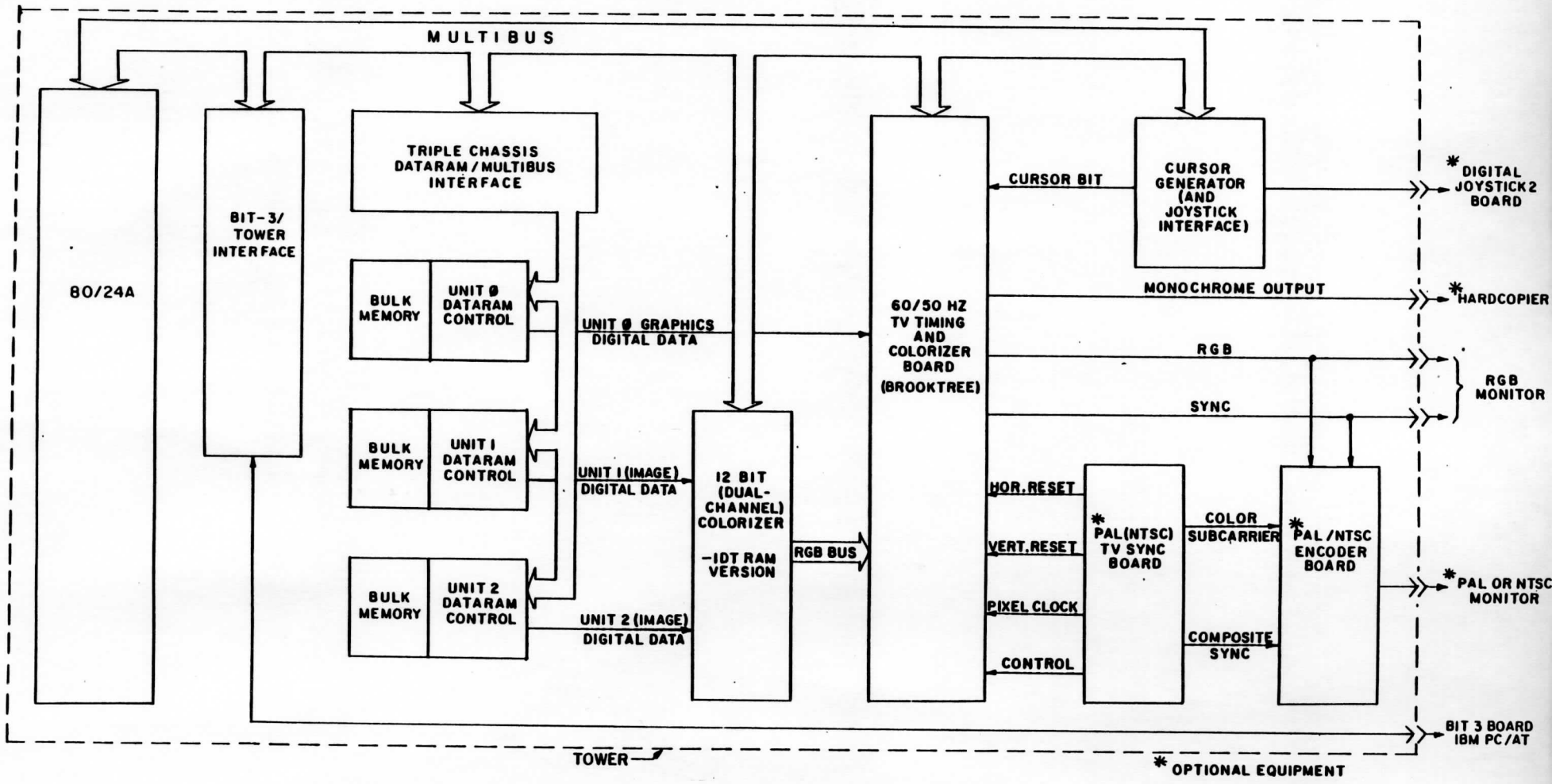
ELECTRONIC CONTROL CABINET (TOWER) OVERVIEW

Figure 3 is a block diagram of the workstation, showing the Electronic board, Control Cabinet, and external components. Except for the DATARAM memory storage, the BiT 3, and the Intel 8Ø/24A microprocessor board, all control cabinet blocks are designed and built by SSEC. The Electronic Control Cabinet is a standard 19-inch rack, often referred to as "the Tower."

MICROPROCESSOR

The microprocessor controls the data flow between the various boards and components in the workstation. It also controls communications between the IBM PC/AT and the Electronic Control Cabinet. The microprocessor accepts commands or data "packets" from the PC/AT, decodes the command or destination-device-address, and executes the command or data transfer.

The microprocessor is an Intel iSBC 8Ø/24A single-board computer, having 8K bytes of on-board RAM. The board supports a maximum of 32K bytes of EPROM (Erasable Programmable Read Only Memory). Three of the available four EPROM chips contain the microprocessor's instructions, constants, and most tables. The fourth EPROM chip contains only a video image compression table. (Refer to the 12-Bit (Dual Channel) Colorizer-IDT RAM Version overview.) The board supports one serial I/O (Input/Output) device via the J3 jack. The J3 jack is connected to the CRT terminal during diagnostic testing. The 8Ø/24 board uses an Intel 8Ø85A 8-bit



FUNCTIONAL BLOCK DIAGRAM
ELECTRONIC CONTROL CABINET (TOWER)

FIGURE-3

microprocessor for the central processor unit; it performs on-board processing as well as on- and off-board control.

CABINET/CHASSIS

The Electronic Control Cabinet (Tower) is a standard 19-inch electronics rack. The rack has an overall height of 56 inches, including the casters. The cabinet has an overall depth of 3Ø inches and width of 24 inches. The rack has a front opening of 44 inches by 19 inches and houses the following five 19-inch modular electronic units:

- PAL/NTSC Encoder (optional)
- MULTIBUS chassis
- DATARAM memory storage (units Ø, 1, and 2)

Each module contains its own DC power supply which plugs into a switched convenience AC outlet panel, located near the bottom rear of the cabinet.

The PAL/NTSC Encoder is located at the top of the cabinet (when installed) and enables the workstation to produce NTSC or PAL composite color video. The composite color video can be used to drive an optional NTSC or PAL Color Monitor and modulate a commercial TV transmitter. The PAL/NTSC Encoder is designed and manufactured by SSEC and is documented in Section 1Ø of this manual.

The MULTIBUS chassis was designed and is fabricated by SSEC. Boards are accessed through the front of these SSEC enclosures. The MULTIBUS chassis contains its own DC power supplies and a card cage that accepts up to nine PC cards.

All boards within the card cage are interconnected by the card cage backplane, through a bus structure called MULTIBUS^{R}. MULTIBUS is registered trademark of Intel Corporation and has become an industry standard. The standard is now controlled by IEEE (IEEE 796). The P1-bus consists of 16 address lines, 8 data lines, control lines, interrupt lines, and bus exchange lines.

All SSEC boards, housed in the card cage, are designed to be MULTIBUS-compatible with the P1 connector. SSEC uses the P2 connector for various McIDAS-specific timing and video signals.

The DATARAM memory storage units are located below the MULTIBUS chassis. A DATARAM control board, built by SSEC, is located in each of the memory storage units. The DATARAM control board connects the MULTIBUS to the memory storage system via the Triple Chassis DATARAM/MULTIBUS

Interface. Additional information on the Memory Storage Unit is found in the next section of the Overview (Memory Storage System).

MEMORY STORAGE SYSTEM

The Memory Storage System consists of three separate memory storage units. One unit stores graphics overlay data while the other two units store compressed image data. Each unit can be populated with from one to four storage array boards. Each array board provides storage for 16 frames of video data. Increasing with the number of array boards, the memory storage unit can store 16, 32, 48, or 64 graphics frames and 32, 64, 96, or 128 image frames.

In response to the significant amount of memory required for video storage, SSEC developed a memory control board that allows the microprocessor to store images and graphics in the Memory Storage Units. These data are automatically retrieved when the microprocessor addresses the unit via a frame number for read operations. Video data is stored one pixel at a time by addressing the frame number, video line number (Ø-511), and pixel position within that line (Ø-639). Video data is read sequentially beginning with the starting address and ending with the last pixel address of the frame. The read process is repeated until the user selects a different frame number. During the read process, data is read sequentially by the Control board and output to the 12-Bit (Dual Channel) Colorizer-IDT RAM Version board (image data) or the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree (graphics) board, at TV pixel painting rates. See the manufacturer's literature for more information on the memory storage modules.

12-BIT (DUAL CHANNEL) COLORIZER-IDT RAM VERSION

The 12-Bit (Dual Channel) Colorizer-IDT RAM Version board expands (decompresses) the two 3-bit video image channels into two 6-bit channels. The 6-bit channels are used as address inputs to an enhancement table. The table is user-programmable via the host computer. The 15 binary output bits from the table are divided into three 5-bit buses which represent magnitudes of red, green, and blue (RGB) drive signals. The table provides a means to assign color drive intensities (pseudocolors) as a function of the 6-bit image channel inputs, individually or in combination with each other.

6Ø/5Ø HZ TV TIMING AND COLORIZER-BROOKTREE

The RGB bus signal outputs from the 12-Bit (Dual Channel) Colorizer-IDT RAM Version board are inputs to the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board. The 3-bit graphics bus and the cursor bit are also inputs to this board. This board does the following:

- generates all TV timing signals
- multiplexes image, graphics, and cursor data
- converts the digital video into analog video, suitable for driving a standard RGB monitor
- assigns color to the graphics and cursor data

The TV timing signals are horizontal and vertical drive signals, used by frame-processing logic; PXLCK (pixel clock), used for timing and synchronization of all digital video signals; and composite sync, used by the RGB monitor.

Each pixel, as seen on the RGB monitor screen, is either an image pixel, a graphics pixel, or a cursor pixel. The TV Timing and Colorizer board assigns priority to the pixel type, from highest to lowest, as follows:

- cursor
- graphics
- image

Graphics bits are processed by a color enhancement table, similar to the process by which image color enhancement is performed on the 12-Bit (Dual Channel) Colorizer-IDT RAM Version board. For each cursor bit value ("Ø" or "1"), eight colors can be loaded into the table; the 15 RGB outputs of the lookup table result in 32,768 user-selectable colors and brightness levels.

The digital RGB video data is applied to the digital-to-analog (D-to-A) converters, combined with composite sync and output to the RGB monitor. The TV Timing and Colorizer board also provides a monochrome output to drive hard copiers.

CURSOR GENERATOR

The Cursor Generator combines two unrelated functions. This board generates the cursor symbol, and interfaces the serial input joystick data to the microprocessor.

When the user positions the joysticks, the joystick board generates a serial output data stream containing cursor position information. The Joystick Interface section of this board converts the serial data stream to parallel data; parallel data is transmitted via the MULTIBUS to the microprocessor.

The microprocessor updates its stored cursor position registers and transmits the updated values back to the Cursor Generator portion of the board. The microprocessor also transmits cursor symbol size and shape information. The Cursor Generator uses these input parameters and TV timing signals to determine if the pixel (on the RGB monitor) about to be painted is a cursor pixel. If the pixel is a cursor pixel, a cursor bit is sent to the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board.

HOST/WORKSTATION INTERFACE

Early versions of the McIDAS workstation communicated directly with the host via Bisync, a subset of the IBM Bisync communications protocol. Bisync transfers data from a data source to a data receiver in the form of message packets. SSEC designed and uses a protocol which is embedded into the data portion of the Bisync protocol. This protocol (referred to hereafter as the "workstation protocol") is documented in the MIDDS Host to Terminal - Terminal to Host System Protocol Description, dated 26 June 1985 by SSEC (Rev. Level 1). The communications protocol is half duplex, byte oriented, and binary synchronous. Host software and workstation hardware and firmware evolved using this communications scheme. Backward compatibility of new communications schemes and workstation design were maintained to allow owners of older systems to update their systems.

Later in the workstation development history, a local area network (LAN) system was developed to connect several workstations within a limited physical area to a host computer. The system is designed around a proprietary LAN designed and fabricated by Proteon Inc. The LAN is known as proNET™, and features a data throughput rate of 1ØMbits per second. A drawback of the system was that the LAN reformatted the Bisync message packets by embedding the Bisync protocol in the proNET protocol, impeding the desired backward compatibility. A solution to this problem was to sandwich the proNET™ LAN between two SSEC-designed and -fabricated message protocol adapter cards. This arrangement allows the host software

and the workstation hardware and firmware to remain virtually unchanged when the McIDAS is interconnected via the LAN. Thus, the workstations and host perform as if they are connected via a Bisync link.

The latest generation of the McIDAS workstation contains a PC/AT computer. Because of its diverse communications capability, the PC/AT is functionally located in the communications path between the Tower and the host. Protocol conversion by the PC/AT is an advantage of performing all host to workstation-workstation to host communications via the PC/AT. Thus, the Tower communications firmware and hardware can remain virtually unchanged, if the PC/AT communicates with the Tower, through the Bisync protocol.

The PC/AT does not have Bisync capability, and its internal bus structure is incompatible with MULTIBUS. The following paragraphs describe the solutions to these problems.

A bus-to-bus converter called a Multibus Adapter, designed and manufactured by BiT 3 Computer Corporation, solves the PC/AT bus-to-MULTIBUS incompatibility problem. The MULTIBUS Adapter consists of two boards. One board plugs into the PC/AT while the other plugs into the Tower. The two boards are connected by two 5Ø-conductor ribbon cables. The MULTIBUS adapter contains a bi-ported RAM which resides in the MULTIBUS and PC/AT address domains. The bi-ported RAM serves as a two-section message packet buffer. One section of the buffer functions as a transmit buffer; the other section functions as a receive buffer.

The Tower interrupts the PC/AT to inform it when it will accept message packets. The Tower produces these interrupts at a 3Øhz rate; they occur on alternate vertical retrace intervals. The message packets, transmitted to the Tower from the PC/AT, have the same message packet format as that formerly transmitted from the host to the workstation (Bisync).

The Bisync communications scheme was replaced by Async for greater data transmission efficiency and compatibility with the PC/AT. The Async and Bisync protocols are different. The Bisync protocol (also known as Ø2,Ø3) contains embedded framing characters, begins with an ASCII Ø2 (STX-Start of Text), and ends with an ASCII Ø3 (ETX-End of Text). The Ø2,Ø3 protocol gets its name from the STX and ETX codes. The Async protocol begins each message packet with FØH, and is sometimes referred to as the "FØ protocol." Each async message packet contains a message-type

identification code. One of the message types is an Ø2,Ø3 protocol. Thus, the FØ protocol can embed an Ø2,Ø3 type message.

Because the protocols are different, the host communicates with the workstation via a protocol converter, allowing host software to remain Ø2,Ø3 protocol oriented.

The protocol converter is connected to the PC/AT via a pair of high-speed, error-correcting modems, such as Fastlink modems. These modems feature several carriers and automatically adjust baud rates and select the most error free carriers to maintain reliable communications at the highest baud rates. The modems allow communications over commercial telephone lines and/or dedicated lines at baud rates of up to 19.2K bits per second. These modems are self-pacing, using X-on/X-off to start and stop data transmissions respectively.

There are two conditions under which message packets are generated by the PC/AT. First, "workstation protocol" messages are transmitted from the host to the PC/AT by embedding the "workstation protocol" into the Async protocol. The PC/AT extracts the workstation protocol from the Async message, embeds it into a Bisync formatted message, and forwards the packet to the Tower. Second, the PC/AT interprets single-character user's commands entered at its keyboard and forms Bisync formatted packets. These packets are transmitted to the workstation where they are executed by the Tower. These messages contain image and graphics frame control, and cursor control.

Several messages are transmitted from the Tower to the PC/AT, but only the following are processed:

- ID response - the response contains the Tower's ID, maximum number of image frames, and maximum number of graphics frames. The PC/AT ignores the ID, but retains the remaining data.
- raw joystick data - the Tower sends joystick position data.
- Tower cursor state - the Tower sends cursor size and position data to the PC/AT.

Proteon Inc. designed and fabricated a proNET adapter board which is optionally installed in PC/AT workstations that use proNET. The PC/AT converts incoming proNET formatted messages to Bisync format and forwards them to the Tower via the MULTIBUS adapter. For messages from the PC/AT or Tower to the host, the PC/AT converts the messages to proNET-compatible format.

The BiT 3 MULTIBUS Adapter interfaces the MULTIBUS to the PC/AT; the memory addresses and I/O ports residing on the MULTIBUS can be accessed by the PC/AT. However, at present, all MULTIBUS I/O port accesses are made only by the 8Ø/24A card. The capability of the PC/AT to address the MULTIBUS I/O ports is a design feature that allows expansion of the PC/AT's role in the McIDAS workstation. The following paragraph describes the integration of this feature.

The PC/AT addresses I/O ports with a 3-digit hexidecimal (hex) addresses (Ø-7FFH). Any block of I/O addresses, not used internally by the PC/AT or any of its optional adapter cards, can be assigned as MULTIBUS I/O ports, via programming on the MULTIBUS Adapter board. The 8Ø85 microprocessor on the 8Ø/24A microcomputer card addresses I/O ports using a 2-digit hex address. Furthermore, the 8Ø85 writes the port address to both the upper eight bits and the lower eight bits of the MULTIBUS. This allows the MULTIBUS board designer the option of decoding specific I/O port addresses using the upper, lower, or combinations of the upper and lower eight bits of the MULTIBUS address bus. Because of the 8Ø85's port addressing scheme, PC/AT port addresses may appear at first glance to have little relativity to the 8Ø/24A's port addresses. Table 2 shows the port address correspondence and the portion of the MULTIBUS that is used by the specific board for the port address decode.

8Ø85 port	PC/AT port	Board	Decode
BØH	B328H	Dual Channel Col.	Upper four bits and lower three bits
B1H	B329H	Dual Channel Col.	"
B2H	B32AH	Dual Channel Col.	"
B3H	B32BH	Dual Channel Col.	"
73H	7328H	TV Timing and Col.	Upper eight bits
83H	8328H	TV Timing and Col.	"
93H	9328H	TV Timing and Col.	"
38H	Ø338H	Cursor/Joy	Lower eight bits
39H	Ø339H	Cursor/Joy	"
3AH	Ø33AH	Cursor/Joy	"
3BH	Ø33BH	Cursor/Joy	"
3CH	Ø33CH	Cursor/Joy	"
3DH	Ø33DH	Cursor/Joy	"
3EH	Ø33EH	Cursor/Joy	"
3FH	Ø33FH	Cursor/Joy	"

Table 2

In addition to the PC/AT port addresses shown in Table 2, the PC/AT uses port addresses Ø3ØØH-Ø3Ø7H for the proNET™ Adapter card. Finally, the BiT 3 MULTIBUS Adapter card requires several I/O port addresses for board control. These ports are available to both the MULTIBUS and the PC/AT. The MULTIBUS port addresses 7CH-7FH correspond to PC/AT port addresses Ø32ØH-Ø323H, and are used for BiT 3 MULTIBUS Adapter board control.

Regardless of interface type (proNET or Async), bisync protocol data is transferred between the PC/AT and the Tower. The PC/AT performs required protocol conversion on the workstation end of the communications interface. Host-to-workstation message transmissions consist primarily of:

- ASCII text to the ECD
- ASCII text to the printer
- graphics plotting parameters (starting points, line lengths and directions)
- pseudocoloring table loading data
- TV image data
- cursor size, shape, and position
- image looping parameters
- graphics and cursor color palette loading data
- workstation ID number
- TV frame numbers

Workstation-to-host message transmissions consist primarily of:

- keystroke characters
- workstation ID, including number of image and graphics frames available (generally ignored by the IBM host)
- TV image and graphics display status--frame number shown and upper and lower loop bounds
- raw joystick position data

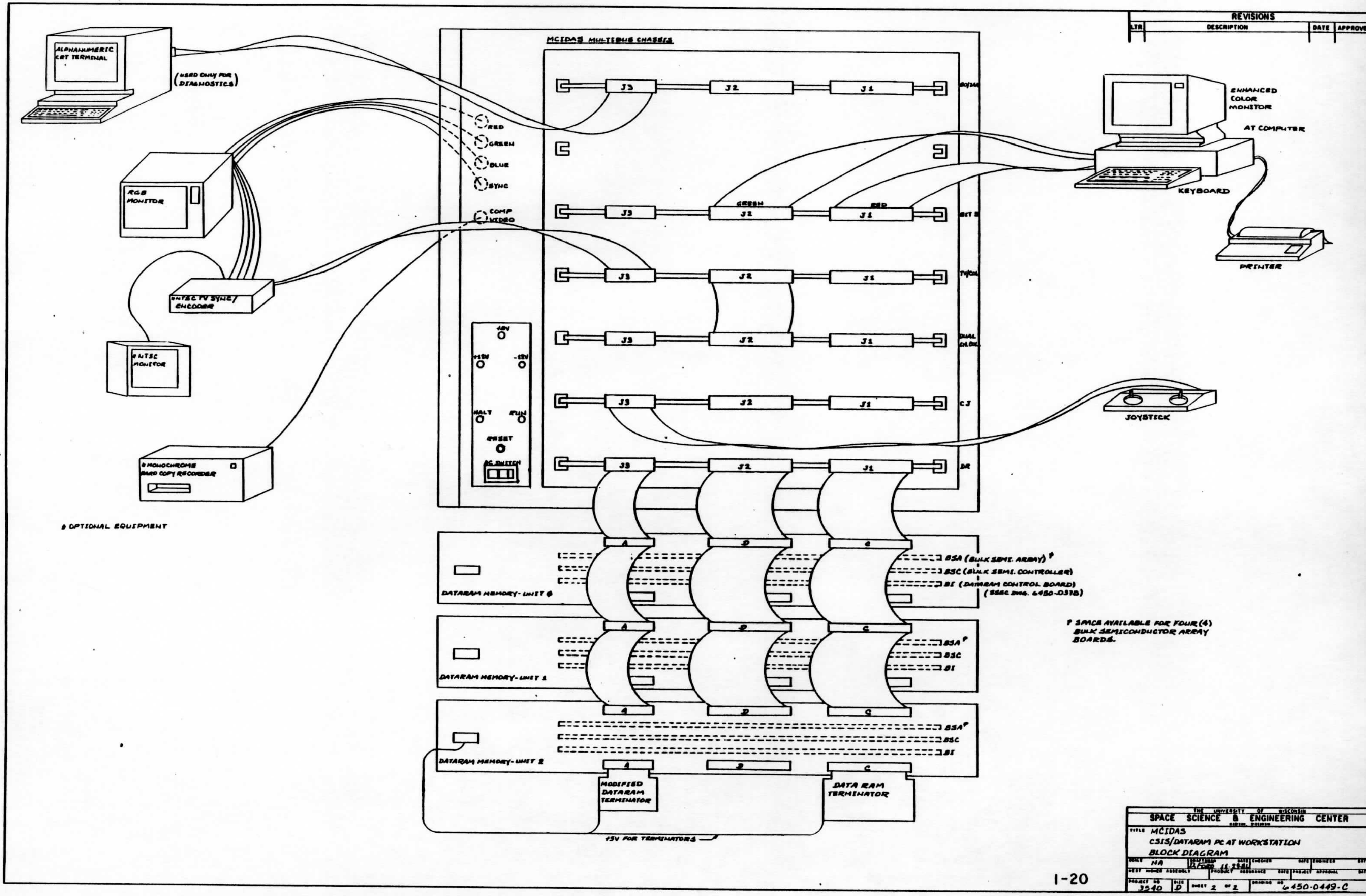
WORKSTATION SUMMARY

The workstation is best summarized by tracing a user's command through the system. For this example, assume the user wants to transfer an image frame to the workstation. Refer to Figure 4. The user types the proper sequence of characters at the PC/AT's keyboard to request the desired image from the host. (The input data format is located in the

McIDAS Applications Guide.) The PC/AT formats the command into a message packet and transfers the packet to the Host. The host deciphers the received packet, determines that the workstation has requested an image frame, and transmits the image, line by line.

The host forms each image line into a 642-byte packet, consisting of a two-byte image line number and 64Ø six-bit pixel data values. The host transmits the packets to the workstation's PC/AT. The PC/AT forwards the packet to the Tower. The microprocessor strips the "image line number" from the message packet and transfers this data to the appropriate Memory Storage Unit's DATARAM control board. The DATARAM control board loads the image line number into the pixel address generation section of the DATARAM control board. Now, the microprocessor processes each of the 64Ø six-bit pixel data values in a compression algorithm. The algorithm reduces the 6-bit pixel data to 3-bit pixel data, thereby reducing the memory storage requirements by 5Ø percent. After each pixel is processed, it is transferred to the DATARAM control board, which loads the pixel into memory and increments the pixel address counter. This process continues until each of the 64Ø pixels have been processed and stored. For each image frame, a total of about 49Ø packets (as described above) are transferred from the host and processed and stored by the workstation.

4/PCAT/01


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
ALPHANUMERIC CRT TERMINAL
(USED ONLY FOR DIAGNOSTICS)
MCIDAS MULTIBUS CHASSIS
J3
J2
J1
RED
GREEN
BLUE
SYNC
COMP VIDEO
RGB MONITOR
NTSC TV SYNC/ ENCODER
NTSC MONITOR
MONOCHROME HARD COPY RECORDER
+5V
+12V
-12V
HALT
RUN
RESET
AC SWITCH
BIT
CJ
DR
ENHANCED COLOR MONITOR
AT COMPUTER
KEYBOARD
PRINTER
JOYSTICK
* OPTIONAL EQUIPMENT
BSA (BULK SEMI. ARRAY)
BSC (BULK SEMI. CONTROLLER)
BI (DATARAM CONTROL BOARD)
(SSEC DWG. 6450-0318)
DATARAM MEMORY - UNIT 0
DATARAM MEMORY - UNIT 1
DATARAM MEMORY - UNIT 2
BSA
BSC
BI
A
D
C
SPACE AVAILABLE FOR FOUR (4) BULK SEMICONDUCTOR ARRAY BOARDS.
MODIFIED DATARAM TERMINATOR
DATA RAM TERMINATOR
+5V FOR TERMINATORS
THE UNIVERSITY OF WISCONSIN
SPACE SCIENCE & ENGINEERING CENTER
TITLE MCIDAS
CSIS/DATARAM PC AT WORKSTATION
BLOCK DIAGRAM
SCALE NA
PROJECT NO 3540
SIZE D
SHEET 2 OF 2
DRAWING NO 6450-0449-C

SECTION 2
SINGLE BOARD COMPUTER
TABLE OF CONTENTS

SINGLE BOARD COMPUTER

INTRODUCTION

The Single Board Computer consists of an Intel® iSBC 8Ø/24A™ single board microcomputer. This document provides only a functional overview of the Single Board Computer. For complete hardware documentation of the iSBC 8Ø/24A™, see Intel®'s iSBC® 8Ø/24A SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL (Manual order number 148437-ØØ1). Note: Intel, iSBC, and MULTIBUS are registered trademarks of Intel Corporation.

For a more complete understanding of the McIDAS workstation and system, it is necessary to understand the workstation/host interface protocol, the workstation operational firmware[1] and the diagnostic firmware. The workstation/host interface protocol is described in the SSEC document, HOST TO TERMINAL - TERMINAL TO HOST SYSTEM PROTOCOL DESCRIPTION, dated 11 September 1984.

The operational and diagnostic firmware is documented in the McIDAS WORKSTATION FIRMWARE DESCRIPTION.[2]

HARDWARE FUNCTIONAL DESCRIPTION

The 8Ø/24A provides the processing power necessary to oversee all Tower processes and maintain a communications link between the PC/AT and the Tower. This board receives data from the PC/AT's MULTIBUS Adapter and steers it to the proper workstation device, and collects status information and data from that device, packing it into a message for transmission to the PC/AT.

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[1] The term "firmware" describes programs stored in non-volatile EPROM that may be altered by the user.

[2] This document is not yet completed. It will be forwarded to you upon completion.

The 8Ø/24A board is built around the Intel 8Ø85A microprocessor chip. The address, data, and control lines of the microprocessor are not only connected to other on-board chips, they are connected to most other electronic control cabinet boards via the MULTIBUS and MULTIBUS interface logic. Note: For additional information on the MULTIBUS, refer to Intel's MULTIBUS® DATA BOOK (Order number 21Ø893-ØØ3).

The iSBC 8Ø/24A™ board (referred to as the "8Ø/24A") is a MULTIBUS-compatible computer system. The board contains 8K bytes of RAM and 32K bytes of erasable-programmable-read-only-memory (EPROM). The board has six 8-bit I/O ports and one programmable serial communications channel.

Figure 1 is a functional block diagram of the iSBC 8Ø/24A.

MICROPROCESSOR

The microprocessor executes the commands of the workstation firmware package. The microprocessor goes to the EPROM memory block, retrieves the instruction to be executed, and carries out the assigned task. The 8Ø85A microprocessor deciphers the instructions and initiates their execution.

MEMORY AND I/O MAPPING

All controllable devices external to the microprocessor are assigned a memory address or an I/O address. The Memory and I/O Mapping block in Figure 1 generates the device-enabling signals by processing the microprocessor's address bus output and IO/M control signal. IO/M is high when the microprocessor performs an I/O read or write operation and is low when it performs a memory read or write operation. I/O read and write addressing places an identical binary address on the lower and upper eight bits of the address bus, and represent port addresses of ØØH-FFH (hexadecimal). Memory read and write operations use all 16 address bus lines (ØØØØH-FFFFH). The memory and I/O mapping block only provides address deciphering for on-board memory and I/O devices. Each device external to the 8Ø/24A board (off-board) that is addressable by the microprocessor (via the MULTIBUS) must provide its own memory or I/O mapping logic. The External Bus Interface provides the MULTIBUS with all address and control lines necessary to perform memory and I/O mapping.

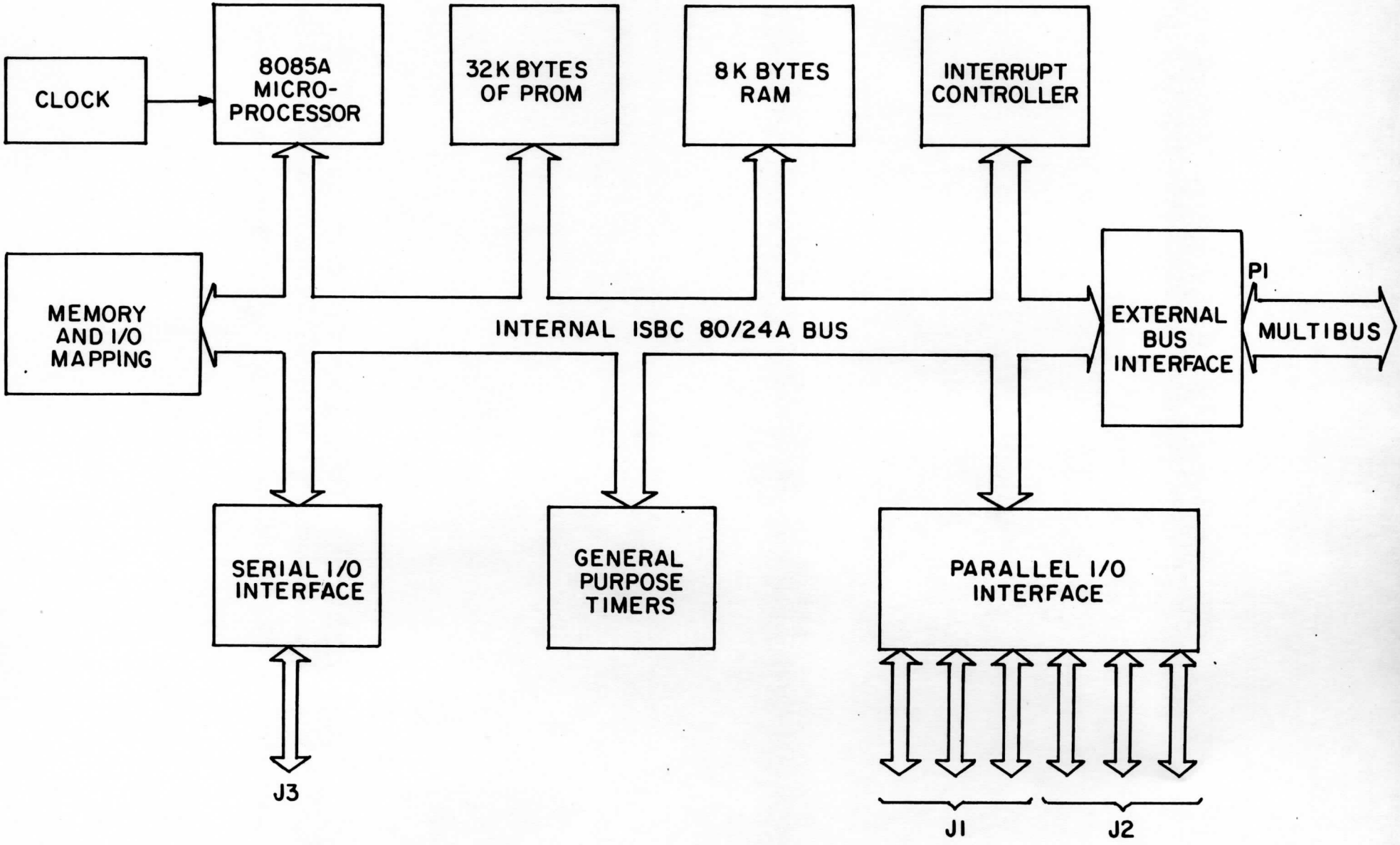


FIGURE 1 - MICROPROCESSOR BOARD FUNCTIONAL BLOCK DIAGRAM

The iSBC 80/24A and all other workstation boards and devices are memory and I/O mapped, as shown in Table 1 below.

8085 ADDRESS/PORT	I/O-MEMORY	FUNCTION
0000H - 5FFFH	Memory (EPROM)	Instruction code (80/24A)
6000H - 7FFFH	Memory (EPROM)	Video compression (8024A)
8000H - 9FFFH	Memory (RAM)	BiT 3 Communications Buffer
A000H - BFFFH	Memory (RAM)	General (80/24A)
C000H - EFFFH	Memory	Dual channel colorizer enhancement tables
F000H - FBFFH	(not used)	
FC00H - FC7F	Memory	DATARAM control addresses
FC80 - FEFFH	(not used)	
FF00H - FF3F	Memory	Graphics enhancement palette
FF40 - FF7F	Memory	Cursor enhancement palette
FF80 - FFFF	(not used)	
00 - 37H	(not used)	
38H - 3FH	I/O (Input)	Cursor/Joy Board Joystick Position Data
73H	I/O (Output)	TV Timing and Colorizer Graphics Enable
74H-76H	Not used	
77H	I/O (Input/Output)	Bisync Control
78H - 7BH	I/O (Output)	Cursor/Joy Board Cursor Size and Control
7CH - 7FH	I/O (Input/Output)	BiT 3 MULTIBUS Adapter Board Control
80H - 82H	(not used)	
83H	I/O (Output)	TV Timing and Colorizer - Image Enable
84H - AFH	(not used)	
93H	I/O Input	TV Timing and Colorizer Vertical Interval
B0H	I/O (Output)	Dual Channel Colorizer - Mask and Control Register Load
B1H	I/O (Output)	Dual Channel Colorizer - Mask and Control Register Load
B2H	I/O (Output)	Dual Channel Colorizer - Firmware Backward Compatibility Support
B3H	I/O (Output)	Dual Channel Colorizer - Firmware Backward Compatibility Support
B4H - D9H	(not used)	
DAH	I/O (Input/Output)	80/24A Interrupt Controller
DBH	(not used)	
DCH	I/O (Input/Output)	80/24A - Timer #0 Read/Load
DDH	I/O (Input/Output)	80/24A - Timer #1 Read/Load
DEH	I/O (Input/Output)	80/24A - Timer #2 Read/Load
DFH	I/O (Output)	80/24A - Timer Mode Control
E0 - E3	(not used)	
E4H	I/O (Input)	80/24A - iSBX 351 Baud Rate Select (Line Printer)
E5H	I/O (Input)	80/24A - Number of Image Frames
E6H	I/O (Input)	80/24A - Number of Graphics Frames
E7H	I/O	(Not used)
E8H	I/O (Input)	80/24A - Workstation ID Number
E9H - EBH	(not used)	
ECH	I/O (Input/Output)	80/24A - USART Data (CRT)
EDH	I/O (Input/Output)	80/24A - USART Command/Status
EEH-EFH	I/O	(Not used)
F0H	I/O (Input/Output)	80/24A - iSBX 351 USART Command/Status
F1H	I/O (Input/Output)	80/24A - iSBX 351 USART Data (Line Printer)
F2H - F9H	(not used)	
FA	I/O (Input/Output)	80/24A iSBC 351 Timer #2 Control
FB	I/O (Output)	80/24A iSBC 351 Timer Mode Control
FC - FFH	(not used)	

Table 1. 8085 Memory and I/O Mapping

EPROM

The first 24,576 (ØØØØH - 5FFFH) bytes of EPROM are used by the microprocessor for non-volatile instruction storage. Included in this block are tables and constants. The last 8192 bytes of storage (addresses 6ØØØ - 7FFF) make up a special table used to compress the image data from six bits per pixel to three bits per pixel. The compression process reduces image storage requirements by half.

RAM

The RAM block is an 8192-byte static RAM. The RAM stores variables, system configuration, status and other scratch pad data.

SERIAL I/O INTERFACE

The serial I/O Interface block provides a Serial RS-232C communications link to an external device, via the J3 Port. In older style workstations J3 connects to a CRT terminal. The PC/AT replaces the CRT terminal by serving as an intelligent terminal. J3 is used to connect a CRT terminal to the tower during diagnostic testing.

GENERAL PURPOSE TIMER

The general-purpose Timer block contains three independent timers. The timers are software-programmable and may be configured as frequency generators, interval timers, and real-time interrupt generators.

PARALLEL I/O INTERFACE

The Parallel I/O Interface block provides six general-purpose 8-bit parallel I/O ports. In McIDAS, only five ports are used. All ports are configured as inputs ports only. Ports E4, E5, and E6 are connected to connector J1 while E8, E9, and EA are connected to connector J2. Programming connectors are connected to J1 and J2, are used to program the selected port input pins. During initialization, performed by the microprocessor immediately after a power turn-on or system reset, the microprocessor reads ports E4, E5, E6, E8 and E9 to determine the following:

- number of video frames - port E5
- number of graphics frames - port E6
- system AC power frequency (5Ø hz or 6Ø hz) - port E9
- workstation ID number - port E8

INTERRUPT CONTROLLER

The microprocessor can directly control four interrupt sources. In McIDAS, all four direct sources are grounded (disabled). The Interrupt Controller block can control eight additional interrupt sources (indirectly). The Interrupt Controller contains an integral priority scheme which arbitrates contention among interrupts. Jumpers connect system interrupts to the selected interrupt priorities. In the McIDAS, three interrupt sources are controlled by the Interrupt Controller. The Vertical Interval on the TV Timing and Colorizer board generates a rate of 3Ø interrupts per second (INTØ/). These interrupts have the highest priority. The CRT Terminal input data is the second highest priority interrupt rate source. Timer #Ø generates the programmable interrupt rate with the lowest priority.

For complete configuration of the iSBC 8Ø24A refer to the McIDAS DESIGN NOTE INTEL 8Ø24A Configuration. The design note is part of your original documentation package.

4/PCAT/02

SECTION 3
12-BIT DUAL CHANNEL COLORIZER - IDT RAM VERSION
TABLE OF CONTENTS

12-BIT (DUAL CHANNEL) COLORIZER - IDT RAM VERSION
(SSEC DRAWING 35Ø4-Ø45, DATED 6/24/86)

INTRODUCTION

The 12-bit Dual Channel Colorizer performs three major functions on the compressed data from the DATARAM's two image storage units:

- data decompression
- user interaction with image data processing
- user interaction with color enhancement processing

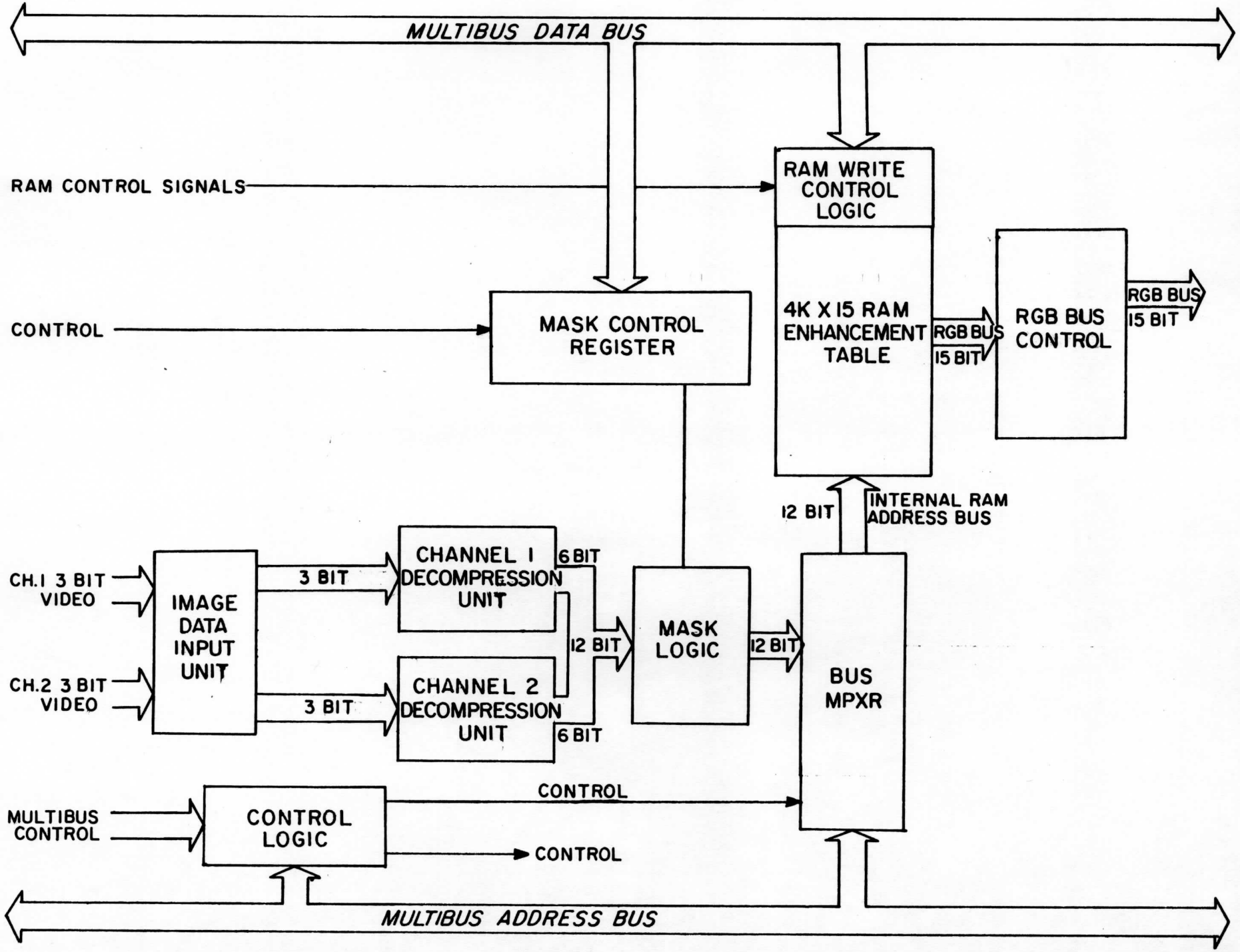
An image picture contains approximately 313,600 pixels, each of which originally is represented by a 6-bit binary code (64 brightness levels). If the 6-bit format is used, over two million bits of storage are required to store each image picture. To reduce storage requirements by half, the 6-bit real data values are compressed into 3-bit "partitions." The microprocessor executes the compression algorithm when it moves the data from the communications buffer to the DATARAM storage unit. The 3-bit partition values are stored in the workstation, reducing the memory requirement by half. Data decompression is the process of reconstituting the 6-bit digital image data from compressed 3-bit partition codes.

Pixel-by-pixel decompression is performed simultaneously on two pictures. Through user interaction, either or both picture(s) can be selected, masked according to video intensity, combined, or processed by combinations of the above actions.

The last major function of the Dual Channel Colorizer is color enhancement of the dual channel video data. The user can define a "gray scale level" to "color hue and brightness" relationship for each video channel individually or for two combined video channels. This function allows a greater volume of image data with more rapid analysis than is possible with a monochrome image.

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the Dual Channel Colorizer.



12 BIT DUAL CHANNEL COLORIZER FUNCTIONAL BLOCK DIAGRAM
FIGURE-1

The inputs to the Image Data Input Unit are the compressed 3-bit per channel (six bits total) image data from the two DATARAM image storage units. The Image Data Input Unit converts the dual channel input data to TTL logic levels.

Two identical state machines are used to decompress the two 3-bit channels into two 6-bit channels. The only input to the state machines, other than the 3-bit input data, is feedback of the previous 6-bit output data (the previous pixel brightness level).

The 6-bit decompressed data are passed to the Mask Logic block, which can turn off any of the decompressed input data lines via the Mask Control Register block. The output from the Mask Logic block is applied to the Bus Multiplexer block.

The Mask Control Register receives data from the Multibus and latching signals from the Control Logic Unit. The Mask Control Register can store (latch) up to 12 mask control bits used by the Mask Logic Unit. Currently, the Mask Control Register is used as a channel selector, enabling or disabling all data bits of each channel.

The 12-bit output from the Mask Logic Block is applied to one set of inputs of a Bus Multiplexer. The other set of Bus Multiplexer inputs are driven by the Multibus address bus. The Multiplexer output is an address bus for the RAM Enhancement Table. When driven by the Multibus, the multiplexed address bus selects a RAM Enhancement Table cell to be written into. The data to be written into the table cell come from the Multibus data bus. When driven by the Mask Logic Block, the multiplexed address bus selects a cell in the Enhancement Table from which data are read.

The Enhancement Table is a 4K by 15 static RAM and functions as a programmable look-up table. The output of the table is the origin of the RGB (Red, Green, and Blue) bus. The Mask Logic Block output (12-bit, dual-channel, decompressed video) represents video intensity and is applied as an address to the Enhancement Table via the Multiplexer. Note that in single channel operation, six bits are masked off. The 4Ø96 possible combinations of video intensities can address 4Ø96 different 15-bit locations. In each location, five bits are used for each of the three color drives. When the user preprograms the intensities of these colors, each video intensity input corresponds to a particular RGB output.

The RGB Bus Control is a tri-state latch. The latch is controlled by a signal from the TV Timing and Colorizer Board (SSEC 35Ø4-Ø43 sheet 2 of 4). The RGB Bus Control allows the TV Timing and Colorizer board to turn off the RGB bus during the painting of graphics or cursor pixels, thereby assigning the Dual Channel Colorizer image data the lowest priority of the three video data types (image, graphics, and cursor).

The Control Logic block contains line drivers and receivers, memory and I/O mapping, and associated logic circuits that generate the control and gating signals for most of the board.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the 12-bit Dual Channel Colorizer is shown on SSEC drawing #35Ø4-Ø45 dated 6/24/86). The schematic circuit analysis is accomplished by analyzing groups of components, represented by a single block in Figure 1 above.

SCHEMATIC CONVENTIONS

When reference is made to the schematic circuit symbol of a multiple device, the symbol ID number is used, followed by a hyphen and the section letter designator. The symbol ID number alone is used to refer to single section ICs.

CONTROL LOGIC

The Control Logic is found on sheet 1 of the schematic diagrams. The primary objective of this Control Logic analysis is to determine which outputs are memory-mapped, which are I/O-mapped, and which addresses activate each signal.

All control signals are derived from two Multibus control signals and the Multibus address bus. The following are Multibus control signals:

- MWTC/ (Memory Write Command, inverted)
- IOWC/ (I/O Write Command, inverted)

The upper eight bits of the address bus are buffered and inverted by octal tri-state buffer J33 (74LS540) and applied to mapping PROM G2Ø (28S42). A list of the six outputs from G2Ø, their addresses, and their primary uses follows:

Signal	System Addresses	Prom Address	Prom Output	Primary Use
MW1/	CØØ1H-DFFFH(odd)	1CØ-1DFH	FEH	Enhancement Table Odd (Write)
MW2/	CØØØH-DFFEH(even)	ØCØ-ØDFH	FDH	Enhancement Table Even (Write)
IBØ/	port BØH	ØBØH	FBH	Mask and Control Register Load (Write)
IB1/	port B1H	1B1H	F7H	Mask and Control Register Load (Write)
IB2/	port B2H	ØB2H	EFH	*
IB3/	port B3H	1B3H	DFH	*

* signals exist for firmware support/backward compatibility only.

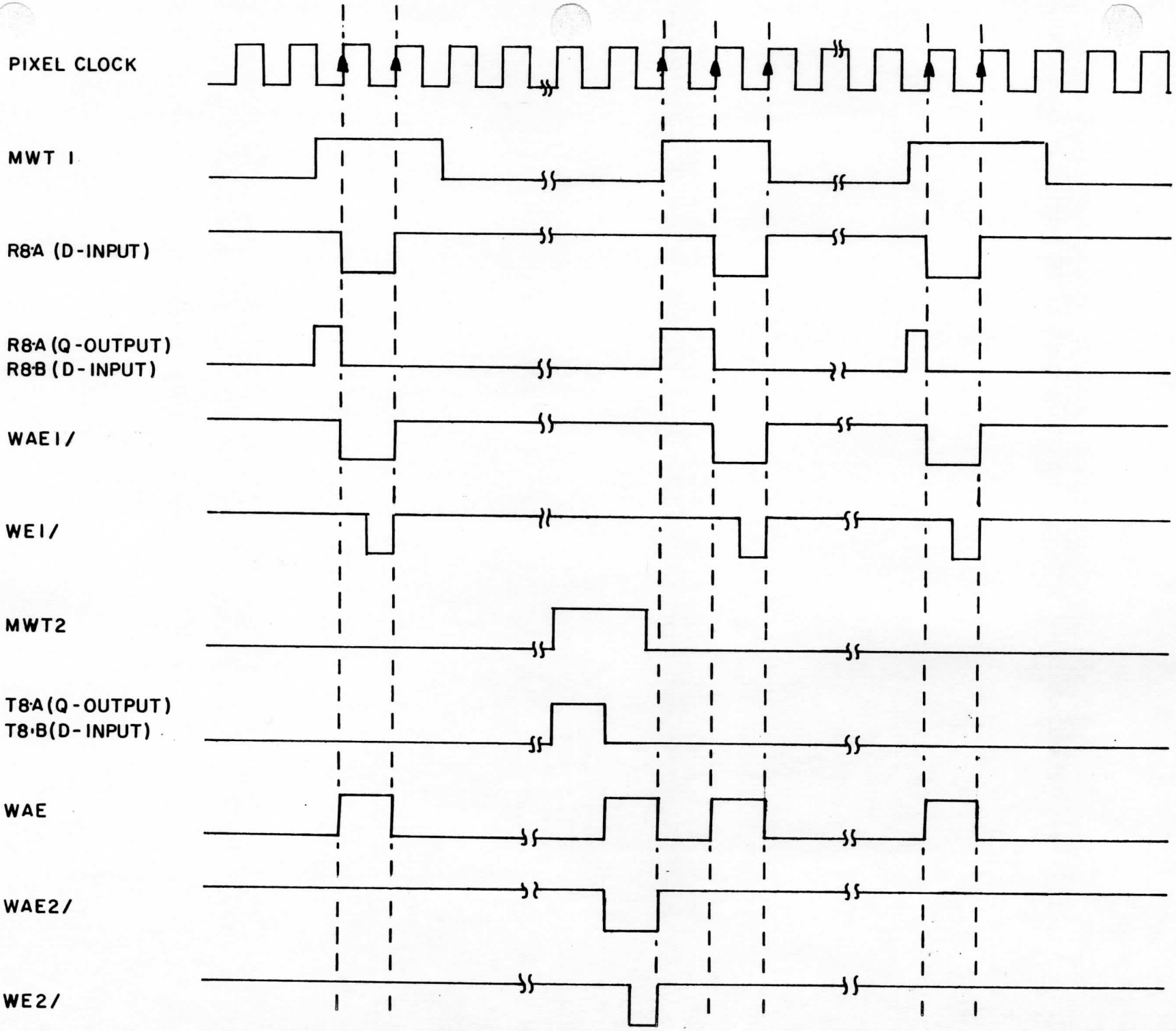
The Memory Write Control (MWTC/) and I/O Write Control (IOWC/) signals are buffered by octal tri-state buffer G33 (74LS244); they are used along with the six signals from the control mapping PROM to develop the other control signals used throughout the board.

The buffered Memory Write Control command MWT/ (active low) is applied along with the MW1/ signal from PROM G2Ø to OR gate J1Ø-A where they develop the signal MWT1/. This signal is inverted by NAND gate inverter L1Ø-A (74SØØ) and applied to the clocking input of D-latch R8-A. Likewise, the MWT/ signal is applied with mapping PROM signal MW2/ to OR gate J1Ø-B. The output is inverted by L1Ø-B and applied to the clocking input of D-latch T8-A (74S74).

Signals MWT1 and MWT2 control the memory write state of the RAM Enhancement table. MWT1 is active for all odd memory write addresses from CØØ1H-DFFFH while MWT2 is active for all even memory write addresses from CØØØH-DFFEH.

Dual D-latches R8-A and B make up a circuit used to synchronize the memory write enable signal MWT1 with the system timing signal PXLCK. Similarly dual D-latches T8-A and B make up a synchronizer for signal MWT2.

Refer to Timing Diagram 1. Signal MWT1 is applied to the clocking input of R8-A. The operation of the synchronizer is best described in terms of the PXLCK signal and its effect on the Dual D-latches' outputs. In a quiescent condition (MWT1 inactive low for several PXLCK pulses),



TIMING DIAGRAM-1 (3504-045)

R8-A and R8-B are both reset. The reset state of R8-B places an inactive high at the CLR input to R8-A and places a high level at its D-input. R8-A's output can only go high if it is clocked by MWT1. R8-B's Q-output can only go high if its D-input goes high prior to a rising edge of PXLCK at its clock input (pin 11).

When the memory write enable MWT1 goes active (from low to a high state), it clocks the first D-latch R8-A. The Q output of R8-A changes state and outputs a high level to the D-input of R8-B. On the next rising edge of PXLCK, the high level present at R8-B's D-input is latched into R8-B. A high on the D-input to R8-B causes the Q/ output to change to a low level, applying a low to the D and CLR inputs of R8-A. The low level at R8-A's CLR input causes it to immediately clear. The clearing action of R8-A causes its Q-output to go to a low logic level, which on the next PXLCK is clocked through R8-B to end the cycle.

In effect, the first D-latch, R8-A, is used to set up the operation of the second D-latch, R8-B. WAE1, the Q/ output of the second D-latch is an active low pulse, one PXLCK cycle long, synchronized with the PXLCK signal. To generate a half PXLCK wide write signal (WE1/), R8-B's output is gated through OR gate G1Ø-A by PXLCK before it is applied to the write enable input of the Enhancement RAM.

The MWT2 signal is applied to Dual D-latches T8-A and -B in exactly the same manner as was previously described for the MWT1 signal. D-latches T8-A and -B synchronize the PXLCK signal to the MWT2 signal. WAE2/ (active low) is the synchronized output from T8-B and is applied to OR gate G1Ø-B to generate the write signal WE2/.

The reader should note that what has been accomplished here is the generation of very short (approx. 40 nsec) write pulses for the RAM enhancement table. This minimizes interference with the image display while the enhancement table is being loaded.

The outputs from the clocked OR gates (74S32), WE1/ and WE2/, are the active low memory write enable signals used by the RAM Enhancement Table. Because the Multibus can supply only eight data bits to the RAM at a time, and the table is organized as a 4K by 15-bit RAM, each memory location must be programmed in two write operations. WE1/ (enhancement table odd addresses) loads the Red magnitude and two MSBs of the Green magnitude; while WE2/ (enhancement table even addresses) loads the three LSBs of the Green and all of the Blue magnitude.

WAE1/ and WAE2/ are applied to NAND gate L1Ø-C to develop the WAE signal, used to control the Enhancement Table Address Multiplexer. The WAE signal is applied to the output control pin of octal D-latches X2Ø and Z2Ø. The signal is also applied to a NAND gate L1Ø-D (74SØØ) where it is inverted and applied to the gating inputs of Tri-state buffers L2Ø and J2Ø.

The WAE signal performs two functions: in one state it enables the Mask Logic Block to drive the Address Bus Multiplexer, and in the other state it enables the Multibus to drive the Address Bus Multiplexer. When WAE is high (WAE/ is low), the bus is driven by the Multibus via buffers L2Ø and J2Ø. When WAE is low the latches X2Ø and Z2Ø are enabled and the bus is driven by the Mask Logic Block. The signal WAE/ is active low only during memory writes to addresses CØØØ-DFFFH.

The control PROM's outputs, IBØ/ through IB3/, are used to develop four control signals, MAL/, MAH/, MBL/, and MBH/. Each of the signals IBØ/-IB3/ is ORed with the IOWC/ signal to develop the MAL/-MBH/ signals. The MAx/ signals (high and low block) are applied to the Mask Control Register (R33 and T33, 74LS374) where they are used to clock the masked data bus output to the Mask Logic units. MAL/ clocks R33 (the eight LSBs) while MAH/ clocks T33 (the four MSBs).

The MAL/ and MAH/ signals, along with the MBL/ and MBH/ signals, are applied to 4-input AND gate (74LS21) N8-B, where they combine to form the MACK/ signal. MACK/ is active low when any I/O write-related signal is active (when an I/O write operation to ports BØ-B3H has been initiated). MACK/ is applied to 3-input AND gate (74LS21) N8-A along with the MWT1/ and MWT2/ signals. The output of N8-A is the XXACK/ signal (active low) and is active when any input is low. This means that either a memory write or an I/O write operation enables the XXACK/ output. This output is used as an enable for the A-half of line driver G-33 (74S244). When an I/O write or a memory write operation command is sent and the correct address has been decoded by the mapping PROM G2Ø, the XXACK/ output of N8-A goes low, enabling the A-half of G33. Only one line driver in the A-half of G33 is used. This driver has its input grounded and drives the XACK/ line. Thus, when enabled, this device passes an active low XACK/ signal to the CPU on the single-board computer, signaling the acknowledgement of the command.

IMAGE DATA INPUT UNIT

Refer to sheet 2. Image data enters the board from the two image data storage units via the P2 bus. Channel 1 supplies three bits to quad line receiver AF22 (26LS33) while channel 2 supplies its three bits to quad line receiver AH22 (26LS33). The line receivers convert the differential input signals to TTL levels.

DECOMPRESSION UNIT

The Decompression Units are shown on sheet 2 of the schematics. The two identical decompression state machines share a data input D-latch (AF33) (74S374); each contains a PROM and a feedback D-latch. Channel 1 consists of PROM AD2Ø (28S42) and latch AB2Ø (74S374). The channel 2 counterparts are AD33 and AB33. These state machines outputs form all but the three least significant address inputs for the next data input. The three address LSBs are driven by the compressed data partitions stored in the DATARAM. The PROM in each state machine functions as a 6-bit by 512 RAM look-up table. Note that D-latches AB2Ø and AB33 are clocked by PXLCK, thus the present PROM outputs become address inputs for the next PXLCK.

The state machine must always start in a known state. The input data stream consists of horizontal scan lines of video, thus the state machine must always be reset to state Ø before starting a new horizontal line. Currently, the state machines are reset to "zero" simply by supplying several pixel partitions of "zero" to each state machine at the end of each horizontal scan line. All image data other than the 64Ø visible pixels per horizontal line are automatically set to zero by the DATARAM control boards and 8Ø85 firmware. The states within the state machine are designed so that a maximum of five consecutive "zero" value partitions always cause a return to state "zero." In the present configuration, image data output latches AB2Ø and AB33 are enabled continuously.

The output from each state machine is decompressed image data, a 6-bit number. It designates the current state of the state machine. This current state (fed back as the six MSB address inputs after the next PXLCK), together with the next partition (the three LSB address inputs), forms the new address to the PROM and advances the machine into a new state. Table 1 is the composite PROM state table which, for discussion, has been converted from hexidecimal to decimal. As an example, assume

Gray Value	Partition 0	1	2	3	4	5	6	7
0	0	1	4	15	27	39	51	63
1	0	1	2	5	10	33	56	61
2	1	1	3	6	11	34	57	62
3	2	3	4	7	12	35	58	63
4	0	3	4	5	8	13	36	59
5	1	4	5	6	9	14	37	60
6	2	5	6	7	10	15	38	61
7	3	6	7	8	11	16	39	62
8	4	7	8	9	12	17	40	63
9	0	5	8	9	10	13	18	41
10	1	6	9	10	11	14	19	42
11	2	7	10	11	12	15	20	43
12	3	8	11	12	13	16	21	44
13	4	9	12	13	14	17	22	45
14	5	10	13	14	15	18	23	46
15	6	11	14	15	16	19	24	47
16	7	12	15	16	17	20	25	48
17	8	13	16	17	18	21	26	49
18	9	14	17	18	19	22	27	50
19	10	15	18	19	20	23	28	51
20	11	16	19	20	21	24	29	52
21	12	17	20	21	22	25	30	53
22	13	18	21	22	23	26	31	54
23	14	19	22	23	24	27	32	55
24	15	20	23	24	25	28	33	56
25	16	21	24	25	26	29	34	57
26	17	22	25	26	27	30	35	58
27	18	23	26	27	28	31	36	59
28	19	24	27	28	29	32	37	60
29	20	25	28	29	30	33	38	61
30	21	26	29	30	31	34	39	62
31	22	27	30	31	32	35	40	63
32	0	23	28	31	32	33	36	41
33	1	24	29	32	33	34	37	42
34	2	25	30	33	34	35	38	43
35	3	26	31	34	35	36	39	44
36	4	27	32	35	36	37	40	45
37	5	28	33	36	37	38	41	46
38	6	29	34	37	38	39	42	47
39	7	30	35	38	39	40	43	48
40	8	31	36	39	40	41	44	49
41	9	32	37	40	41	42	45	50
42	10	33	38	41	42	43	46	51
43	11	34	39	42	43	44	47	52
44	12	35	40	43	44	45	48	53
45	13	36	41	44	45	46	49	54
46	14	37	42	45	46	47	50	55
47	15	38	43	46	47	48	51	56
48	16	39	44	47	48	49	52	57
49	17	40	45	48	49	50	53	58
50	18	41	46	49	50	51	54	59
51	19	42	47	50	51	52	55	60
52	20	43	48	51	52	53	56	61
53	21	44	49	52	53	54	57	62
54	22	45	50	53	54	55	58	63
55	0	23	46	51	54	55	56	59
56	1	24	47	52	55	56	57	60
57	2	25	48	53	56	57	58	61
58	3	26	49	54	57	58	59	62
59	4	27	50	55	58	59	60	63
60	0	5	28	51	56	59	60	61
61	1	6	29	52	57	60	61	62
62	2	7	30	53	58	61	62	63
63	0	12	24	36	48	59	62	63

Table 1. Composite PROM table with traces showing the compression and decompression of the real data values 34, 42, 28, 30 and 31.

that the state machine currently has an output of 17 and the next two incoming partitions are six and five. By reading down the "Gray Value" row to 17 (current output) and then across to the partition 6 column, the result is an output of 26. The 26 is not only an output, it also selects the next "Gray Value" row, 26. When the next partition comes in (five), read down the partition 5 column to row 26 to find the next output, 3Ø. Thus, with an initial output of 17 and partitions of six and five as inputs, the next two outputs are 26 and 3Ø.

With this much information about the decompression process, we can actually infer the compression algorithm without reading any of the code. Compression is a process of determining which partition yields the closest value on a given "Gray Value" line (refer to Table 1). When a value is determined by the algorithm, that value determines the "Gray Value" line for the next data input compression cycle. The partition number is stored in the DATARAM. The following is an example of the compression process. As stated earlier, the state machine always starts at zero at the beginning of each horizontal scan. Therefore, for our example, assume that we are starting at zero, and the following set of image data is applied to the compression algorithm: 34, 42, 29, 31 and 32. Refer to Table 1 during this example analysis. Start at "zero" ("Gray Value" line Ø). The first uncompressed data input is 34; 39 is selected because it is the closest value in line Ø to the original input value of 34. A partition value of 5 is stored and a new "Gray Value" of 39 is determined. Now, at "Gray Value" line 39, the next input value is 42. A partition value of 6 yields a 43, the closest value to 42, which leads to "Gray Value" line 43 for the next input and stores a partition value of 6. Next, an input of 29 results in a partition value of 1 and a new "Gray Value" line of 34. Now, an input of 31 results in a partition of 2 and a "Gray Value" line of 3Ø. Finally, an input value of 32 at "Gray Value" line 3Ø stores a partition value of 4 and yields "Gray Value" line 31.

In summary, the input values of 34, 42, 29, 31, and 32 result in partition values of 5, 6, 1, 2, and 4. When these partition values are decompressed, the data outputs are 39, 43, 34, 3Ø, and 31. Table 2, below, shows the inputs, partitions, outputs and error magnitudes.

Table 2

Partition	Image Input	Image Output	Error
5	34	39	5
6	42	43	1
1	29	34	5
2	31	3Ø	1
4	32	31	1

The error, while usually small and generally insignificant (especially when input data changes are small), is the consequence of reducing the memory storage requirements by 50%.

MASK LOGIC UNIT

Twelve dual-input AND gates constitute the Mask Logic Unit. The circuitry consists of quad AND gates V33, X33, and Z33. Each of the data bits from the output of the dual decompressors (12 bits total) is applied to a separate AND gate in the Mask Logic Unit. The other input to each gate is a control bit (12 total) from the Mask Control Register. If a particular control bit is a "one", the corresponding AND gate passes its data from the decompressor to the Bus Multiplexer. Thus, the Mask Logic Unit is simply a 12-section, single-pole-single-throw electronic switch. Currently, this unit is used as a channel selector. The following are four possible states of operation:

- channel one and channel two disabled
- channel one enabled, channel two disabled
- channel one disabled, channel two enabled
- channel one and channel two enabled

The output of the Mask Logic Unit is passed on to X2Ø and Z2Ø (74S374) (tri-state latches), part of the Bus Multiplexer.

MASK CONTROL REGISTER

The Mask Control Register consists of tri-state octal D-latches R33 and T33. Each of the tri-state octal latches is connected to the buffered

Multibus data bus (DATØ-DAT7). The outputs from R33 are used as mask control bits for the least significant eight bits of the Mask Logic Unit. R33 is clocked by MAL/ from the Control Logic Unit. MAL/ is an I/O-mapped control signal, addressed by the CPU as port BØH. Thus, when addressing port BØH, the data (mask data) present on the Multibus data bus is latched into R33. In a similar manner, T33 latches the four MSB mask control bits and is addressed as port B1H.

Only two of the four MSB outputs from T33 are used.

BUS MULTIPLEXER

The Bus Multiplexer is shown on sheet 1 of the schematics and consists of octal tri-state D-latches X2Ø and Z2Ø (74LS374) and non-inverting tri-state buffers L2Ø and J2Ø. The D-latch outputs are enabled by a low WAE while the buffer outputs are enabled by a low WAE/ (refer to the Control Logic Section for information on the generation of WAE). As stated earlier, WAE/ is active low during memory writes to addresses CØØØH-DFFFH. Therefore, during these times, L2Ø and J2Ø are enabled, allowing the Multibus address bus to address the RAM Enhancement Table.

RAM Enhancement Table

The RAM Enhancement Table is shown on sheet 2 of the schematic diagrams. The RAM consists of four 4K by 4-bit static RAM chips organized as a 4K by 16-bit static RAM (IDT 71681SA25C). Of the 16 output bits, only 15 are used. These RAMS feature separate data input and output pins, allowing the input pins to be connected directly to the buffered Multibus data lines (DATØ-DAT7). To write data into the table, WE1/ or WE2/ is brought low by performing a memory write to addresses CØØØH-DFFFH.

Because the RAM address bus lines (RAØ-RA11) are driven by buffered Multibus address lines ADR1-ADRC respectively, the CPU makes two consecutive memory writes to program one address in the table (ADRØ effectively toggles the write enables while ADR1-ADRC select the address). The output of the RAM chips forms the RGB bus and is applied to the RGB Bus Controller.

RGB Bus Controller

The bus controller consists of X5 and V5 (74S374), located on sheet 2 of the schematics diagrams. These tri-state latches are clocked by PXLCK and enabled by a control signal from the TV Timing and Colorizer board via J2 pin 4. Thus, the RGB data generated by the Dual Channel Colorizer can be disabled (during a cursor and/or graphics pixel) by the TV Timing and Colorizer.

4/PCAT/03

4. 60/50HZ TV TIMING AND COLORIZER

SECTION 4
50/60 HZ TV TIMING AND COLORIZER BOARD
TABLE OF CONTENTS

50-6Ø HZ TV TIMING AND COLORIZER BOARD - BROOKTREE
(SSEC DRAWING 35Ø4-Ø43, MODIFICATION C, DATED 2/09/87)

INTRODUCTION

The TV Timing and Colorizer board includes two units, the TV Timing Unit and the Graphics/Cursor Colorizer Unit. Although some timing signals from the TV Timing Unit are used by the Colorizer Unit, the units are distinct.

The TV Timing Unit generates all the synchronizing, timing, and control signals required to display the picture on the monitor. In addition, it produces many of the memory management signals required by the DATARAM Control board.

The Graphics/Cursor Colorizer Unit assigns priority ratings to the image, graphics, and cursor data, then generates graphics and cursor color signals, pixel by pixel, under control of the microprocessor.

The functional as well as detailed description of this board's operation will be discussed with reference to the 6Ø Hz mode of operation. All signal frequencies will be given for 6Ø Hz mode with 5Ø Hz mode values following in parenthesis; ex: 6Ø Hz (5Ø Hz).

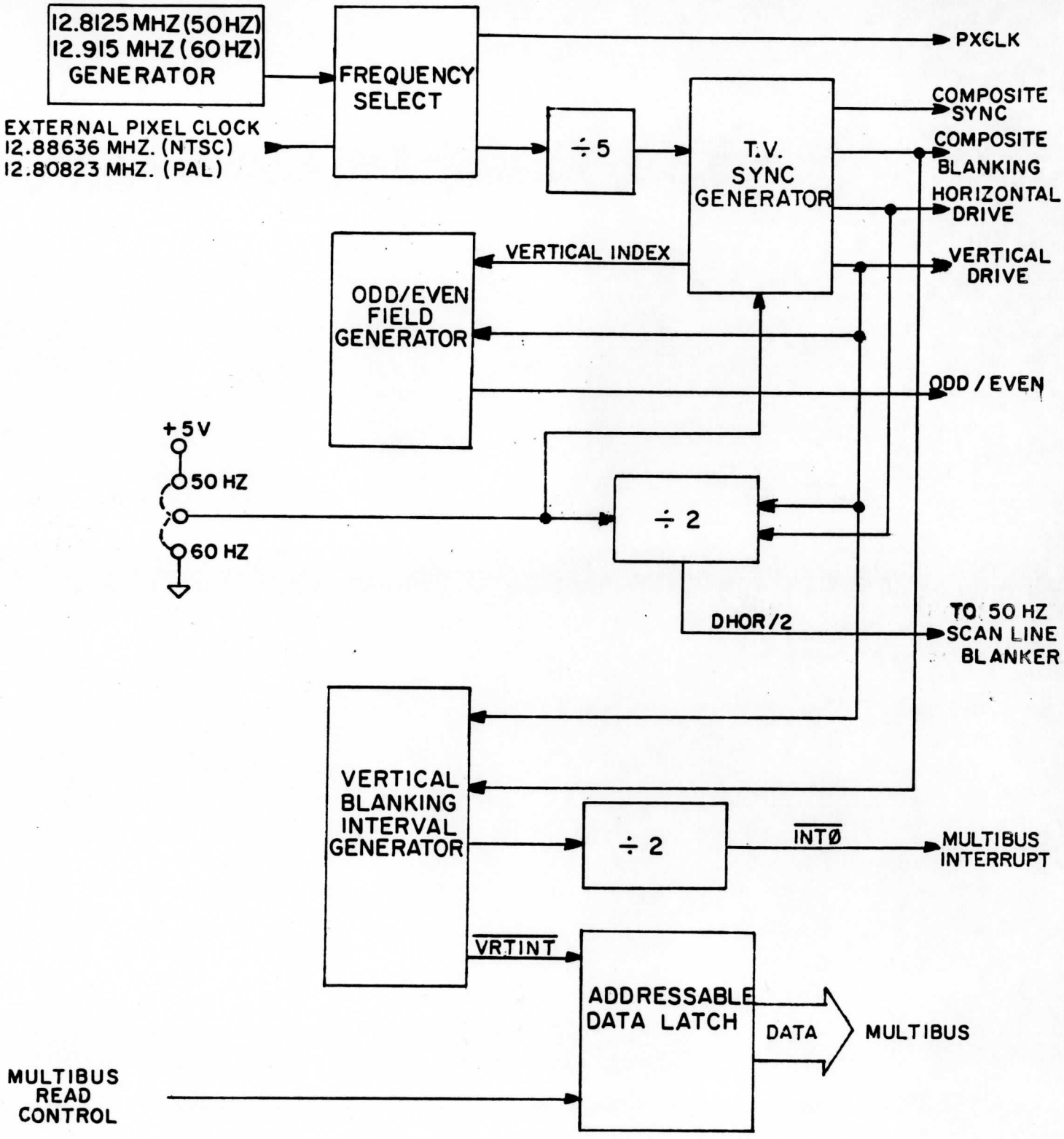
FUNCTIONAL DESCRIPTION

TV TIMING UNIT

Figure 1 is a functional block diagram of the TV Timing Unit. The unit produces the following six output waveforms:

- PXLCK (picture element clock ≅ 12.915 Mhz)
- VRDRV (vertical drive - 6Ø hz)
- HORDRV (horizontal drive - 15.75 Khz)
- BLNK (composite blanking)
- SYNC (composite synchronization)
- OE (odd/even field identification - 3Ø hz)

PXLCK, VRDRV, HORDRV, and OE are exported, via the P2 bus, to one or more of the following boards:



50/60 HZ T.V. TIMING GENERATOR FUNCTIONAL BLOCK DIAGRAM

FIGURE 1

(3504-043)

- DATARAM/Multibus Interface
- DATARAM Control
- Dual Channel Colorizer
- Cursor Generator

BLNK and SYNC are used by only the Graphics/Cursor Colorizer Unit.

All TV timing signals originate with either the on-board 12.915-Mhz (12.8125 MHZ) generator or the optional external PIXEL CLOCK generator from the PAL/NTSC TV Sync Board. The on-board generator output is applied to the Frequency Select block, essentially an electronic switch. The PAL/NTSC external PIXEL CLOCK generator in NTSC mode provides a 12.886362-Mhz reference frequency input to the Frequency Select block and provides control signals. The Frequency Select block automatically switches to the PAL/NTSC TV Sync Board generator reference if it is available.

The output of the Frequency Select block is used as PXLCK and is the source for the divide-by-five block. The divide-by-five block produces the 2.583-Mhz (2.5625-MHz) or 2.577272-Mhz (NTSC) reference input to the TV Sync Generator block, a single IC chip that produces all of the standard TV signals.

The vertical drive is interlaced. That is, the TV scans the 262½ odd lines, retraces to the top of the screen and scans the 262½ even lines in each complete picture. Therefore, there are 6Ø vertical sync pulses/sec but only 3Ø complete pictures. The DATARAM Control board must know which field is being scanned (odd or even). As an aid, the TV Sync Generator provides a short duration pulse (vertical index) at the beginning of each picture (3Ø-hz rate). The "Odd/Even Generator" uses the Vertical Index and the Vertical Drive as inputs to generate a 3Ø-hz symmetrical square waveform. The waveform is a logic "one" (high) during the odd field and a logic "zero" during the even field. A control signal DHOR/2 is generated by dividing the HORDRV frequency in half and referencing it to the VRDRV signal pulse for use by the 5Ø-hz extra line blanking circuit.

Because many McIDAS processes are based on frames of information (image and graphics data storage and retrieval, for example), the DATARAM units must know when each field starts and which field (odd or even) is being scanned. The Vertical Blanking Generator block extracts the vertical blanking signal from the composite blanking (BLNK) to produce VRTINT/ (vertical interval). VRTINT/ is available to the Multibus via the "Data

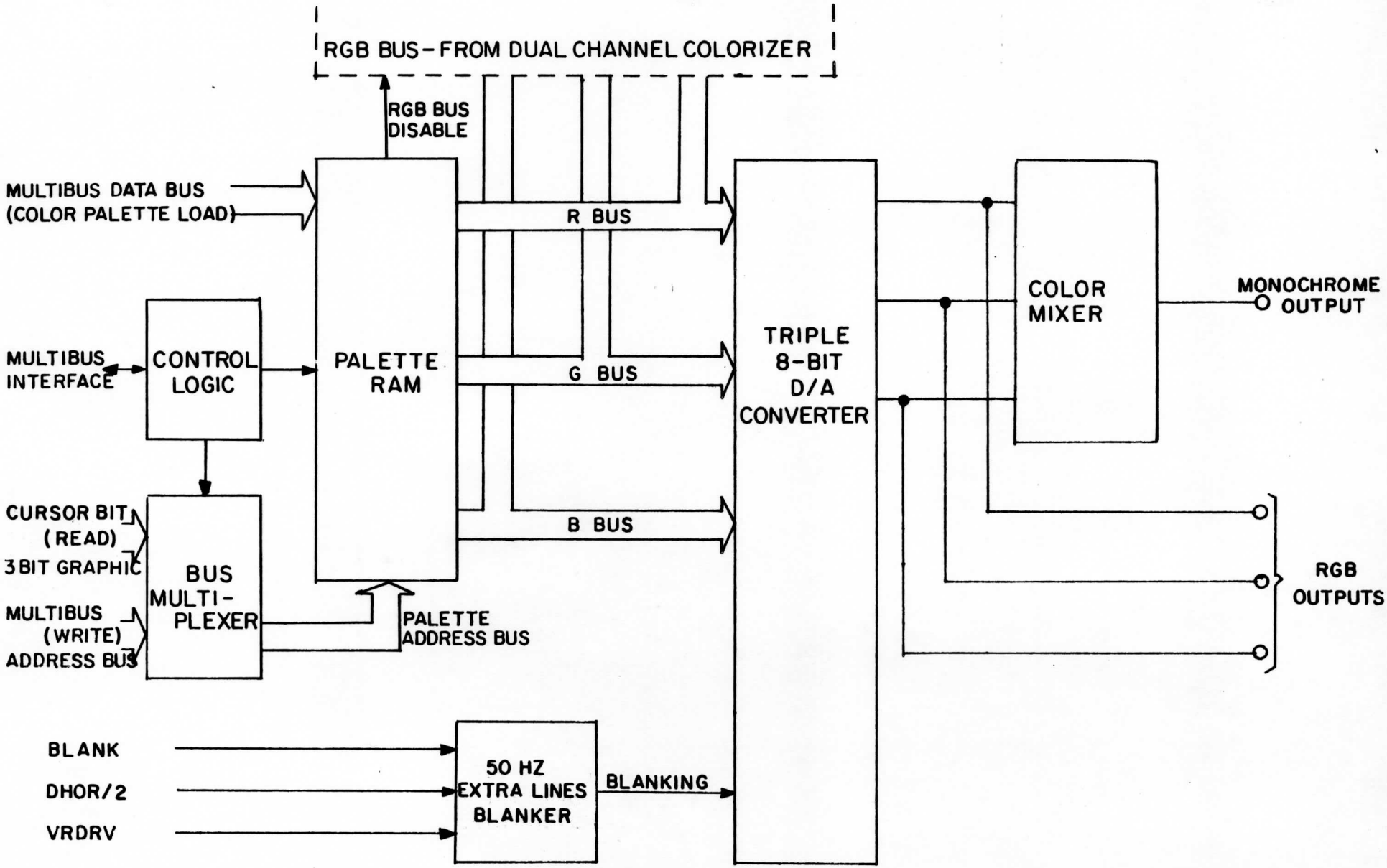
Latch" and is a logic "zero" during vertical blanking (retrace). An interrupt (INTØ/), to inform the CPU that a vertical blanking time has begun, is generated by applying VRTINT to a divide-by-two circuit. The output of the divide-by-two circuit is a symmetrical square wave. The negative-going edge of INTØ/ interrupts the CPU. The CPU uses INTØ/ and VRTINT/ to define a time window during which the cursor and graphics palettes can be loaded transparently. This window occurs only once during each complete picture, though it may occur at the beginning of either field (odd or even).

GRAPHICS/CURSOR COLORIZER UNIT

Figure 2 is a functional block diagram of the Graphics/Cursor Colorizer Unit. Image data is presented to this unit by the Dual Channel Colorizer board, via the RGB (red, green, blue) bus. The Palette RAM output connects directly to the RGB bus. Only one data source for the RGB bus is permitted at one time, either the Dual Channel Colorizer (image data) or the Palette RAM (graphic/cursor data). Because it is able to disconnect the Dual Channel Colorizer (via the RGB Bus Disable signal) during graphics/cursor pixel times, the Palette RAM has a higher priority.

Temporarily disregard the Palette RAM inputs, they are discussed in the next paragraph. The digital image data is converted to analog data by a triple digital-to-analog converter, for the each of the three primary colors. In the 5Ø-hz mode, 625 scan lines are produced. A scan line circuit is used to blank unused 118 lines of the displayed signal applied to the D-to-A converter. The outputs from the converter are fed to a color mixer and off-board, via the P2 bus, to the rear of the chassis. The P2 bus outputs are the RGB monitor video signals. The Color Mixer block sums 3Ø% of the red drive with 59% of the green drive and 11% of the blue drive to produce a monochrome output for monochrome monitors or hard copiers. These percentages are NTSC standard and represent the brightness amplitude output from a monochrome camera if it scans red, green, and blue objects of equal brightness.

The Palette RAM has 64 possible data storage addresses. The first 32 addresses (Ø-31) are the graphics color storage area (palette); addresses 32-63 are reserved for cursor color storage. More precisely, the graphics palette consists of addresses 1-7 while the cursor palette consists of



FUNCTIONAL BLOCK DIAGRAM OF THE GRAPHIC/CURSOR COLORIZER

FIGURE 2

addresses 32-39. Address Ø is selected only during image pixel painting (no graphics and no cursor); it connects the RGB bus to the Dual Channel Colorizer board and turns off the Palette RAM output. Graphics Palette addresses 8-31 and cursor palette addresses 38-63 are not used.

The user can preload up to seven graphics colors (addresses 1-7) and up to eight cursor colors (addresses 32-39) into the Palette RAM via the CPU and the Multibus. There are over 32,ØØØ possible color and brightness combinations to choose from.

Data is read from the Palette RAM under command of the Palette address bus. The bus is driven by three color selector bits and the cursor bit (from the Cursor/Joyboard and Graphics Tablet Interface board). Each palette occupies exactly half of the RAM; the palette required is determined by the state of the most significant RAM address bit. The cursor bit drives this bit and therefore selects the palette. When the cursor bit is "zero," the graphics palette is selected and when the cursor bit is "one," the cursor palette is selected. The color in each palette is selected by the same three colorselector bits.

During the Palette RAM loading process, the palette address bus is connected to the Multibus address bus by the "Bus Multiplexer." The palette data is supplied by the Multibus data bus. The palette "read," "write," and "Bus Multiplexer" controls are directed by the "Control Logic" block.

DETAILED CIRCUIT DESCRIPTION

TV TIMING UNIT

The TV Timing Unit is shown on sheet 1 of 4, SSEC drawing #35Ø4-Ø43, Modification C, dated 2/9/87 (5Ø/6Ø HZ TV Timing and Colorizer-BROOKTREE).

PIXEL CLOCK Generator

This circuit is AD3, a 25.83-Mhz (25.625 Mhz) crystal oscillator. The oscillator output is buffered by inverter Z3-A (74SØ4) and applied to the clock input of D flip-flop AB3-B (74S74). AB3-B is configured as a divide-by-two circuit by connecting the Q/ output to the D input. The output frequency of AB3-B is 12.915 Mhz (12.8125-MHZ) and is applied to AK3, the Frequency Select circuit.

Frequency Select Circuit

The Frequency Select circuit consists of data selector AK3 (74S157) and line receivers AH3-A, -B, -C, and -D (26L933). Functionally, AK3 is a triple pole, double-throw switch. The output of AH3-B determines the position of the switch. If AH3-B pin 5 is high, pin 3 of AK3 (1B) is connected to pin 4 (1Y) likewise, pin 6 (2B) and pin 1Ø (3B) are connected to pin 7 (2Y) and pin 9 (3Y) respectively. When pin 5 of AH3-B is low, the 'A' inputs are switched through the device, connecting pin 2 (1A) to pin 4 (1Y), pin 5 (2A) to pin 7 (2Y), and pin 11 (3A) to pin 9 (3Y). Line receivers AH3-A, AH3-B, and AH3-C convert the differential NTSC generator inputs (12.886362-Mhz, Vertical Sync Reset and Horizontal Sync Reset) into TTL logic levels. The "section 1" portion of AK3 selects the frequency source while the "section 2" portion of AK3 selects the Sync Reset source. Note that if the NTSC generator is not connected to the J3 bus, line receiver AH3-B has a floating input. AM26LS33 line receivers are guaranteed by the manufacturer to have a high output when their inputs are floating. Therefore, AH3-B, the control line receiver, has a high output when the NTSC generator is not connected. AH3-B connects the on-board 12.915-Mhz frequency source to AK3-4 and connects the pin 7 and pin 9 outputs to a pull-up. One of the functions, therefore, of the NTSC generator is to force pin 5 of AH3-B low, connecting its three outputs (12.886362 Mhz and both Sync Resets) to the outputs of AK3. The purpose of the Sync Reset signals is covered in detail in the TV Sync Generator description. The output of AK3 pin 4 becomes PXLCK after it is buffered by Z3-B.

Divide-by-Five Circuit

The divide-by-five circuit is 4-bit binary counter AK13 (74LS163) and AF14-A (74LSØØ). The counter is preloaded with a count of 2 by NAND gate AF14-A. AF14-A is qualified by a counter output of Ø11ØB(6), because the Q_B and Q_C counter outputs are used. It takes four counts to qualify the output of Z11-C, but the counter (74LS163) has a synchronous load feature so it does not preload until the next clock pulse input. The output frequency of the divide-by-five circuit is 2.583 Mhz (2.5625 MHz) or optionally 2.577272 Mhz. The output frequency is applied to the TV Sync Generator and to inverting buffer Z3-C.

TV Sync Generator

The TV Sync Generator is TV camera sync generator chip AM4 (Ferranti, ZNA134). This chip provides all of the basic sync functions for either color or monochrome 625-line/5Ø-Hz or 525-line/6Ø-Hz interlaced camera and video recorder applications. A jumper located at either AM1-AN1 or AM2-AN2 selects the 5Ø or 6Ø hz mode.

The chip divides the reference frequency by 164 to produce the horizontal sync frequency of 15,75Ø hz (5Ø Hz, 15,625 Hz). The vertical sync frequency is generated by dividing the horizontal frequency by 262.5 or 312.5 respectively. Therefore, the vertical drive frequency is 6Ø.ØØ hz or 50.00 Hz. All output signals from this chip are composites of these three frequencies. For further information on the TV Sync Generator, refer to a Ferranti Semiconductor reference manual. If PXLCK is divided by five to produce the reference frequency, and the reference frequency is divided by 164 to produce the horizontal frequency, the PXLCK frequency is 82Ø times the horizontal frequency. Thus, there are 82Ø pixels per horizontal line. However, approximately 172 pixels are lost due to the horizontal blanking time for retrace. This leaves approximately 648 active pixels per horizontal line (in the McIDAS, the additional pixels beyond 648 are set to zero.

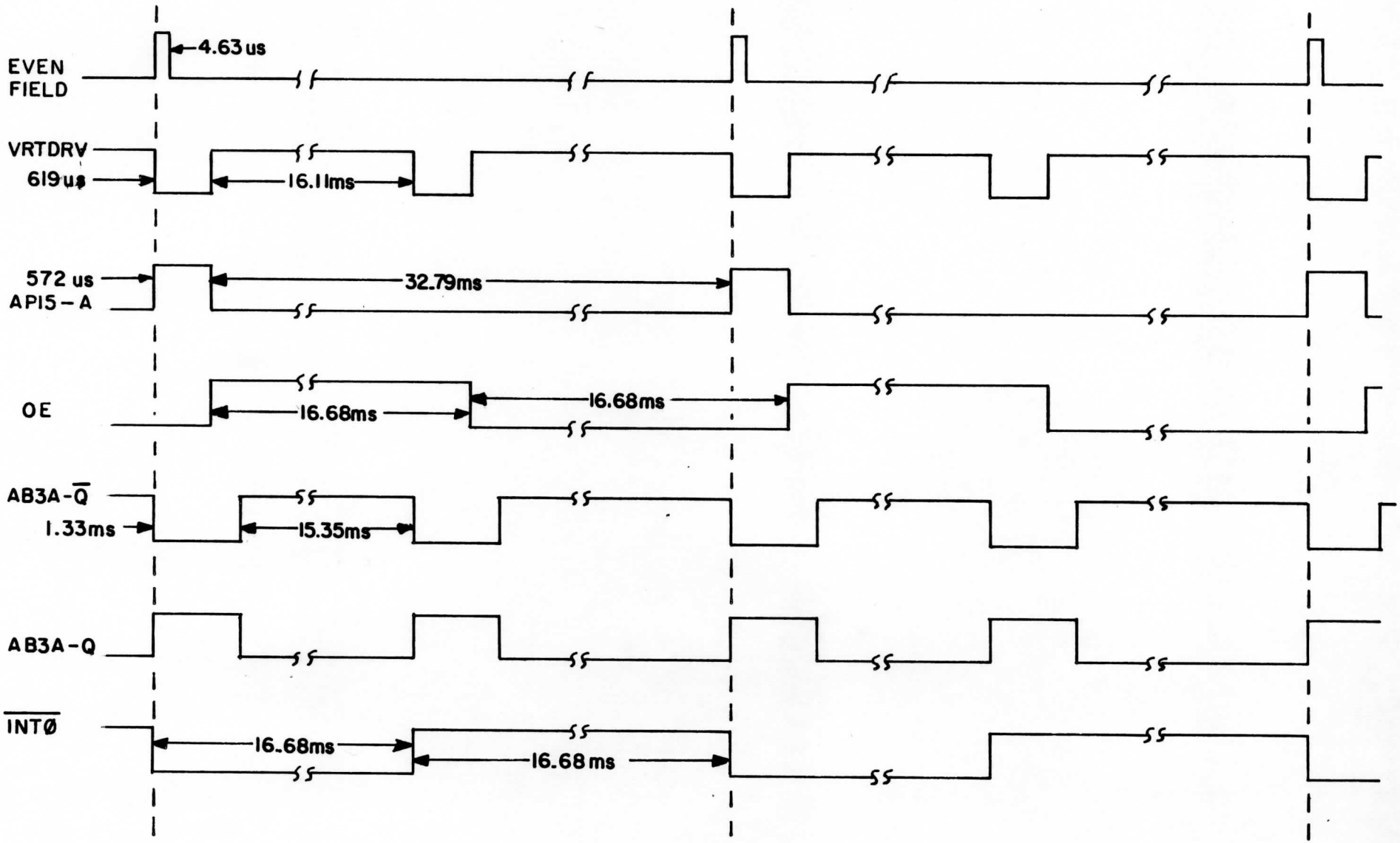
When an NTSC generator is used, it produces its own sync signals for use by an NTSC monitor and the standard RGB monitor (the NTSC generator uses the same type of sync generator chip). The NTSC generator sync signals and the AM4 sync signals must be locked together because the AM4 signals are used by the DATARAM control board for reading image and graphics data from memory. If the two sets of sync signals are not locked together, the images appear to drift or float across the screen. This is because they are produced under control of one set of sync signals and displayed under control of the other.

AM4 is designed to be synchronized by an external sync generator. This feature is used when AM4 operates with an optional NTSC (PAL) generator. The generator provides two sync reset inputs to line receivers AH3-C and -D. The horizontal sync reset signal is coupled from pin 5(2A) to pin 7(2Y) of AK3, while the vertical sync reset signal is coupled from pin 11(3A) to pin 9 (3Y). These two signals provide the horizontal and vertical reset input to AM4.

Horizontal drive (pin 5), vertical drive (pin 16), composite blanking (pin 4), and composite sync (pin 3) outputs from AM4 are resynced to PXLCK by quad-D latches AP3 (74LS175) and AM23 (74S175). AP3 resyncs the outputs to the 2.583-Mhz reference and AM23 resyncs the outputs of AP3 with PXLCK. VRDRV (AM23 pin 2), HORDRV (AM23 pin 7), and PXLCK (Z3-B pin 4) are exported from this board by line drivers AP26-B, -C and -A (26LS31) respectively. In addition, PXLCK, composite blanking, and composite sync are routed to the Graphics and Cursor Colorizer Unit (sheets 2, 3 and 4 of the schematic).

Odd/Even Field Generator

The Odd/Even Generator consists of dual D-type F/F AP15-A and -B (74LS74). The even field index output pulse from AM4 (pin 14) is a 4.63 µsec active high pulse occurring at a 3Ø-hz rate. The pulse signals the beginning of a new picture. (Remember, a picture frame consists of two fields, odd and even.) The active high pulse is applied to the clock input of AP15-A. Refer to Timing Diagram 1. The output of AP15-A follows the D input (pin 2) on the rising edge of the inverted even field clock input. The D input is always a logic "one" when the clock pulse arrives. After the clock pulse arrives, the output of AP15-A is also a logic "one." The AP15-A output is also the AP15-B input. AP15-B is clocked by VRDRV (positive-going edge). As a result, AP15-B Q output (pin 9) goes to a logic "one" on the trailing positive-going edge of VRDRV (about 572 µsec after the even field pulse). This produces a logic "zero" output from AP15-B Q/, which asynchronously clears AP15-A. Therefore, AP15-A has a 572-µsec active high output pulse every 33.3 µsec. When AP15-A returns to a logic "zero" output, it provides a "zero" input to AP15-B. Therefore, AP15-B also goes to a logic "zero" output at pin 9 but not until the next trailing edge of VRDRV arrives. When AP15-B pin 9 goes to a logic "zero", the Q1 (pin 8) returns to a logic "one". This action prepares AP15-A for the next even field clock input. The same action produces a symmetrical waveform at the Q output of AP15-B; the waveform changes state on the trailing edge of each vertical drive (VRDRV) pulse. This waveform is called OE (odd/ even). These waveforms are shown in Timing Diagram 1.



TIMING DIAGRAM - 1

TV TIMING AND COLORIZER BOARD

(3504-043 SHT. 1)

Vertical Blanking Interval Generator

The Vertical Blanking Interval Generator provides vertical blanking status to the CPU via the Multibus. To accomplish this, the circuit provides two outputs to the Multibus, an interrupt (INTØ/) and a vertical blanking interval waveform (VRTINT/). INTØ/ interrupts the computer at the beginning of the vertical blanking period, while VRTINT/ is active low for 1.3 msec during the vertical blanking period. The CPU uses these two waveforms to perform transparent operations (processes, such as graphics or cursor color palette RAM loading, that disrupt the monitor display if performed during the pixel display process).

The Vertical Blanking Interval Generator is D flip-flop AB3-A (74S74). AB3-A is preset 6Ø times/sec by the vertical drive signal (VRDRV) and is clocked by composite blanking. VRDRV presets the Q output (pin 5) to a logic "one." The first rising edge of composite blanking following the preset causes the Q output to return to the low state, because the D input (pin 2) is grounded. This results in a 6Ø-hz waveform with an active low period of 1.3 msec (VRTINT/) at pin 6 (Q/) of AB3-A.

The Q output of AB3-A (pin 5) is applied to divide-by-two counter X12 (74LS669). The Q_A output of X12 (pin 14) is a symmetrical 3Ø-hz square wave and is applied to open collector NAND Gate X21-A (74S38). The output of X12-A is INTØ/.

VRTINT/ is applied to the D1 (pin 3) input of tri-state octal latch L33 (74S374). D2 - D7 of L33 are grounded and the eight output lines are connected to the Multibus data bus. Therefore, when the CPU is interrupted by INTØ/, the CPU polls (reads) the status of VRTINT/ by enabling L33. L33 is enabled by driving pin 1 (OE/) low. Due to inverter L2Ø-F (74LS24Ø), the clock input goes high at the same time pin 1 goes low. This device latches on the rising edge of the clock. NAND gate G26-C (74LSØØ) drives pin 1 and L2Ø-F, and is qualified when IORC/ is active low (I/O read command) and signal TIMEN is active high. TIMEN is an output of memory mapping PROM J36 (on sheet 2 of the schematic). TIMEN is active high during port address 93. G26-C is qualified, as is L33, during a port read to I/O port 93.

DHOR/2

VRDRV is applied to the preset input (pin 10) of D-latch AB13-B (74LS74) while the HORDRV signal is applied to the clocking input (pin

11). AB13-B is configured as a divide-by-two circuit by connecting the Q/ output to the D input. The D-latch presets every 60th of a second and outputs an active high pulse at a frequency of 7.875 KHz, one half the Horizontal Drive rate. The Q output (pin 9) is applied to AND gate Z13-B (pin 3 and 4). A 50-Hz mode jumper tied to +5V provides a high logic level to pin 5 of AND gate Z13-B. Z13-B (74LS11) is qualified only when the jumper is placed in the 5Ø Hz mode, passing the 7.875-KHz DHOR/2 signal to the scan line blanking circuitry. This circuitry provides blanking signals to the Video D-to-A converters.

GRAPHICS/CURSOR COLORIZER UNIT

The digital portion of the Graphics/Cursor Colorizer is described first and is found on sheet 2 of 4, SSEC #35Ø4-Ø43. The digital-to-analog conversion portion (sheet 3) is covered next, followed by the composite video section (sheet 4).

Palette RAM

The Palette RAM consists of two Fairchild F93419 RAM chips (R16 and U16). Most of the circuitry on sheet 2 of the schematic is involved with board control and reading or writing data to or from the Palette RAM. As a result, the RAM is analyzed in terms of the following:

- electrical characteristics and configuration
- read/write controls
- addressing inputs
- RGB bus control
- output function

Electrical Characteristics and Configuration

Two RAM chips (R16 and U16) are organized as 64 by 9-bit static, random-access, open-collector memories. The chips feature separate data input ($D_Ø$ - D_8) and data output ($O_Ø$ - O_8) ports and a common address port ($A_Ø$ - A_5). Note that $D_Ø$ of both chips is grounded (not used) and output bit $O_Ø$ of both chips is not used. The address and data input ports are parallel connected and the data output ports drive separate RGB bus lines, thus the two RAMS function as a 64 by 16-bit RAM.

Read/Write Control

The CS/ (active low Chip Select) is grounded and functions as a read enable. Because pin 15 is grounded, the output is always enabled. Although the output of the Palette RAM is always enabled, it can give up control of the RGB bus, as explained in the RGB Bus Control section.

The WE/ (active low Write Enable) allows data bus input data to be stored in the address specified by the address port input. Each chip has its own WE/ that originates from a separate output of E26. The generation of these signals is explained in the Control Logic Description.

Addressing Inputs

The address ports ($A_{\emptyset}$ - A_5) are connected in parallel and receive inputs from tri-state buffer N2Ø during read operations and from the Multibus address bus, via tri-state bus driver N33, during write operations. In this way, the Palette RAM address bus is multiplexed.

RGB Bus Control

Data output ports O_2 - O_6 of R16 are connected to R_4 - $R_{\emptyset}$ of the Red bus respectively, O_7 - O_8 of R16 and O_1 - O_3 of U16 are connected to G_4 - $G_{\emptyset}$ of the Green bus respectively, and O_4 - O_8 of U16 are connected to B_4 - $B_{\emptyset}$ of the Blue bus respectively.

The resistor network, X3, is the collector load resistors for the RAM open collector outputs. The two data sources for the RGB bus are the Palette RAM and the Dual Channel Colorizer. The Dual Channel Colorizer board provides image data to the RGB bus via two 74S374 tri-state buffers (X5 and V5 on sheet 2, SSEC #35Ø4 - Ø45). The Output Enable (OE) of these chips is driven by inverting input OR gate G26-D (on sheet 2, SSEC #35Ø4 - Ø43). When the output of G26-D (74LSØØ) is a "one," the Dual Channel Colorizer output buffers are in a high impedance condition (outputs disabled). During this time, the Palette RAM is the source of RGB data. The output of G26-D is a "one" any time at least one of its two inputs is a "zero". The two inputs to G26-D are O_1 (R16) and PALEN/. PALEN/ is a "one" during normal operation and is explained in detail in the Control Logic section. The output of G26-D is the inverted output of O_1 (R16) during normal operation. When O_1 (R16) is a "zero," the Palette RAM is the RGB data source and when O_1 (R16) is a "one," the Dual Channel Colorizer is the RGB data source.

As stated in the Read/Write Control section, the RAM output is always enabled. The Palette RAM must output all "one"s to give up control of the RGB bus during non-cursor and non-graphic pixels. This action, causing the output transistors in the Palette RAM to turn off, normally allows all bus lines to go to a logic high. If the Dual Channel Colorizer (DCC) is enabled by G26-D, its output buffers override the logic "one"s (on RGB lines that the DCC is attempting to pull down to a logic "zero") during the painting of an image pixel. Address ØØH in the Palette RAM is normally loaded with FFH (all binary "one"s) and is dedicated to image pixel processing.

Output Function

The RGB bus consists of five lines for each of the three colors. The binary value on each set of lines ranges from ØØØØØB (off) to 11111B (full brightness). There are 32 distinct levels for each set of five lines (each color).

Address Bus Multiplexer

The Palette RAM Address Bus Multiplexer consists of non-inverting tri-state buffer N2Ø (74S244) and inverting tri-state buffer N33 (74LS24Ø). N33 is enabled for data loading of the Palette RAM by bringing pins IG/ and 2G/ (pins 1 and 19) low. With N33 enabled, the Multibus address lines ADR1/ - ADR6/ are inverted and connected to A_0 - A_5 of the Palette RAM, selecting the address that will be loaded with the data present on the input data bus. N2Ø is enabled during Palette RAM read operations by bringing pins 1 and 19 on N2Ø low. The only four active input lines to N2Ø are D2, D5, D6, and D7.

The P2 bus is the source of the active inputs to N2Ø. The cursor bit signal (CURS) from the Cursor/Joy Board enters the board from P2-18 and P2-20. Signals VID2, VID1, and VIDØ, from the DATARAM Control board, enter the board on P2-12 and P2-1Ø, P2-8 and P2-6, and P2-4 and P2-2 respectively. All four signals (the three video signals and the cursor signal) are converted to TTL by quad line receiver AF26 (26LS33). VIDØ, VID1, and VID2 form a three-bit binary color selector address with VIDØ functioning as the LSB. The color selector bits and the cursor bit are applied to the inputs of N2Ø via AND gates J26-A, -B, -C, and -D (74SØ8).

These AND gates allow an operator to inhibit one or more of the four bits. Operation of this feature is explained in more detail in the Control Logic Section. Normally, all bits are gated through.

With N2Ø pins D1, D3, and D4 grounded, the following are the possible pallette RAM addresses and their functions:

Binary Address	Function
ØØØØØØ	Image Pixel Processing
ØØØØØ1	Graphics Color #1
ØØØØ1Ø	" " #2
ØØØ11	" " #3
ØØ1ØØ	" " #4
ØØ1Ø1	" " #5
ØØ11Ø	" " #6
ØØ111	" " #7
1ØØØØØ	Cursor Color #1
1ØØØ1	" " #2
1ØØ1Ø	" " #3
1ØØ11	" " #4
1Ø1ØØ	" " #5
1Ø1Ø1	" " #6
1Ø11Ø	" " #7
1Ø111	" " #8

Control Logic Section

The Control Logic consists of PROM J36 (HM3-7621) #49B, shift register C16, 3-to-8 line decoder E26, quad D flip-flops G16 and J16, and associated gates, buffers, inverters, line drivers, and receivers.

PROM J36 provides four mapping outputs (O_1 - O_4) that are either memory mapped or I/O mapped by external gates. IOWC/ (I/O write command) enters this board from P1-22 and is inverted by buffer E36-F. IOWC is applied to NAND gate G26-B along with the O_4 output from the PROM. This output is active high for PROM address inputs 83ØØH-837FH (I/O port address 83). Therefore, the output of G26-B is active low for I/O write commands to port address 83. The output of G26-B is applied to quad D flip-flop J16 as a clock. The D input to J16 (pin 4) is driven by DØ/ (buffered Multibus data bit Ø - DATØ). Therefore, an I/O write to port 83

with a LSB data bit equal to "zero" produces a "one" at J16-pin 4 (remember, the address bus bits are inverted) and an output from J16 (pin 3) of "zero." Conversely, a "data write" to port 83, with the data LSB equal to "one," produces a "one" output from J16 pin 3. When J16 pin 3 is a "zero," AND gate J26-D is turned off and the cursor is disabled (turned off).

The operation of NAND gate G26-A (74LSØØ), quad D flip-flop G16 (74LS175) and AND gates J26-A, -B, and -C (74SØ8) is nearly identical to the process just described in the preceding paragraph. Note, however, that DØ/, D1/, and D2/ are applied to the D inputs (1D, 2D, and 3D respectively), and the 1Q/, 2Q/, and 3Q/ outputs are applied to NAND gates J26-A, -B, and -C respectively. The PROM O_3 output is active for addresses 73ØØH-737FH and is I/O mapped by G26-A. An I/O write to port address 73, with any of the three LSBs equal to "zero," turns off the corresponding color selector bit.

PROM output O_1 is active for address inputs of FFØØH-FF7FH and is applied to AND gate E16-C (74LSØ8), along with the output of OR gate C26-A (74LS32). OR gate C26-A has inputs MRDC (Memory Read Command) and MWTC (Memory Write Command) to pins 2 and 1 respectively. The output of E16-C is active high for memory read or write to addresses FFØØH-FF7FH.

The output of E16-C is applied to both data inputs (A and B, pins 1 and 2 respectively) and the CLR input (pin 9) of C16 (74LS164). When the output of E16 is "zero," the C16 outputs are all "zero" (Q_A, Q_B, Q_C, and Q_D). When the output of E16-C is a "one," a stream of "one"s is clocked by PXLCK, through C16. That is, after the first clock pulse, Q_A is a "one," and Q_B -Q_D are "zero." After the second clock pulse, Q_A and Q_B are "one" and Q_C and Q_D are "zero," and after the third clock pulse, Q_A, Q_B, and Q_C are "one," etc. Note that the Q_A output and the inverted Q_D (inverted by inverter L2Ø-D) output are applied to AND gate E16-D. E16-D, therefore, is qualified from the rising edge of the first PXLCK until the rising edge of the fourth PXLCK, after a memory read or write to addresses FFØØH-FF7FH.

When E16-D is qualified, AND gate C36-B (74LS21) is qualified, producing GRFEN, GRFEN enables tri-state buffer N33 and disables tri-state buffer N2Ø. In this way, the Palette RAM is addressed by the Multibus address bus.

Three-to-8 line decoder E26 (74LS138) is qualified when G1 (pin 6) is "one," and G2A and G2B are "zero." The Q_B output of C16 is applied directly to G1 of E26, qualifying this input on the second PXLCK clock rising edge following a memory read or write to address FFØØ-FF7FH. If the request is a "memory write," the output of inverter L2Ø-A is a "one," not a qualifying input to E16-A. However, the Q_C output of C16 does qualify E16-A, until its output goes to a logic "one" on the rising edge of the third clock pulse after C16 is enabled. Therefore, during a "memory write," E26 is enabled from the rising edge of the second PXLCK to the rising edge of the third PXLCK, following the qualification of C16. During a "memory write," the C input (pin 3) of E26 is "zero" due to the inversion of the inactive high MRDC/ by inverter E36-D (74SØ4). The B input of E26 is "one" due to the inversion of the active low MWTC/ by inverter L2Ø-A. The A input of E26 is ADRØ and can be either "one" or "zero." When ADRØ is "zero," Y_2 of E26 is active low, enabling RAM U16 (F93419). When ADRØ is "one," Y_3 of E26 is active low, enabling RAM R16 (F93419). The table below summarizes the memory write operation to addresses FFØØH-FF7FH.

ADDRESS	RAM	REMARKS
FFØØH	U16	Image pixel processing. Inverted data must be all "one"s.
FFØ1H	R16	Image pixel processing. Inverted data must be all "one"s.
FFØ2H	U16	G2-GØ and B_4-$B_Ø$ RGB data load. Graphics Color #1
FFØ3H	R16	R_4-$R_Ø$ and G_4-G_3 RGB data load. Graphics Color #1
FFØ4H	U16	Same as address FFØ2H but Graphics Color #2
FFØ5H	R16	Same as address FFØ3H but Graphics Color #2
FFØ6H-FFØEH (even)	U16	Same as address FFØ2H but Graphics Colors 3-7
FFØ7H-FFØFH (odd)	R16	Same as address FFØ3H but Graphics Colors 3-7
FF1ØH-FF3FH		Not used.
FF4ØH	U16	G_2-$G_Ø$ and B_4-B_3 RGB Data Load. Cursor Color #1
FF41H	R16	R_4-$R_Ø$ and G_4-G_3 RGB Data Load. Cursor Color #1
FF42H-FF4EH (even)	U16	Same as FF4OH, but Cursor Colors 2-8
FF43H-FF4FH (odd)	R16	Same as FF41H, but Cursor Colors 2-8
FF5ØH-FF7FH		Not used

During a memory read to addresses FFØØH-FF7FH, GRFEN is produced just as it was during a memory write, enabling N33 and disabling N2Ø. Now, however, the G2-A and -B inputs of E26 are already qualified, because MWTC/ is a "one." E26 is enabled as soon as G1 goes high, on the second rising PXLCK following the enabling of C16. During a memory read, the C input is a "one" and the B input is a "zero." During a memory read, the outputs from E26 are Y_4 (ADRØ equal to zero) and Y_5 (ADRØ equal to "one"). Y_4 and Y_5 enable tri-state buffers V33 and T33 (74LS240's) respectively, allowing the user to examine the contents of the Palette RAM. PALEN/ is formed by ORing Y_4 (GRFRD1/) and Y_5 (GRFRD2/) via gate E16-B. PALEN/ enables tri-state buffer N33 and disables tri-state buffer N2Ø, via gate C36-B (74LS21). In summary, a memory read allows the Multibus address bus to address the Palette RAM and enables T33 or V33, allowing the specified Palette RAM contents onto the Multibus data bus for review by the user.

Gate C36-A combines the four signals (memory or I/O mapped) to enable tri-state buffer G36-A (74LS125). Thus, XACK/ (Transfer Acknowledge) goes active low, informing the CPU that the off-board memory or I/O process has been completed.

Digital-To-Analog Converter Section

The Digital-to-Analog Converter (DAC) AA23 (Brooktree BT1Ø1) is a triple 8-bit "VIDEODAC" designed specifically for high performance, high resolution color graphics. Incorporated into the VIDEODAC are three separate DACs, one for each of the three RGB bus groups. The RGB bus signals are applied directly to the DAC inputs.

Each of the 5-bit color bus group signals are applied to the most significant five bits of the 8-bit DAC inputs. The remaining three LSB's inputs are grounded. The pixel clock and composite sync signals developed on page one of the schematic diagrams are applied to AA23 pins 16 and 36 respectively.

The TV sync generator chip discussed earlier can operate in a 6Ø Hz/525 scan line or a 5Ø Hz/625 scan line mode. The display monitors used with the system are limited in the number of lines which can be displayed. Therefore, a scan line blanker circuit is incorporated into the blanking circuitry supporting the VIDEODAC.

Two 74LS161 ICs, AD12 and AD21, make up an 8-bit binary down counter. The data inputs are hardwired to a Ø11Ø111ØB or 11ØD count. The counters are loaded to the 11Ø count by the 6Ø Hz vertical drive pulse and are clocked by a one-half horizontal rate drive signal DHOR/2, a frequency of 7.875 KHz. When the last counter AD21 has reached a zero count, its ripple carry output (pin 15) is used as a clocking signal to toggle a D-type flip-flop AB13-A (74LS74). Initially, the Q/ output of AB13-A is in an inactive high state due to the 6Ø Hz vertical drive acting as a clear signal. This high level is applied to one of the inputs of AND gate Z13-A (74LS11), qualifying it. Z13-A is used to pass the composite blanking signal to the VIDEODAC. When the down counter output toggles flip-flop AB13-A, its Q/ output changes state (active low) and disqualifies AND gate Z13-A, no longer allowing the composite blanking signal to reach VIDEODAC AA23.

In effect, the VIDEODAC receives its normal composite blanking signal but is also blanked during a period required to blank the unnecessary scan lines generated by operating in the 5ØHz/625 scan line mode. The extra mode was developed for 5Ø-hz systems, which operate on 5Ø hz AC power and a 5ØHz/625 scan line mode of operation.

The VIDEODAC generates RS-343-A compatible red, green, and blue video signals and is capable of driving doubly-terminated 75-ohm coaxial cable directly, without requiring external buffering. The RGB video signals are applied to the P2 bus directly from the VIDEODAC. The composite sync signal is also applied to the P2 bus, using an LHØØØ2 current amplifier AH38 and a 68-ohm matching resistor. The sync output therefore "matches" the 75-ohm characteristic impedence required to drive a standard RGB monitor.

Color Mixer Section

The RGB video signal output voltages are also applied to the composite video circuitry (see sheet 4 of the schematic diagrams). Operational amplifier AH25 (LM318) functions as a summing amplifier. The red, green, and blue drive voltages are applied to 3.ØK-ohm, 1.5K-ohm, and 8.2K-ohm input resistors respectively. For example, if +1.ØØV (actually composed of Ø.3V and Ø.7V video signals) is simultaneously applied to the three input resistors, the red, green, and blue input currents are 333 µa,

667 µa and 122 µa respectively. Because the amplifier input current is negligible, the total input current flowing through the 1.8K-ohm feedback resistor is 1.122 µa. Therefore, the summing amplifier voltage level is -1.ØØ2V. In other words, the amplifier adds 59% of the green drive to 3Ø% of the red drive and 11% of the blue drive. The basis of these percentages was addressed in the Graphics/Cursor Colorizer Functional Description.

The output of AH25 pin 6 is a negative voltage, ranging from Ø.Ø volts (all RGB binary bits equal to "zero") to -1.4 volts (all RGB binary bits equal "one"). This voltage is applied to another summing amplifier, AH3Ø. AH3Ø (LM318) sums the RGB video (including composite blanking) with composite sync. The composite sync from the TV Timing unit is applied to inverting buffer Z3-D (74SØ4), resulting in a positive 4.Ø-volt pulse input to summing amplifier AH3Ø. The summing amplifier inverts the RGB video (Ø to 1.4V) and inverts and multiplies the sync pulse by 4.7/3Ø to produce a sync pulse with an amplitude of -Ø.63V. Thus the output of AH3Ø is a composite video having a peak-to-peak amplitude of 2.ØV. Current amplifier AM38 reduces the output impedance to 74 ohm (6-ohm amplifier output impedance and the 68-ohm resistor). Therefore, to drive a 75-ohm monochrome monitor or hard copier, the input voltages to these devices are the industry standard 1.ØV peak to peak.

4/PCAT/04

SECTION 5
CURSOR GENERATOR
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CURSOR GENERATOR

(SSEC DRAWING #35Ø4-Ø29, MOD L, DATED 11/21/86)

INTRODUCTION

The Cursor Generator is a combination of two independent units: the Cursor Generator and the Joystick Support Interface. Except for sharing minimal address decoding and an internal data bus, the two units, though they reside on the same board, are physically, functionally, and logically distinct.

The Cursor Generator is a timing circuit that tells the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board whether or not the pixel about to be scanned is a cursor bit. The 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board assigns brightness levels and color to cursor pixels. The Cursor Generator receives eight bytes of cursor parameter data from the microprocessor, via the MULTIBUS, to determine cursor size, shape, and position, and therefore which pixels are cursor pixels. TV timing signals from the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board are used by the Cursor Generator for synchronization.

The Joystick Support Interface receives, decodes, and stores the serial RS-232 joystick position data output from the Digital Joystick 2 board. This position data is available to the MULTIBUS via addressable buffers and is used to determine the position of the cursor. Typically, the right joystick provides coarse position control while the left functions as a vernier (fine) control.

FUNCTIONAL DESCRIPTION

Both units are described separately.

CURSOR GENERATOR FUNCTIONAL DESCRIPTION

The TV picture is composed of 525 horizontal lines, classified alternately as odd lines and even lines. Each horizontal line is subdivided into 78Ø picture elements (pixels). Forty-two of the horizontal lines are blanked during vertical retrace; 132 pixels are blanked during each horizontal retrace. Therefore, each picture is approximately 64Ø pixels by 483 pixels (see Figure 1). Each line is painted from left to right, one pixel at a time. First, all the even lines are painted and then, all the odd lines are painted, completing one picture. If the host computer requires that the cursor be displayed on pixel 3ØØ of line 251, then the cursor generator's output is "on" when the TV sweep paints pixel 3ØØ of line 251 and the generator's output is "off" at all other times. That is, the output is off during the painting of all even lines and the output is off when the TV sweep paints the first line, the third line, and all other odd lines until it reaches line 251. The generator's output remains off for all the pixels in line 251 until the sweep reaches pixel 3ØØ. While the sweep paints pixel 3ØØ, the generator's output goes on and the cursor is painted or displayed. For the rest of the pixels in line 251 and for the rest of the odd lines, the cursor generator's output is off. This cycle continues until the host computer changes the format of the cursor display. The cursor can be an outlined square, a solid square, a crosshair, or several other rectangular formats. The cursor generator must time its output ("cursor bit") to be on when the individual pixels that create the location and design of the cursor are painted.

Any pixel on the color monitor is referenced by its XY coordinate pair. The vertical coordinate (Y) is a specified number of scan lines from the top of the screen, while the horizontal component consists of a specified number of pixels from the left of the screen. Therefore, the following three timing signals are required to drive the cursor generator:

- vertical timing pulses to locate the top of the screen
- horizontal timing pulses for vertical position (Y)
- pixel clock pulses for horizontal position (X)

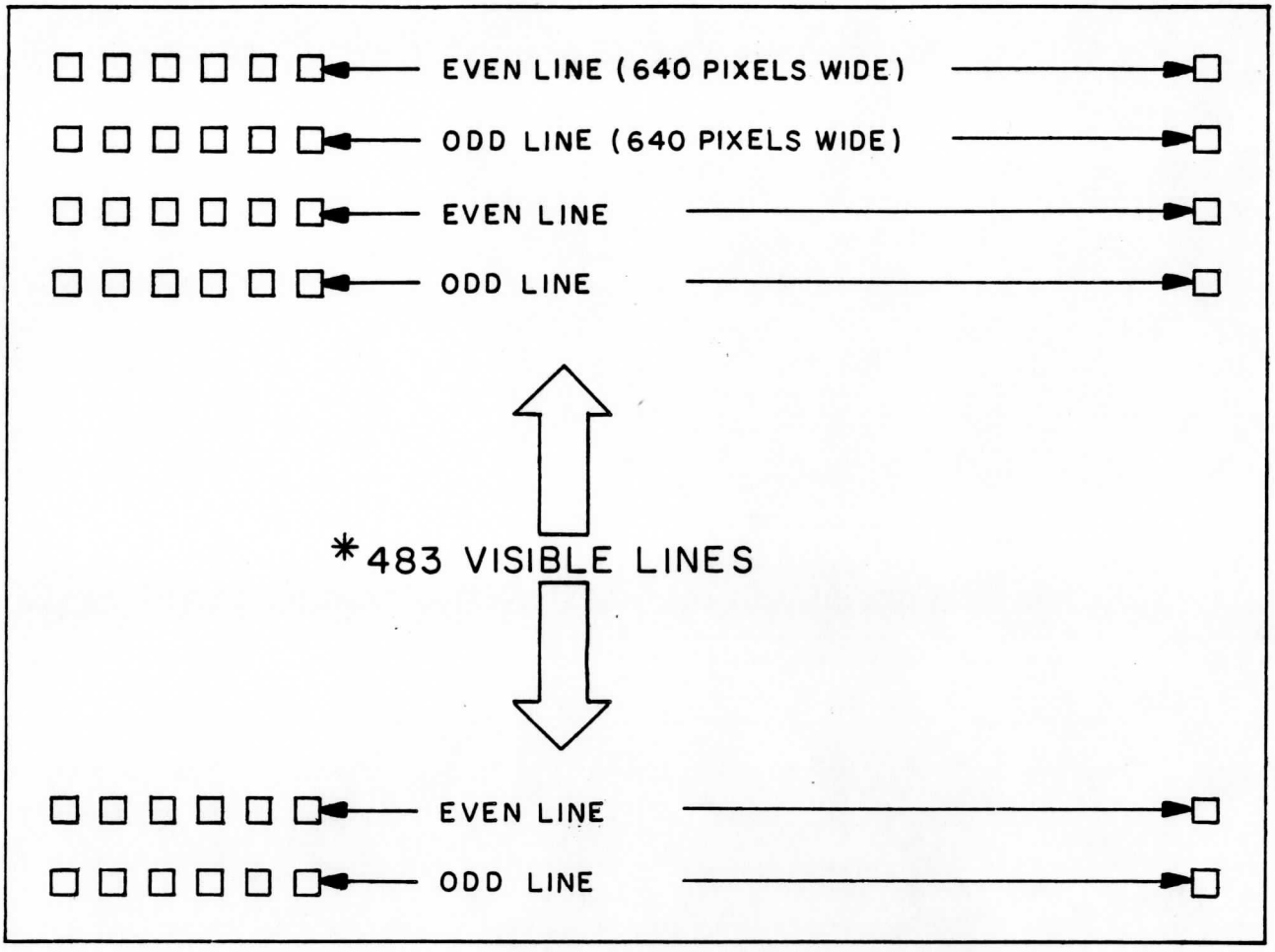


FIGURE 1 COMPOSITION OF A TV PICTURE

* Because 21 horizontal lines are blanked during each of two field retraces, SSEC workstations with Fairchild or National TV timer chips display 483 unblanked horizontal lines. The equation is as follows: 525-[2(21]=483. More recent SSEC workstations use a Ferranti TV timing chip that blanks 2Ø.5 horizontal lines during each field retrace. This results in 484 unblanked horizontal lines, defined as follows: 525-[2(2Ø.5]=484.

Refer to Figure 2, the functional block diagram of the cursor generator. The eight-byte storage register receives eight bytes of cursor parameter data from the MULTIBUS. The eight bytes are defined as follows:

- byte zero - least significant 8 bits of cursor width (pixels)
- byte one - least significant 8 bits of cursor center pixel
- byte two - lower nibble, most significant 4 bits of cursor center pixel
  - upper nibble, most significant 4 bits of cursor center line
- byte three - least significant 8 bits of cursor height (lines)
- byte four - least significant 8 bits of cursor center line
- byte five - lower nibble, most significant 4 bits of cursor width (pixels)
  - upper nibble, most significant 4 bits of cursor height (lines)
- byte six - cursor state assignments
- byte seven - cursor state assignments

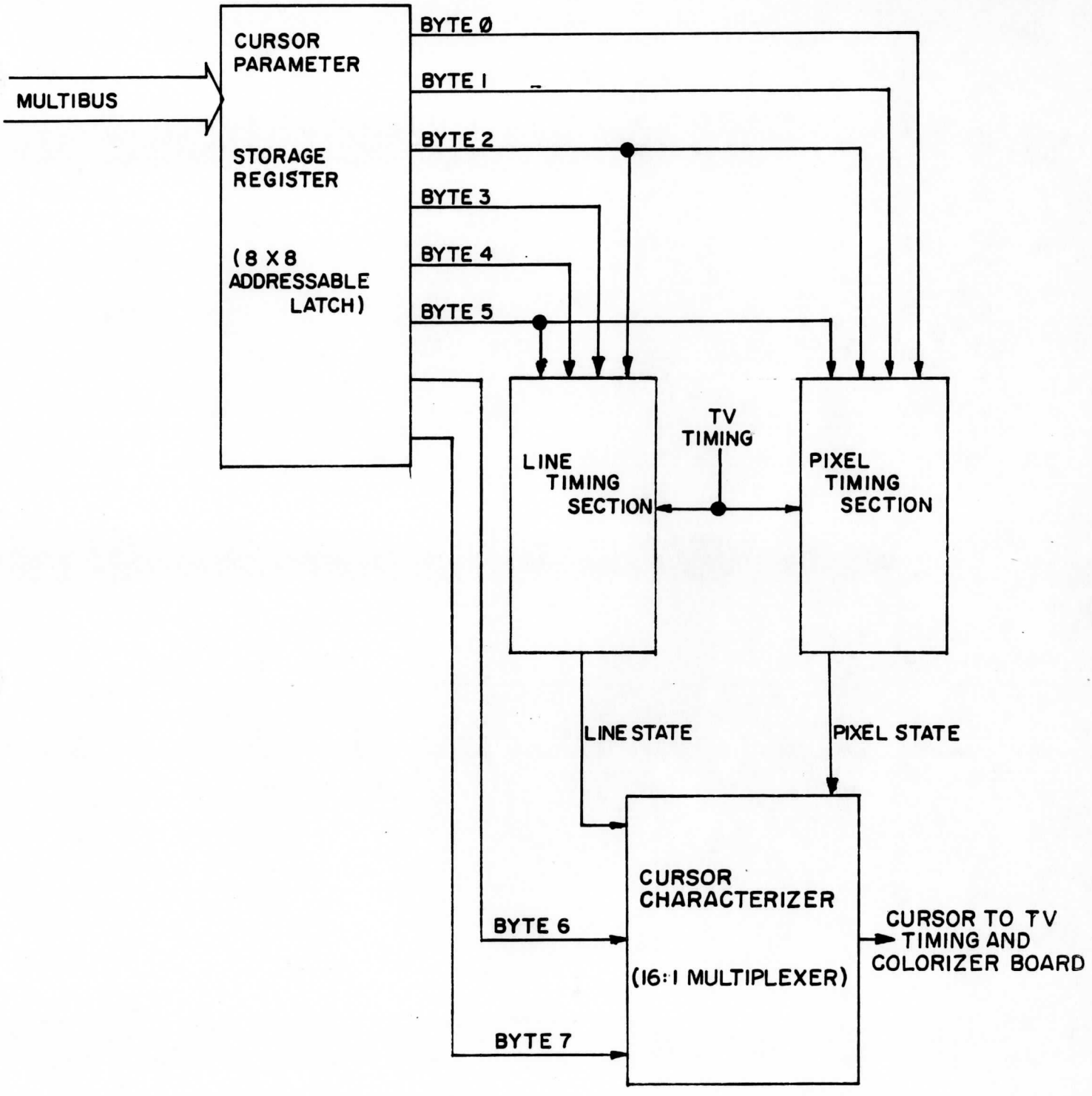
The eight-byte storage register is an addressable latch which continuously supplies parameter data to the other functional blocks, until it is changed by the microprocessor under user control.

The generator is made up of two nearly identical blocks, the line and pixel timing blocks. The blocks compare desired cursor position and size data with present scan position and generate the following four output codes, called "states":

- non-cursor area (state Ø)
- cursor edge (state 1)
- cursor interior (state 2)
- cursor center (state 3)

Sixteen state combinations exist because there are four states in both the horizontal and vertical axis.

The four states in each logic block are combined to form two 2-bit words. The two words are applied as addresses to the Cursor Characterizer. The user assigns a "one" or "zero" to each of the 16 state inputs, via cursor parameter bytes 6 and 7. The characterizer gates one of these inputs, as determined by the two address words from the Cursor Line Timing



CURSOR GENERATOR FUNCTIONAL BLOCK DIAGRAM
(3504-029)

FIGURE 2

and Cursor Pixel Timing blocks to the output. The output of the Cursor Characterizer block is applied to the 60/50 Hz TV Timing and Colorizer-Brooktree board. The output for each pixel scanned is a single bit. If the cursor bit is on, the pixel is a cursor pixel. Otherwise, it is either a graphics or image pixel.

JOYSTICK SUPPORT INTERFACE FUNCTIONAL DESCRIPTION

The Digital Joystick 2 board digitizes the four analog joystick potentiometer outputs and asynchronously transmits the data serially to the Joystick Support Interface unit. Eight bytes of data are transmitted to this unit, that is, two bytes for each of the four potentiometers (pots).

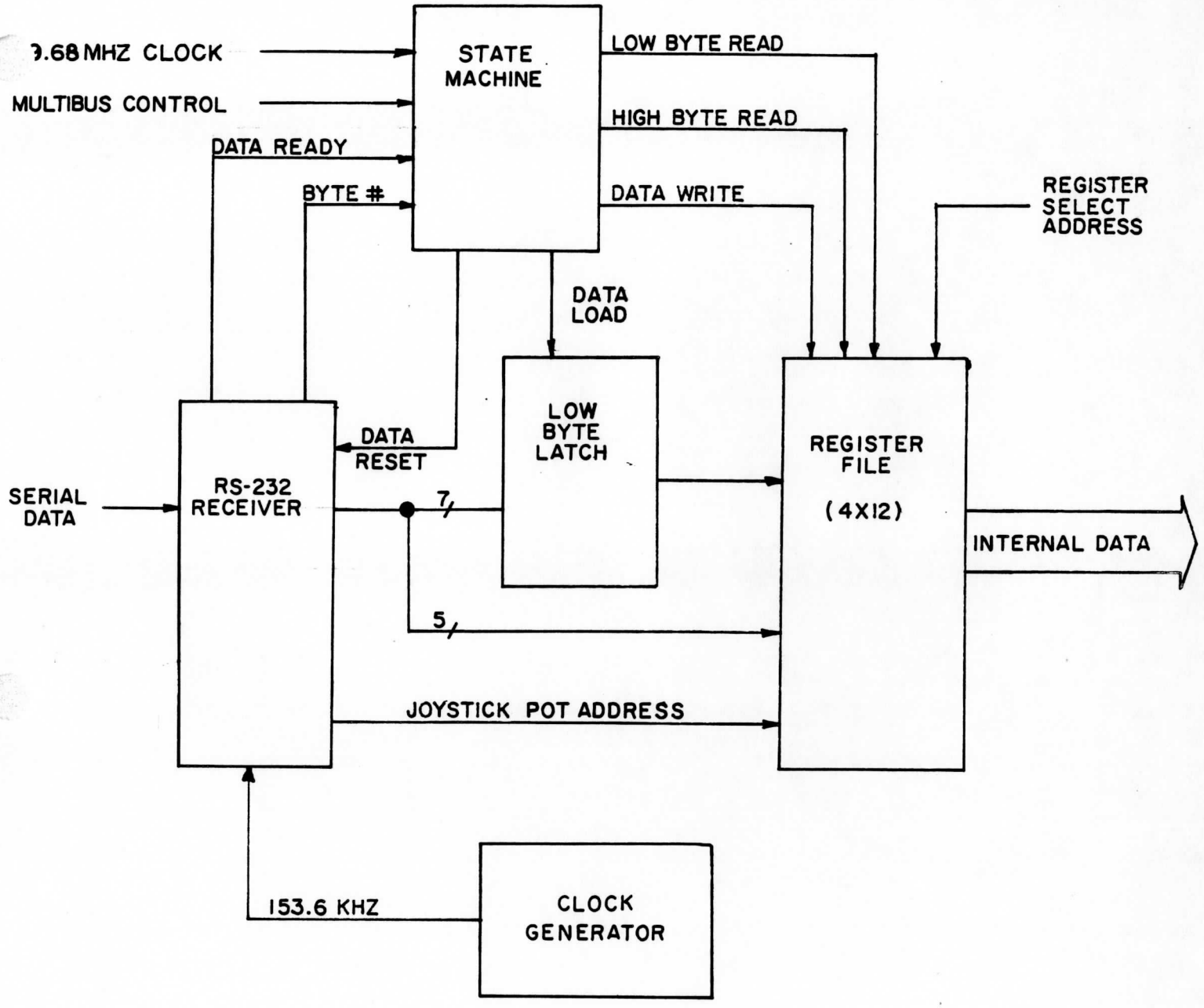
The Digital Joystick 2 board outputs 800 characters per second to the Joystick Support Interface unit (400 pairs). There are four pots, so each pot position is updated 100 times per second. Essentially, this unit must do the following:

- organize the characters into pairs
- store the 12 data bits from each pair in a Register File
- output microprocessor-requested pot position data (via the MULTIBUS)

Figure 3 is a functional block diagram of the Joystick Support Interface. All control logic for this unit is contained in the State Machine. Outputs from the State Machine control the RS-232 Receiver, Low Byte Latch, and Register File read and write operations. The RS-232 Receiver block converts the 9600-baud serial data to parallel format.

The Clock Generator is a crystal-controlled oscillator that drives a divide-by-64 network to produce a 153.6-Khz clock drive to the UART. The UART requires a clock which is 16 times the baud rate. When the UART detects the end of a character, a data ready (DR) command is sent to the State Machine. The UART also sends the first data bit (this is the character ID, refer to the Digital Joystick 2 section) to the State Machine. If the ID bit is a "zero" (1st character), the State Machine enables the Low Byte Latch, which temporarily stores the low seven data bits. If the ID bit is a "one" (2nd character), the State Machine enables the Register File Data Write line.

The Register File consists of four 12-bit buffers. Prior to writing data to the Register File, one of the four buffers must be selected. The



JOYSTICK SUPPORT INTERFACE FUNCTIONAL BLOCK DIAGRAM

(3504-029)

FIGURE 3

joystick pot address data contained in the 2nd character is used as the Data File address. Therefore, each two-character pair contains its own storage address. Each buffer in the Register File is updated (overwritten) 1ØØ times per second, making position information continuously available. The Register File allows data to be written to and read from simultaneously, from the same or different locations. Pot position data is output to the MULTIBUS when requested by the microprocessor via the Internal Data bus. Two data reads are required to transmit the 12 position bits. The MULTIBUS read requests are processed by the State Machine.

DETAILED CIRCUIT DESCRIPTION

The schematic diagrams of the Cursor Generator and the Joystick Support Interface are shown on SSEC drawing #35Ø4-Ø29 (Modification L, dated 11/21/86) sheets 1-4. The schematic circuit analysis is accomplished by analyzing groups of components represented by single blocks on the respective functional block diagrams. The circuitry common to one or more units on this board is described before the individual units are described.

The SSEC circuit schematics are labeled by the column and row in which pin 1 of that chip resides. This is very helpful for troubleshooting, since the symbol ID is also the chip location. However, IC gates, flip-flops, buffers, and inverters usually have several identical logic circuits packaged on the same IC. Therefore, when reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and a section identification letter. The symbol ID number alone is used to refer to single function ICs.

SHARED CIRCUITS DESCRIPTION

The following circuits are shared by one or more units:

- MULTIBUS interface circuits
- Internal bidirectional data bus
- IO (Input/Output) mapping logic

The MULTIBUS interface circuits consist primarily of line drivers and line receivers; however, an important exception is the MULTIBUS signal XACK

(Transfer Acknowledge). From the perspective of the microprocessor, all units on this board function as I/O devices. The 8Ø/24A microprocessor board requires an external response (XACK) to any off-board I/O write or read requests. The microprocessor enters a wait state and ceases all other processing until XACK goes true (or microprocessor board time out occurs), informing the CPU that the request has been carried out by the off-board hardware. There are two separate I/O units on this board; each must provide an acknowledge input to the XACK generator.

The Joystick Support Interface is an I/O read-only device and generates the acknowledge signal JACK. The output of Z3-A (JACK - see Sheet 4) is ANDed with IORC by gate A32-D to form READ. READ, therefore, goes active high if the Joystick acknowledges a CPU I/O read request. READ controls the Internal data bus, as explained later, and is combined with WRITE by OR gate AB3-B. WRITE is an acknowledge signal generated by the Cursor Generator unit. The output of AB3-B is inverted by E12-F and applied to the enable input of tri-state line driver T32-F. When enabled, the line driver's output (XACK) is pulled low, providing the required acknowledge to the 8Ø/24A board.

The internal bidirectional data bus is connected to the MULTIBUS data lines (DATØ-DAT7) by two bidirectional four-bit bus drivers (V32 and X32 on page 1). The enable pins (1 and 13) of both drivers are driven by READ (true during I/O read operations to the joystick unit), allowing data onto the MULTIBUS only during READ time. At all other times, the bus drivers allow incoming data to go from the MULTIBUS to the internal bus. The internal data bus goes to both units on the board.

The I/O mapping logic is G32, a 512 by 4-bit PROM. The #54B program in the PROM allows a high on pin 11 ("Y") if the address on the inverted address lines is 38H-3FH. This eight-address block addresses the Cursor Generator unit during "write" operations and addresses the Joystick Support Interface unit during "read" operations.

CURSOR GENERATOR CIRCUIT DESCRIPTION

The Cursor Generator is located on sheets 1-3 on the SSEC #35Ø4-Ø29 drawing. The Cursor Parameter Storage Register, as previously shown in Figure 2, consists of eight 8-bit addressable latches (N3, N12, N23, N32,

R3, R12, R23, and R32). Each latch stores one bit in one of eight output latches, determined by the three input address lines: A, B, and C (pins 1, 2, and 3 respectively).

The data inputs to the eight latch ICs are the eight data lines of the Internal bus. The Internal data bus is connected to the MULTIBUS data lines at all times except during an I/O read to the joystick unit. The latch address lines (A, B, and C) are all connected in parallel, as are the enable inputs (pin 14). If a latch is enabled on one chip, the corresponding latch on all eight chips is enabled. Because all address lines are parallel-connected, all chips load data into the same corresponding latch. As an example, assume that the data on DATØ/-DAT7/ are Ø11Ø11ØØ respectively and BAØ-BA2 are Ø11 (binary representation of 3). After the latches are enabled (pin 14 goes low), the Q3 output of the eight latches is ØØ11Ø11Ø (left to right). The outputs from these devices do not change unless the CPU writes over the data. During turn-on or reset, INIT goes active low, setting all outputs to zero.

Addressing the latches is accomplished by applying the lower three address lines (BAØ, BA1, and BA2) to the A, B, and C inputs respectively and driving the enable pins low (pin 14). Gate A32-A ANDs the "Y" output from the PROM (active high for addresses 38H-3FH) with IOWC to produce WRITE. WRITE is inverted by E12-D to produce the addressable latch-enable signal.

The outputs from the addressable latches are wired so that the eight $Q_{Ø}$ outputs of all eight latches form "byte Ø," Q1 outputs form "byte 1," . . . and Q7 outputs form "byte 7." These outputs remain static until changed by the CPU or initialized to zero during turn-on or reset.

Line Counter Section

The schematic diagram for the Line Counter Section of the Cursor Generation Functional Block Diagram (Figure 2) is shown on SSEC drawing #35Ø4-Ø29, sheet 2 of 4.

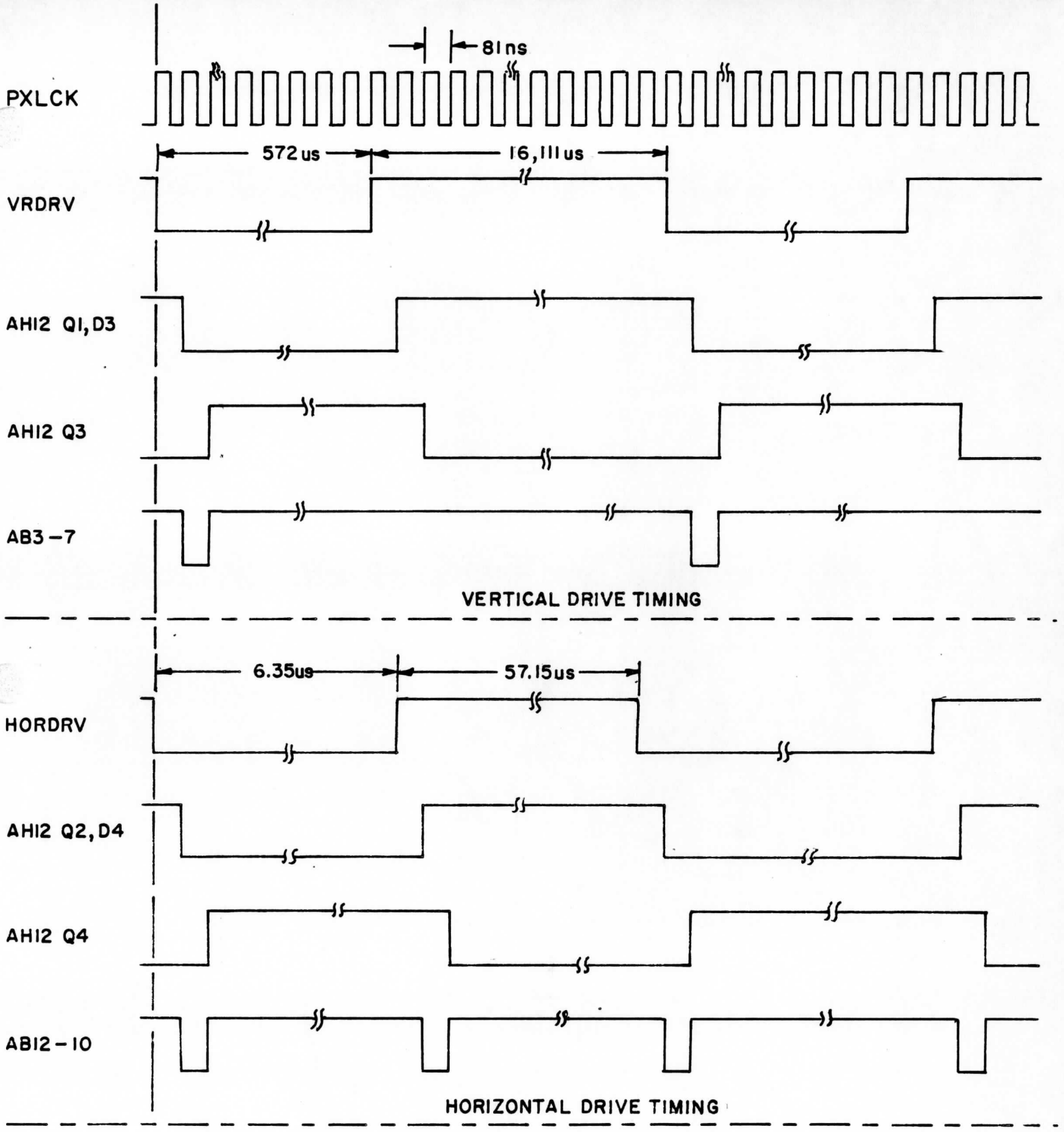
Three timing signals, VRDRV, HORDRV, and PXLCK (vertical drive, horizontal drive, and pixel clock respectively), are applied to this section from the P2 bus via line receivers AP32-A, AP32-B, and AP32-D respectively. The 12.915-Mhz PXLCK (12.88636 Mhz if equipped with the optional PAL (NTSC) TV Sync board) synchronously clocks all D latches and counters in this section.

The horizontal and vertical drive signals (see Timing Diagram 1) are applied to quad D-latch AH12. Two sections of AH12 (#1 and #3) are used by VRDRV while the other two sections (#2 and #4) are used by HORDRV. The latch is wired so that the output of the first section of each pair follows its respective drive signal (VRDRV or HORDV) but delayed one PXLCK period; the output of the second section of each pair is the complement of the respective drive signal and delayed two PXLCK periods. In both sections, the delay between the drive and its complement is one PXLCK period (81 nsec). The vertical drive and its delayed complement are applied to OR gate AB3-C to produce an active low 81-nanosecond pulse at the beginning of each vertical field. The horizontal drive and its delayed complement are applied to Exclusive OR gate AB12-C to produce two active low pulses separated by 6.35 μsec (see Horizontal Drive Timing in Timing Diagram 1). The requirement for two horizontal pulses is explained shortly.

As explained earlier in the Cursor Generator Functional Description, any pixel (or cursor position) can be described by its X,Y coordinates. However, the 525 horizontal lines which make a complete picture are scanned in two alternate groups or fields, containing 262.5 lines per field. During the odd field scan, only the odd lines are scanned; during the even field scan, only the even lines are scanned. Therefore, there is a vertical drive pulse every 262.5 horizontal lines. To properly locate the cursor vertically, the line counter must count both even and odd lines during a field. Thus, two horizontal pulses per line scan must be sent to the line counter.

The line counter consists of three Up/Down binary counters connected in cascade (V3, V12, and V23). Data inputs from the Addressable Latch (see sheet 1) are applied to the preset inputs of the counters.

The preset data represents the desired distance from the top of the screen to the horizontal center of the cursor. The active low vertical drive pulse output from AB3-C is the preload pulse for the counter. Note that the vertical drive pulse is also applied to the clear input of Z23 (quad D-Latch), resulting in a low level at the output of OR gate X23-D. The output of X23-D drives the Up/Down input on the line counters. Upon receiving a vertical drive pulse, the counters are preloaded to the center line of the cursor and the counter is in a count-down mode.



TIMING DIAGRAM I

CURSOR DRIVE SIGNAL GENERATION

(3504-029 SHT.2)

The only additional inputs to the counters are the Horizontal Drive pulse and pixel clock. The horizontal drive enables the counters for one pixel period twice each horizontal scan, resulting in a double decrement.

The outputs from the counters are applied to AND gate X12 and to a 12-bit comparator consisting of three 4-bit magnitude comparators connected in cascade (T3, T12, and T23). The Addressable Latch supplies cursor range data to the comparator. Refer to Figure 4. The range (vertical width) is the number of horizontal lines above and below the cursor center line. As the counter decrements, it eventually matches the Addressable Latch inputs. When this occurs, the "=" pin (pin 6) of T23 goes active high, indicating that the two sets of inputs to the comparator are equal. This signal indicates the edge of the cursor (top or bottom) and is applied to the D1 input of Z23 via OR gate X23-A. After the next counter decrement, the counter input to the comparator is smaller than the Addressable Latch inputs, causing the "=" pin to return to its inactive low state and the "<" pin (pin 7) to go high. The "<" signal is applied to the D2 input of Z23 via OR gate X23-B; it indicates that this line is an interior cursor line (state 2). The counter continues to count down until it reaches "zero". On the next line, the counter underflows to all binary "one"s, qualifying NAND gate X12. NAND gate X12 is the center detector. The output of the NAND gate is inverted by buffer Z12-A and applied to the D4 input of Z23 via OR gate X23-D. The latched output from Q4 of Z23 is applied to OR gate X23-D. The resulting high output from the OR gate (X23-D) causes the counter to count up through the remainder of the field. The counter continues to count up and the comparator continues to indicate interior cursor lines until the counter and Addressable Latch inputs to the comparator match again, indicating the bottom edge of the cursor (see Figure 4).

The "=", "<", and Center Detector outputs are combined by OR gates X23-A, X23-B, and X23-D and latched by Z23 to form a two-bit binary code. The code is defined as follows:

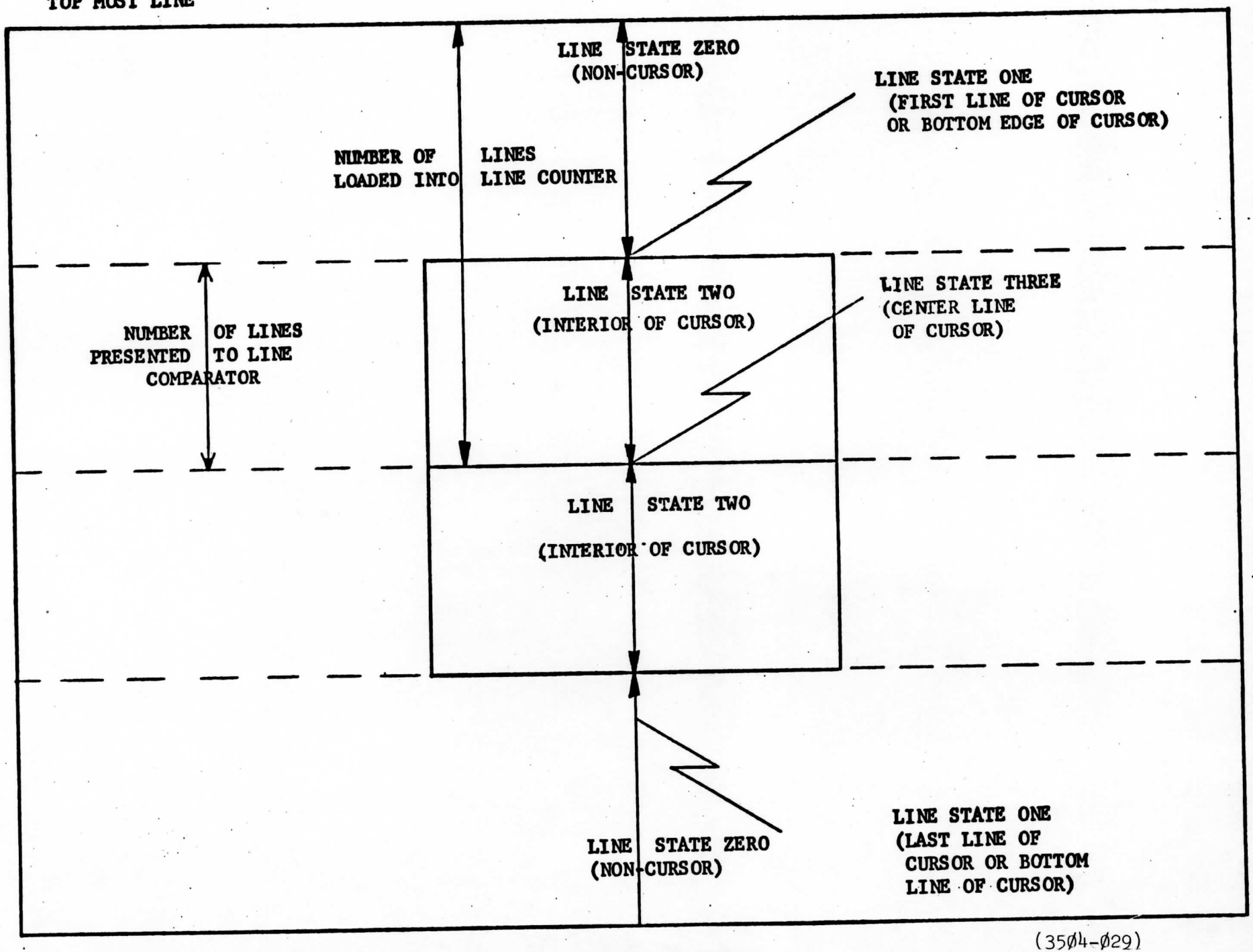


Figure 4. Line Cursor States (Vertical)

State	Q_2	Q_1	Function (Line State)
Ø	Ø	Ø	Non-cursor lines
1	Ø	1	Top or Bottom Edge
2	1	Ø	Interior Cursor Lines
3	1	1	Center Cursor Line

The two-bit binary code, covered after the Pixel Counter Section, is applied to the Cursor Characterizer. The "State" is the decimal equivalent of the two-bit binary code.

Pixel Counter Section

The Pixel Counter Section is shown on SSEC drawing #3504-029, sheet 3 of 4. This section, describing the horizontal position of the cursor, is nearly identical to the line counter section. Only the differences between the two coutners are discussed here.

Horizontal position is determined by counting pixels from the left edge of the screen. The 12-bit counter (J3, J12, and J23) is pre-loaded with the desired number of pixels, measured from the left of the screen to the vertical center axis of the cursor (refer to Figure 5). During pre-load, the horizontal drive pulse is applied to the load pin of the three counter chips. The counters count down or up at the pixel clock rate (PXLCK). The 12-bit comparator (L3, L12, and L23) compares the input from the counter with the input from the Addressable Latch. The input from the Addressable Latch is the desired cursor width (vertical range) from the edge of the cursor (left or right edge) to the cursor's vertical center line (see Figure 5).

The edge-, interior-, and center-detection processes are identical to those in the Line Counter Section. The Q2 and Q3 outputs of latch E23 function as a two-bit binary code and are defined as follows:

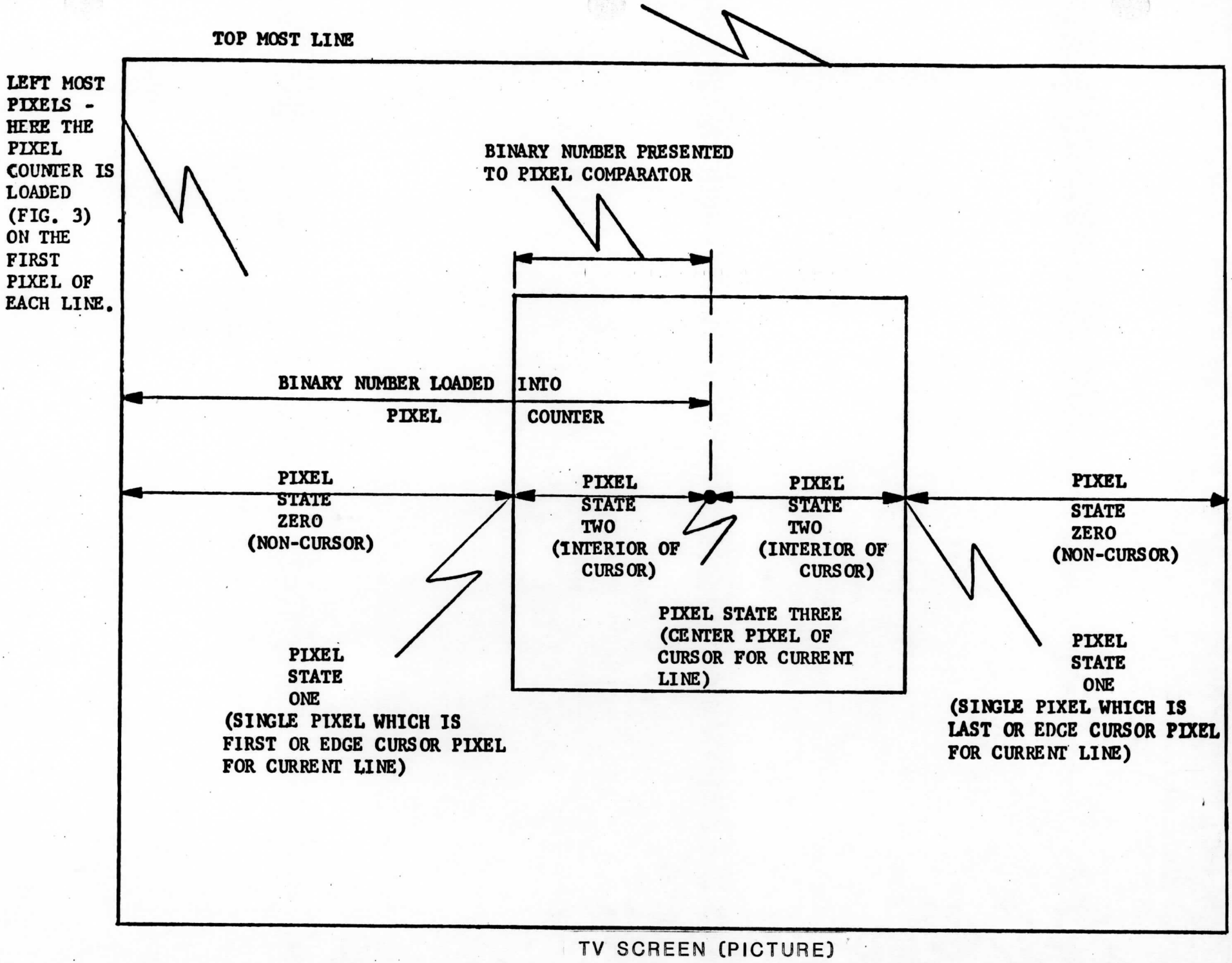


Figure 5. Pixel Cursor States (Horizontal) 3504-029

State	Q_2	Q_1	Function (Pixel State)
Ø	Ø	Ø	Non-cursor pixels
1	Ø	1	Left or right edge cursor pixels
2	1	Ø	Interior cursor pixels
3	1	1	Center cursor pixel

This two-bit binary code is applied to the Cursor Characterizer, discussed in the next paragraph.

Cursor Characterizer Section

The Cursor Characterizer Section is K32, a 16-to-1 line multiplexer; it is located on sheet 3 of 4, SSEC drawing 35Ø4-Ø29. The multiplexer gates only one of its 16 input lines to the output line (pin 1Ø). An input line is selected by a four-bit address input (A, B, C, and D inputs to pins 15, 14, 13, and 11 respectively). The "A" and "B" address inputs are driven by the two-bit binary state code output of the Line Counter Section output latch, while the "C" and "D" address inputs are driven by the output of the Pixel Counter Section latch. The characterizing input to the multiplexer comes from the Addressable Latch (bytes 6 and 7). There are four binary address inputs, so 16 possible states exist. One of 16 inputs is selected as follows:

PIXEL			LINE				
D	C	State	B	A	State	Input Pin	Characteristic (if selected input is high)
Ø	Ø	Ø	Ø	Ø	Ø	8	Exterior lines and pixels
Ø	Ø	Ø	Ø	1	1	7	Edge line, exterior pixels
Ø	Ø	Ø	1	Ø	2	6	Interior line, exterior pixels
Ø	Ø	Ø	1	1	3	5	Center line, exterior pixels
Ø	1	1	Ø	Ø	Ø	4	Exterior line, edge pixels
Ø	1	1	Ø	1	1	3	Edge line, edge pixel
Ø	1	1	1	Ø	2	2	Interior line, edge pixel
Ø	1	1	1	1	3	1	Center line, edge pixel
1	Ø	2	Ø	Ø	Ø	23	Exterior line, interior pixels
1	Ø	2	Ø	1	1	22	Edge line, interior pixels
1	Ø	2	1	Ø	2	21	Interior line, interior pixels
1	Ø	2	1	1	3	2Ø	Center line, interior pixels
1	1	3	Ø	Ø	Ø	19	Exterior line, center pixels
1	1	3	Ø	1	1	18	Edge line, center pixels
1	1	3	1	Ø	2	17	Interior line, center pixels
1	1	3	1	1	3	16	Center line, center pixel

Figure 6 shows the line and pixel state designations for cursor construction. The output of K32 is sent to the TV Timing and Colorizer board via buffer E12-C, latch E23, and line driver AF1-A. If the output is a "one", the TV Timing and Colorizer board treats the pixel being processed as a "cursor pixel." If the output is a "zero", the 6Ø/5Ø Hz TV Timing and Colorizer Board-Brooktree treats the pixel as an image or graphics pixel. The Cursor Generator Section provides cursor status information, pixel by pixel, to the TV Timing and Colorizer board.

JOYSTICK SUPPORT INTERFACE CIRCUIT DESCRIPTION

The Joystick Support Interface schematic is located on sheet 4 of 4, SSEC drawing #35Ø4-Ø29.

Power for the Joystick module (±12V) is provided by the Cursor Generator via J3.

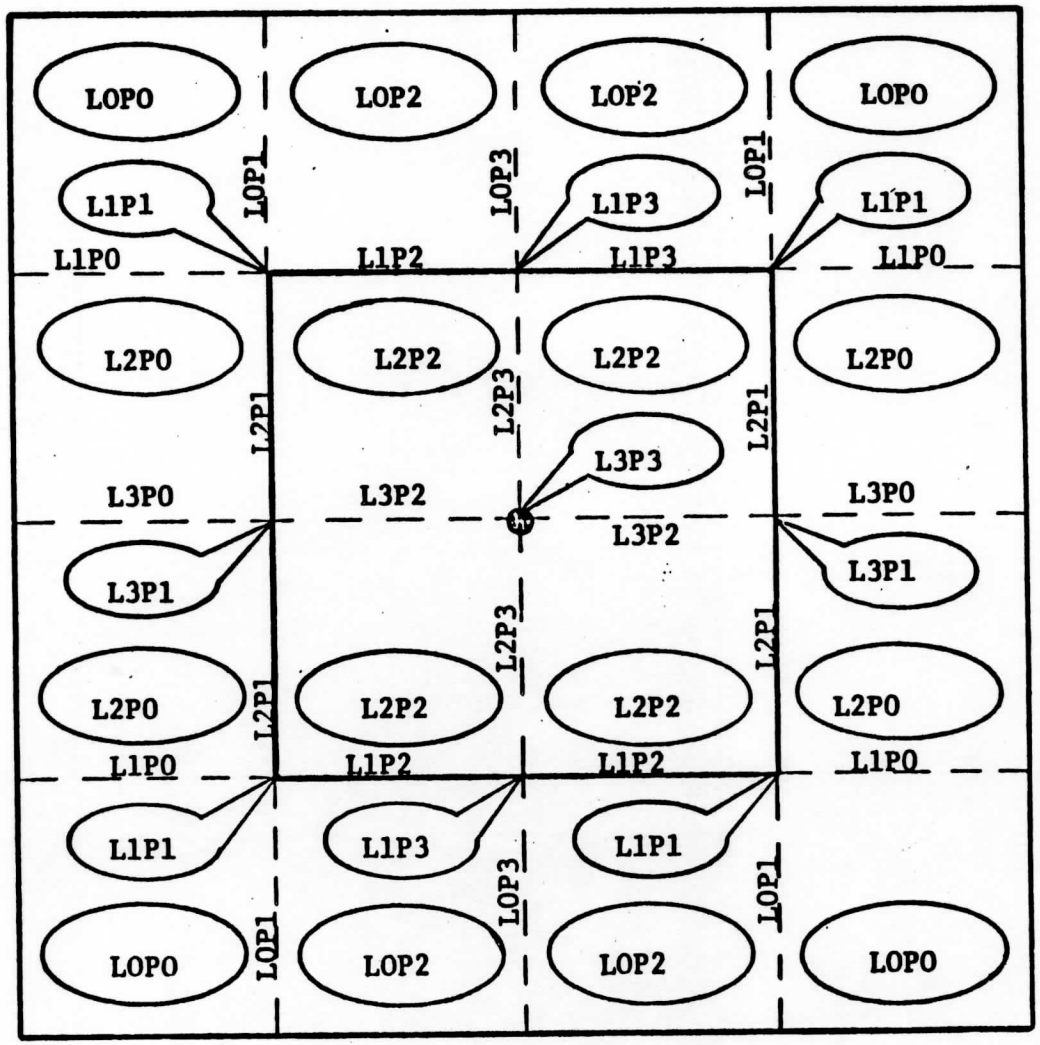


Figure 6. State Designations for Cursor Construction
(3504-029)

The 96ØØ-baud serial asynchronous joystick position data enters the board from J3 pin 5, is converted to TTL logic by line receiver AH3-B, and is applied to the universal asynchronous receiver/transmitter (UART) AF23. The Clock Generator consists of 9.83Ø4-Mhz crystal oscillator AM28, inverting buffer Z12-F, D-latch AP19-D, four-bit binary counter AM37, and D-latch C3-A. The output from the oscillator is buffered by Z12-F and applied to D-latch AP19-D. AP19-D is configured as a divide-by-two circuit, yielding an output frequncy of 4.9152 Mhz. The latch output is applied to the counter (AM37) which divides the input by 16, producing 3Ø7.2-Khz input to C3-A. C3-A is also a D-latch and is configured as a divided-by-two circuit. Thus, the output of C3-A is 153.6 Khz and is the clock frequency for the UART (AF23).

The MULTIBUS initialization signal (INIT/) enters the board from P1 pin 14, is buffered and inverted by hex buffer Z12-D, and is applied to the master reset (pin 21) on the UART. This initializes (clears) the UART during power-up and manual resets. The program wiring of CLS1, CLS2, SBS, PI, and CLR (pins 38, 37, 36, 35, and 34 respectively) configures the UART for eight data bits, odd parity, and two stop bits. The parity bit is invalid, as explained in the Digital Joystick 2 circuit description. The Parity Error output (pin 13) from the UART is not used.

When the UART detects the completion of a character, the following occurs:

- the eight data bits are latched into the output receive buffer (RB1-RB8, RB1 is LSB)
- the data-received line (DR) goes active high

After the DR line goes high, it must be cleared before completion of the next character (1.25 ms). By providing a high input to DRR (Data Received Reset) pin 18, DRR is interpreted by the UART as a "data read complete." The UART resets the DR to inactive low. The DR output signal is used as one of the inputs to the State Machine (AF1Ø, AD1Ø, and AB23). The DRR reset input signal is an output from the State Machine. Note that the LSB (RBR1) of the eight-bit output register is also used as an input to the State Machine. This is the "ID" bit in each character transmitted by the Digital Joystick 2 board. If the bit is a "zero", RBR2-RBR8 contain the lower seven data bits (RBR2 is LSB). If the bit is a "one", RBR4-RBR8 contain the upper five data bits (RBR8 is MSB).

There are three requirements for storing data into the register file (Z32, AB32, and AD32): all 12 data bits must be presented to the file at the same time, a file address must be selected, and a "Write Enable" must be applied to the file. The State Machine outputs an active logic low from Y_1 (pin 14) of AB23 when DR is a logic high and the "ID" is a logic low. This signal latches the data inputs into octal latch AD21. The inputs to AD21 are the seven least significant data bits of a joystick position. Note that the two LSBs from the UART are applied to two exclusive OR gates. These gates function as buffers, required because of the extra TTL loads on these two lines. (In addition to supplying the D1 and D2 latch inputs, the buffers drive the "Write Address" lines on all three register file chips.) After AD21 is latched, its seven data bits are present at the seven LSB input positions of the register file. After the UART completes the next character, DR goes high again; but this time, the "ID" bit is also high. At this time, RBR4-RBR8 are outputting the upper five data bits to the five MSBs of the register file, fulfilling the first requirement for storing data in the data file. Remember, the potentiometer address is contained in the second and third bit positions of the second character (the two buffered UART output lines). The address data is presented to the latch, but has no effect because the latch inputs are not enabled at this time. The address data is also applied to "Write Address" inputs to the register file (pins 12 and 13), fulfilling the second requirement for storing data in the register file. Only the application of a "Write Enable" pulse is needed to write the data into the register file. This pulse is generated by the State Machine.

The State Machine is best understood by examining it during two separate process cycles, data storage and data retrieval. Since we have just finished describing the data storage process, that portion of the State Machine is addressed. The State Machine consists of the following:

- octal D-latch AF1Ø
- PROM AD1Ø
- 3-to-8 line decoder AB23

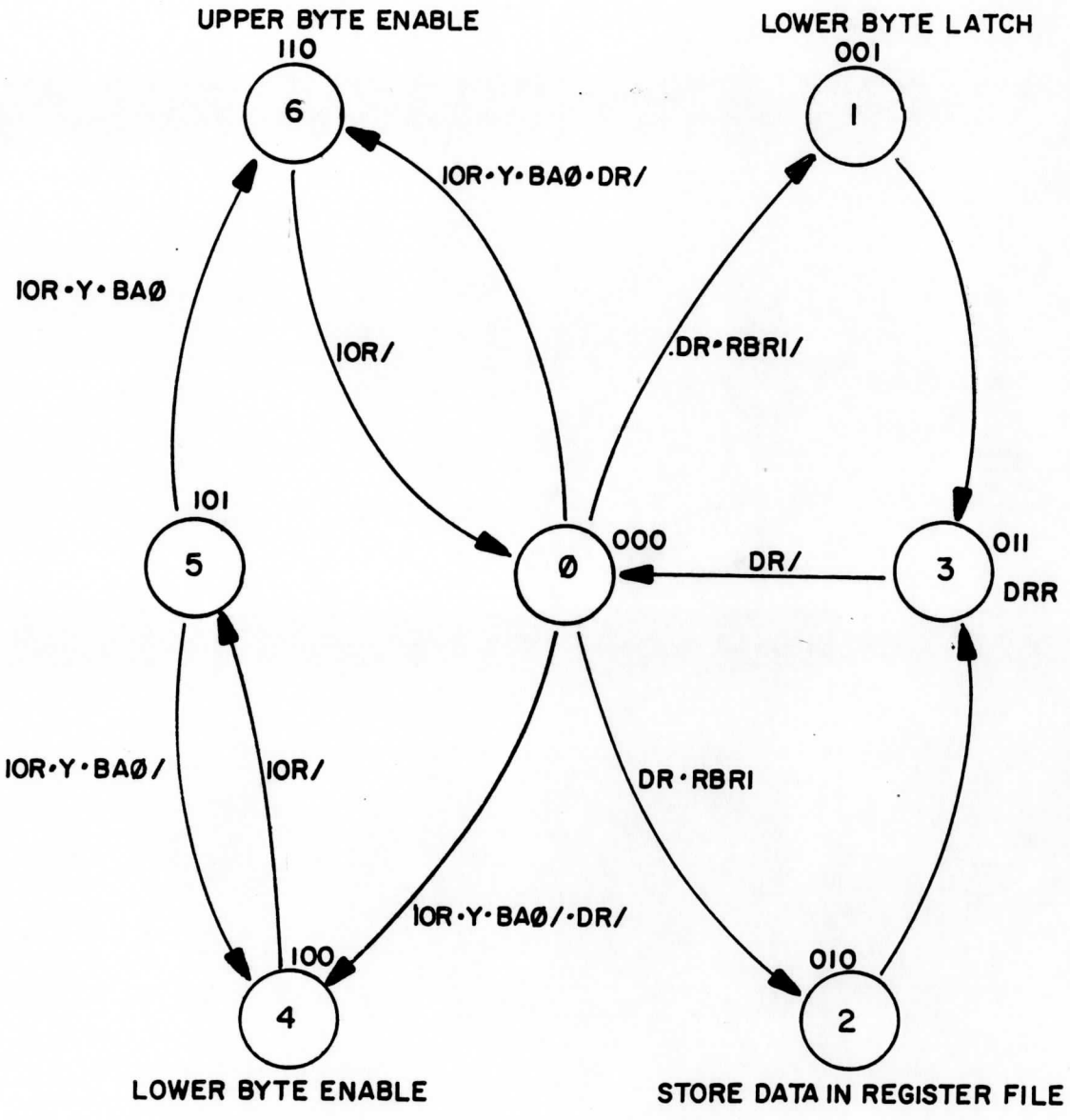
Note that the least significant three bits output from the PROM are used as the least significant three bits input to the latch. Because the latch

output drives the PROM address lines (lower eight lines) and the latch is clocked by the MULTIBUS 9.68-Mhz clock (SBCCK, P1-31), the present PROM output always determines the A5, A6, and A7 (AD1Ø pins 2, 1, and 15 respectively) inputs after the next 9.68-Mhz clock pulse. The present PROM output becomes a directory to the next process. By loading the proper data into the PROM, a very complicated sequence of timing steps is possible with just three components. Because the inputs to the 3-to-8 line decoder are actually the A5, A6, and A7 address lines, a PROM address-to-decoder function correlation can be made. The table below, shows this correlation.

PROM Address (Hexidecimal)	Decoder Output	Function
ØØØ-Ø1F	$Y_Ø$	not used
Ø2Ø-Ø3F	Y_1	1st character latch
Ø4Ø-Ø5F	Y_2	position data store
Ø6Ø-Ø7F	Y_3	data received reset
Ø8Ø-Ø9F	Y_4	LS 8-bit read
ØAØ-ØBF	Y_5	not used
ØCØ-ØDF	Y_6	MS 4-bit read
ØEØ-OFF	Y_7	not used

During the following analysis, refer to Figure 7, the Joystick Support State Diagram, and the PROM code listings (at the end of this section). If we assume that no data "read" or "write" is in progress, then IORC=Ø, Y=Ø, and DR=Ø. RBR1 and BAØ are not significant (as we'll see). The possible address inputs to the PROM under these conditions are ØØH, Ø2H, Ø4H, and Ø6H. The output from the PROM, in each case, is ØH, therefore, the output from AB23 is $Y_Ø$ (idle output).

Assume that the first character of a pot position data pair has just become available (DR goes high and RBR1 is low). After the next 9.68-Mhz



JOYSTICK SUPPORT STATE DIAGRAM

FIGURE 7

(3504-029)

clock pulse the input to the PROM is ØØ1H or ØØ5H (we don't know about BAØ yet). In either case, the PROM output is Ø1H and the data input to the latch is 84H or A4H. After the next clock pulse, this data is latched into the PROM address inputs as Ø21H or Ø25H and the inputs to the decoder yield Y_1 (state 1 in Figure 7). Y_1 causes the octal latch (AD21) to store the UART output data. The PROM input produces an output of Ø3H and the latch (AF1Ø) input is now 86H or A6H. After the next clock pulse, the input to the PROM is Ø61H or Ø65H and the decoder outputs Y_3 (state 3 in Figure 7), resetting DR. When DR is reset, the next clock pulse provides an address of 6ØH or 64H to the PROM, generating an output of ØH. After the next clock pulse, the PROM is back to ØØØH or ØØ4H. Assume that the second character has just arrived and BAØ = "zero", as it has no effect during data store cycles. The latch (AF1Ø) input is ØCØH. After the next clock pulse, the PROM input is ØØ3H, causing an output of Ø2H. With a PROM output of Ø2H, the latch (AF1Ø) input is ØC2H. After the next clock pulse, the PROM input address is Ø43H, producing an output from AB23 of Y_2 (state 2 in Figure 7). Y_2 is the Write Enable for the Register File. The lower seven bits (stored in latch AD21) and the upper five data bits from the UART are stored in one of the files (determined by the Write Address inputs). With a PROM input of Ø43H, the output is Ø3H. After the next clock pulse, the decoder generates a Y_3 output and resets the DR line. The PROM address input is now Ø63H. With the DR line reset and RBR1 still set, the latch data input is Ø46H. After the next clock pulse, the input to the PROM is Ø62H, generating an output of ØH. After the next clock pulse, the PROM input is ØØ2H and the decoder's output returns to $Y_Ø$, completing the cycle.

The data read analysis process is identical to the data storage analysis just described (see analysis above). A listing of the data read control signal inputs follows:

- IORC (I/O Read Command)
- Y (addresses 78-7F hex)
- BAØ (address bit zero)

Note that the BA1 and BA2 are used as read address lines for the Register File. BA1 and BA2 select the file number (1, 2, 3, or 4), while BAØ, via the State Machine, selects the byte (lower or upper). Specifically, the

State Machine requires that both IORC and Y must be present before BAØ determines which byte to output. Note that JACK goes true any time a data read request is processed (see Common Circuits Description).

It appears that many of the PROM states were not used because only one function (of the two) was analyzed at a time. Often, both functions are processed concurrently, accessing other PROM states. The following are noteworthy features about the programming of the State Machine:

1. After a two-byte read cycle process begins, nothing can break into it (UART must wait).
2. If the UART requests service at the same time that a read cycle is requested, the UART is serviced first.

11/PCAT/05

53.PRM 63S241N MMI
Time 14:41:21
Tuesday 29 September 1987

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0	1	0	2	0	1	0	2	0	1	0	2	0	1	0	2
001	0	1	0	2	0	1	0	2	4	1	4	2	6	1	6	2
002	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
003	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
004	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
005	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
006	0	3	0	3	0	3	0	3	0	3	0	3	0	3	0	3
007	0	3	0	3	0	3	0	3	0	3	0	3	0	3	0	3
008	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
009	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
00A	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
00B	5	5	5	5	5	5	5	5	4	4	4	4	6	6	6	6
00C	0	1	0	2	0	1	0	2	0	1	0	2	0	1	0	2
00D	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
00E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
011	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
012	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
013	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
014	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
015	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
016	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
017	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
018	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
019	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01B	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

54B.PRM 63S241N MMI
Time 09:25:23
Wednesday 30 September 1987

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
005	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
006	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
007	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
009	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00C	A	A	A	A	A	A	A	A	0	9	0	C	C	C	C	C
00D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
012	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
013	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
015	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
016	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
017	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
019	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

127B.PRM 63S241N MMI
Time 14:41:33
Tuesday 29 September 1987

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002	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
003	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
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007	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
008	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
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00B	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
00C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
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010	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
011	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
012	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
013	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
014	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
015	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
016	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
017	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
018	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
019	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01B	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

SECTION 6
DATARAM CONTROL BOARD
TABLE OF CONTENTS

DATARAM CONTROL BOARD

(SSEC DRAWING 645Ø-Ø377, MODIFICATION F, DATED 4/23/84)

INTRODUCTION

Present generation McIDAS Workstations use "off-the-shelf" dynamic RAM storage units manufactured by DATARAM Corporation. Each workstation uses three units, one for each of the two image channels and a third for the graphics channel.

In a typical DATARAM application, a DATARAM BS-102 7-inch chassis contains the following:

- an integral power supply
- a Bulk Interface Card (BI)
- a Bulk Semi Controller (BSC)
- up to four Bulk Semiconductor Array boards (BSA)

A BSC provides drive and addressing for all BSA (memory) boards. The BI card provides the interface between the memory system and the CPU. Because the McIDAS data storage protocol is unique, none of the several versions of BI cards manufactured by DATARAM Corporation satisfy the protocol requirements. As a result, the DATARAM Control Board was custom-designed by SSEC. The custom card plugs into the BI slot of the DATARAM Chassis and no DATARAM Chassis or circuit board alterations are required.

The DATARAM Control Board performs two major functions. It provides the protocol interface between the Intel MULTIBUS used in the McIDAS and the DATARAM Memory System (We use the term "DATARAM Memory System" to include: one chassis with integral power supply, one Bulk Semi Controller Card, a DATARAM Control Board, and one or more BSA boards.), and it provides considerable automation for the data storage and retrieval processes, reducing microprocessor overhead. Because one major function of this board is to interface two very different protocols, a thorough understanding of this board requires an in-depth understanding of both systems' protocols. The DATARAM protocol is documented in the Bulk Semi Memory System Model DR-129/229S technical manual by DATARAM Corporation.

If additional information is required on the MULTIBUS, consult the INTEL SBC 80/24A technical manual.

Because of the complexity of the DATARAM Control Board, the Functional Description is divided into a "Functional Overview," and a "Detailed Function Description." The overview provides the big picture while the detailed description provides approximately the same level of detail as the "Functional Description" sections of other SSEC board documentation.

FUNCTIONAL DESCRIPTION

OVERVIEW

McIDAS is a TV-video-frame-based machine, that is, data storage and retrieval are performed by specifying video frame numbers. A TV video frame consists of 525 horizontal lines containing 78Ø pixels each. Several lines, and several pixels at the ends of each line, are blanked by the vertical and horizontal blanking periods respectively. For memory allocation within the workstation DATARAM memory, a video frame is defined as 512 lines containing 64Ø pixels each. Therefore, each frame contains 327,68Ø pixels. Since an Intel 8Ø85 microprocessor can directly address a maximum of only 65,536 addresses (a fraction of one frame) and the workstation can store up to 192 frames of data (approximately 63 million pixels), an indirect addressing scheme is required. A frame of image data is transmitted from the host computer to the workstation as 327,68Ø six-bit pixels. Each pixel is processed by the microprocessor compression algorithm (described in detail in the "12-Bit (Dual Channel) Colorizer-IDT RAM Version" section) into three-bit partitions. The three-bit partitions are stored in (and retrieved from) the DATARAM memory system.

A frame of graphics data is transmitted from the host computer as three-bit values for specified pixel addresses. A graphics frame may require only a few values, since only the foreground is transmitted. Note: the microprocessor <u>does not</u> compress the three-bit values.

The DATARAM BSA boards are each organized as 512K by 32-bit words plus seven bits of error correction code (ECC). The ECC allows the DATARAM memory system to correct internally any single-bit errors during retrieval and to detect multiple-bit errors. Since each of the three DATARAM memory systems can be populated with up to four BSA boards, each unit can store up to 2 million 32-bit words.

To summarize the data formats, the workstation communicates with the DATARAM Control Board in terms of "frames" and "partitions," while the DATARAM Control Board communicates with the memory in terms of direct addresses and 32-bit words.

In the functional description and theory of operation discussions that follow, only one third of the story is told. Unit Ø contains the graphic overlay data while units 1 and 2 contain the image data. The three units function in parallel. To simplify the discussion, only one of the units, representative of unit 1 or 2, is considered. This leaves the you with the responsibility to expand to three units the events described in one of the units, therefore understanding the system as it actually operates.

Figure 1 is a functional overview block diagram of the DATARAM Control board. The following are the three major functional sections in Figure 1:

- Data formatting
- Address Generation
- Control and Handshake

Data Formatting

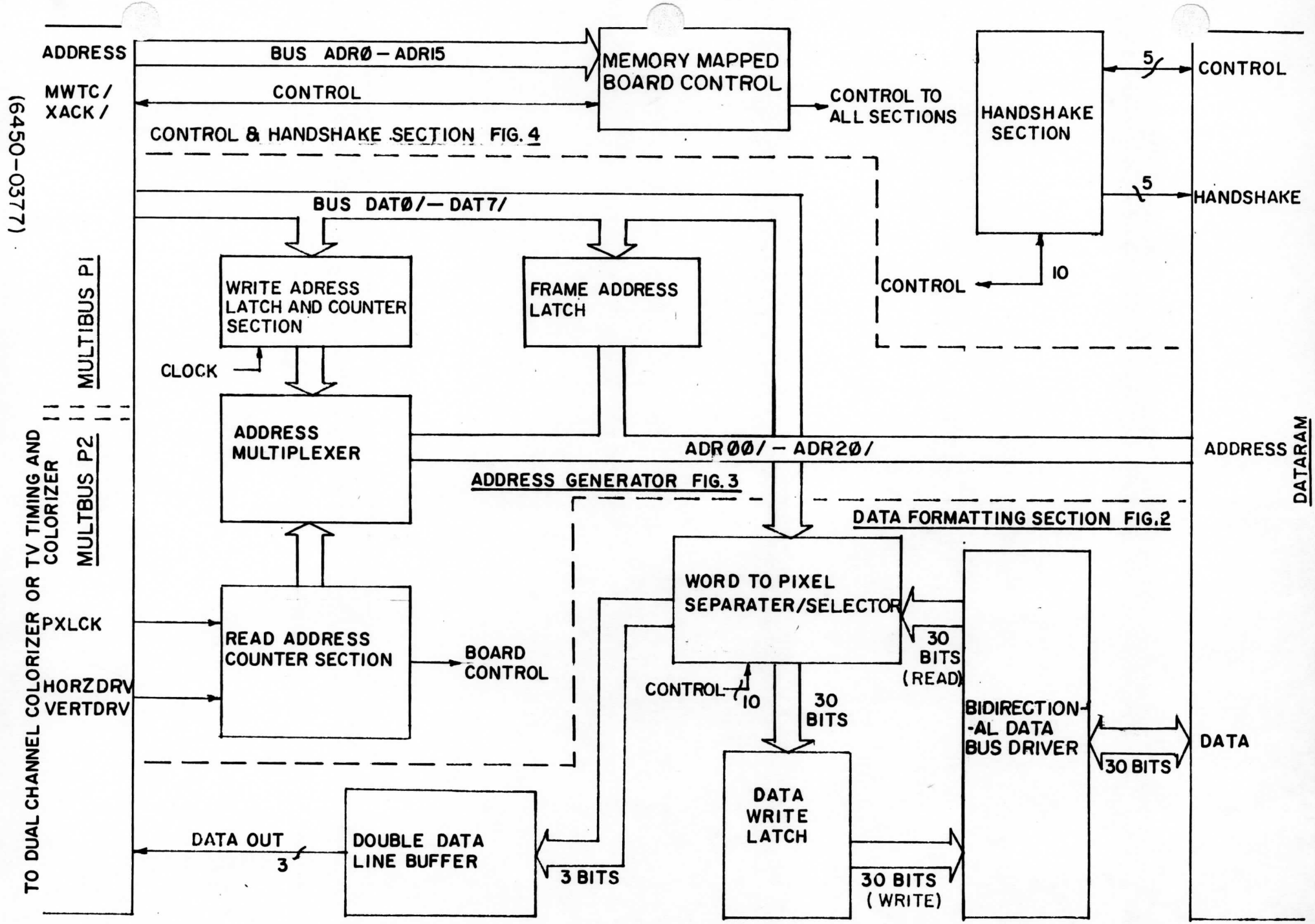
DATARAM manufactures two different word length memories, a 32-bit and a 36-bit version. Both versions use the same 36-bit bus structure. The 36-bit version uses all data bus lines (numbered ØØ-35) while the 32-bit version uses ØØ-15 and 18-33. In the McIDAS, only the 32-bit version is used, and ten 3-bit pixels are packed in each 32-bit word prior to storage. Two data bits are not used (numbers 32 and 33). Thus we use data bus lines ØØ-15 and 18-31. From here on, all reference to "word" means 3Ø bits.

The DATARAM system operates in several modes but only the following three are used in McIDAS:

- 3Ø-bit read
- 3Ø-bit write
- 3Ø-bit read/modify/write (R/M/W)

The 3Ø-bit read reads data, the 3Ø-bit write erases data and the R/M/W mode stores data.

In Figure 1, the Bidirectional Data Bus Driver separates the 3Ø-bit bidirectional data bus into a 3Ø-bit read bus and a 3Ø-bit write bus. The



DATARAM CONTROL
FUNCTIONAL OVERVIEW BLOCK DIAGRAM

FIGURE 1

3Ø bits of read data are unpacked by the Word-to-Pixel Separator/Selector into 1Ø three-bit pixel partitions and exported to the Double Data Line Buffer one pixel at a time. The Double Data Line Buffer consists of two RAM buffers which alternately read and write data. The buffers can store one horizontal line of data (64Ø three-bit pixel partitions). As one buffer is filled with data, the other is emptied. At the end of each horizontal scan, the buffers switch roles. The buffers are necessary because memory read, write and refresh cycles (dynamic RAMs) are multiplexed; by loading in an entire line under these conditions and unloading under control of pixel clock (PXLCK), the data read out flow is smooth and uninterrupted (synchronized to PXLCK). The data output from the buffer is output to the 12-Bit (Dual Channel) Colorizer-IDT RAM Version (image units only) or to the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree Unit (graphics unit).

The data storage cycle is quite different from the one just described for the read cycle. The data write cycle (R/M/W) consists of reading a 3Ø-bit word into the Word-to-Pixel Separator/Selector and modifying one partition with new write data. The modified word is latched by the Data Write Latch and written back into the same memory location as the original word. Thus, though the data is read in 1Ø-pixel groups, it is written one pixel at a time.

Address Generation

There are 483 visible lines in a 525-line TV frame. The remaining 42 lines are blanked by vertical blanking. Each horizontal line is blanked about 17% of the time by horizontal blanking, resulting in approximately 648 visible pixels (83% of 78Ø) per horizontal line. Because digital memories are addressed in binary, a block of memory must be set aside for each frame that is addressable in exact powers of two and is approximately the size of the visible image. If we pack 1Ø pixels per 3Ø-bit word, we need 64 words per 64Ø-pixel horizontal line. The number of horizontal lines with an exact power of two closest to 483 is 512 (only the first 483 lines are used). Thus, a frame allocation in memory consists of 512x64 words (32,768 words or 327,68Ø pixels). Because there are 512K words of storage on each BSA board, each board can store 16 frames. Each unit will store 16, 32, 48 or 64 frames, depending on the number of BSA boards in the chassis.

The Address Generation Section consists of a Read Address Counter, a Write Address Latch and Counter Section and a Frame Address Latch Section. A Frame read process consists of sequentially reading 32,768 words, starting at some particular address (frame number). As a result, the entire read sequence can be controlled automatically by a counter once the starting address and unit number are known. Thus, a read cycle is performed by addressing the proper unit (unit Ø, 1 or 2) and sending a 6-bit frame number (becomes upper six bits of the address to the DATARAM). The Write process is similar, but slightly more complicated. Here, counter address (Ø-32767) and pixel address (Ø-9) may be preloaded and the counter mode (increment/decrement and enable/disable) must be selected. The increased complexity and flexibility of the write address section is due primarily to the graphics write process requirements. Only the graphics data points are stored, not the background. Thus, a graphics frame may contain only a few scattered pixels whereas an image frame is made up of all pixels. (It is possible to load images into the graphics channel, but this is usually not done.)

Handshake Section

The MULTIBUS and DATARAM each have their own timing and control sections which would be incompatible without the Handshake Section. The data read, write, and R/M/W cycles are broken down into several subcycles. Only the DATARAM Control Board can initiate a cycle (or subcycle). However, once a cycle is initiated, sequencing to the next subcycle can be accomplished only after the DATARAM indicates that the current subcycle is completed. The received acknowledgement triggers the request for the next subcycle. This process continues until the cycle is completed. The Handshake Section forces both units into synchronism during cycle execution.

Board Control

There is considerable control logic on the DATARAM Control Board. While the source of some of the control logic is easily defined, some is obscure at discussion levels other than the Detailed Circuit Descriptions. In general, however, there are two major sources of board control: the Memory Mapped Board Control and the Read Address Counter Sections (see Figure 1). The former is a block used almost exclusively to control the

Address Generation section of Figure 1. Within the Read Address Section there are two counter units. One of the counters generates several control signals which either directly or indirectly control nearly all remaining blocks in Figure 1.

DETAILED FUNCTIONAL DESCRIPTION

DATA FORMATTING

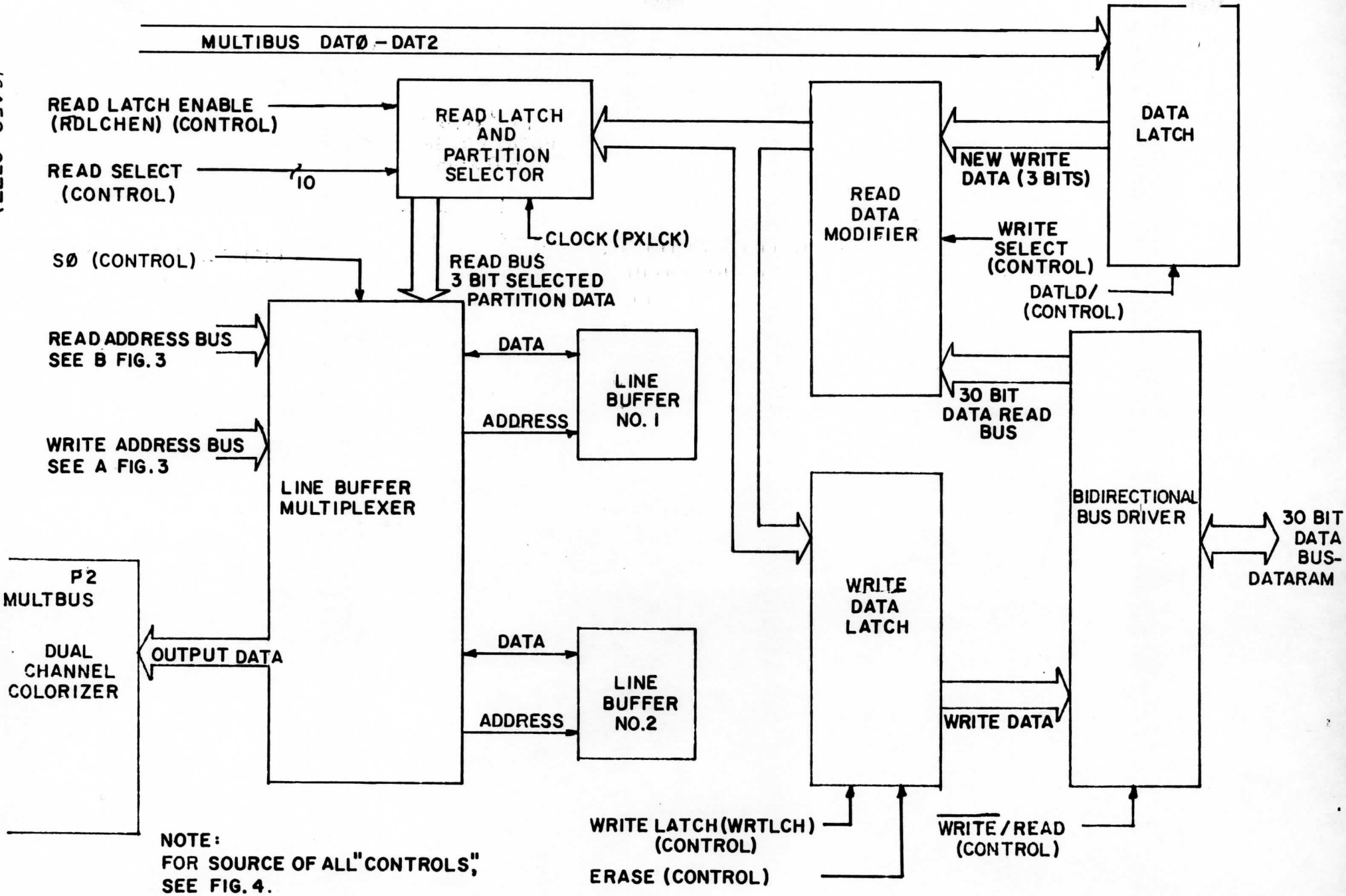
The Data Formatting section described in the Functional Overview is shown in Figure 2.

The Bidirectional Bus Driver is either in the input mode or the output mode, as determined by the control signal $\overline{\text{WRITE}}$/READ. When the control signal is high (read), the 3Ø-bit DATARAM Data Bus is connected to the Read Data Modifier. When the signal is low (write), the 3Ø-bit DATARAM Data Bus is connected to the 3Ø-bit Write Data Latch. During a read process, all Write Select lines going to the Read Data Modifier are inactive high. During this time, the Read Data Modifier passes the 3Ø-bit Data Read Bus to the Read Latch and Partition Separator.

A Read/Modify/Write cycle consists of a read portion followed by a write cycle. The read portion of the cycle is identical to the read cycle description above except a write data partition previously latched into the Data Latch is substituted for one of the read data partitions within the Read Modifier block. The partition to be substituted is determined by which Write Select line is active low. At this time, the output of the Read Modifier exactly matches the 3Ø-bit Data Read Bus input, with the exception of the substituted partition (27 old data bits and three new). While the modified word is present at the output of the Read Modifier, the Write Data Latch is strobed by bringing the Write Latch Control signal active low. When the Write portion of the R/M/W cycle is executed, the output of the Write Data Latch is connected to the 3Ø-bit DATARAM Data Bus by bringing $\overline{\text{WRITE}}$/READ low.

The ERASE/ control is used in the 3Ø-bit write mode only and is used to erase graphics frames. It causes the Write Data Latch to inject all zeros when it is active low, thereby clearing 1Ø pixels per cycle.

Read data, presented to the Read Latch and Partition Separator, is latched by bringing the Read Latch Enable signal active low. Then, each



DATA FORMATTING SECTION
FUNCTIONAL BLOCK DIAGRAM
FIG. 2

(6450-0377)

partition is sequentially gated onto the Read Bus by enabling its associated Read Select line. The Read Bus data is sent to the Line Buffer Section. The need for the Line Buffer is explained in the next paragraph.

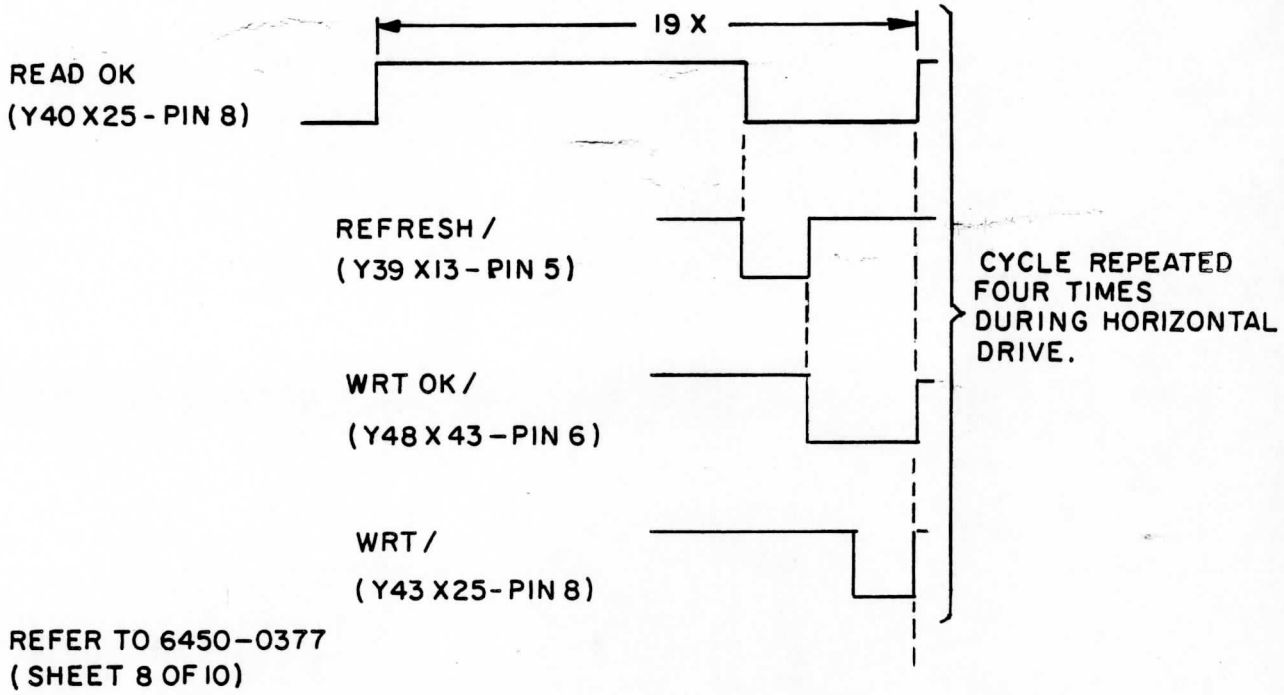
The relationship between horizontal drive time and pixels is established in the 60/50 Hz TV Timing and Colorizer-Brooktree board at 780 pixels per horizontal drive period. The DATARAM Control Board establishes the number of data pixels per horizontal line at 640, leaving 140 pixels as non-data pixels. The 640 data pixels are contained in 64 words. The words must be read and disassembled into pixel partitions during each horizontal period. In addition to reading data from memory, two other processes, memory refresh and data writes (an R/M/W cycle), must be performed periodically.

The DATARAM memory requires a refresh cycle approximately every 14 µsec (one-fourth of a horizontal drive period). The DATARAM chassis are supplied to SSEC with a modification which allows the refresh cycle to be controlled externally, from the BSC board. This enables the DATARAM Control board to determine when a refresh cycle will occur.

A refresh and a R/M/W cycle require about 10 and 20 pixel periods respectively. Therefore, we can break a horizontal period (63.49 µsec) into four repeating cycles, consisting of 16 data reads (160 pixels) one refresh (10 pixels) and a R/M/W cycle (20 pixels). The fourth cycle has 20 extra pixels, resulting in 780 pixels/horizontal period. Note: if no memory write request is made, a R/M/W cycle simply is not executed, though the time is set aside for it. The timing diagram below should help to summarize the three cycle time relationships.

If a pixel period is 81.4 nsec, then 1Ø pixels = .814 µsec. Let x be defined as 1Ø pixels = .814 µsec = one word time.

(READ 16 WORDS)
READ OK HI FOR 16X = 13.024 usec.
REFRESH/ LO FOR 1X = .814 usec.
WRT OK/ LO FOR 2X = 1.628 usec.
WRT/ LO FOR 1X = .814 usec.



REFER TO 6450-0377
(SHEET 8 OF 10)

If the Read Bus Data was output directly to the 12-Bit (Dual Channel) Colorizer-IDT RAM Version, there would be four vertical black bars on the screen. By writing the four groups of 16 words each into a buffer, and then reading them out under control of pixel clock, the data is fully synchronized and smooth flowing. To perform this function, two buffers are required. While one buffer is in a write mode the other is in a read mode. At the end of each horizontal line, the buffers swap modes. Each of the buffers are static RAMS organized as 4-bit by 1Ø24-bit. Only three bits are used and only the first 64Ø cells are used. These RAMS have a bidirectional data port. Therefore, the data input/outputs, as well as the address sources must be switched. For example, if Line Buffer #2 is addressed by the Write Address Bus and is receiving input data from the Read Bus, then Line Buffer #1 is addressed by the Read Address bus and is outputting data to the 12-Bit (Dual Channel) Colorizer-IDT RAM Version (or 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree if this is the graphics unit).

DATARAM ADDRESS

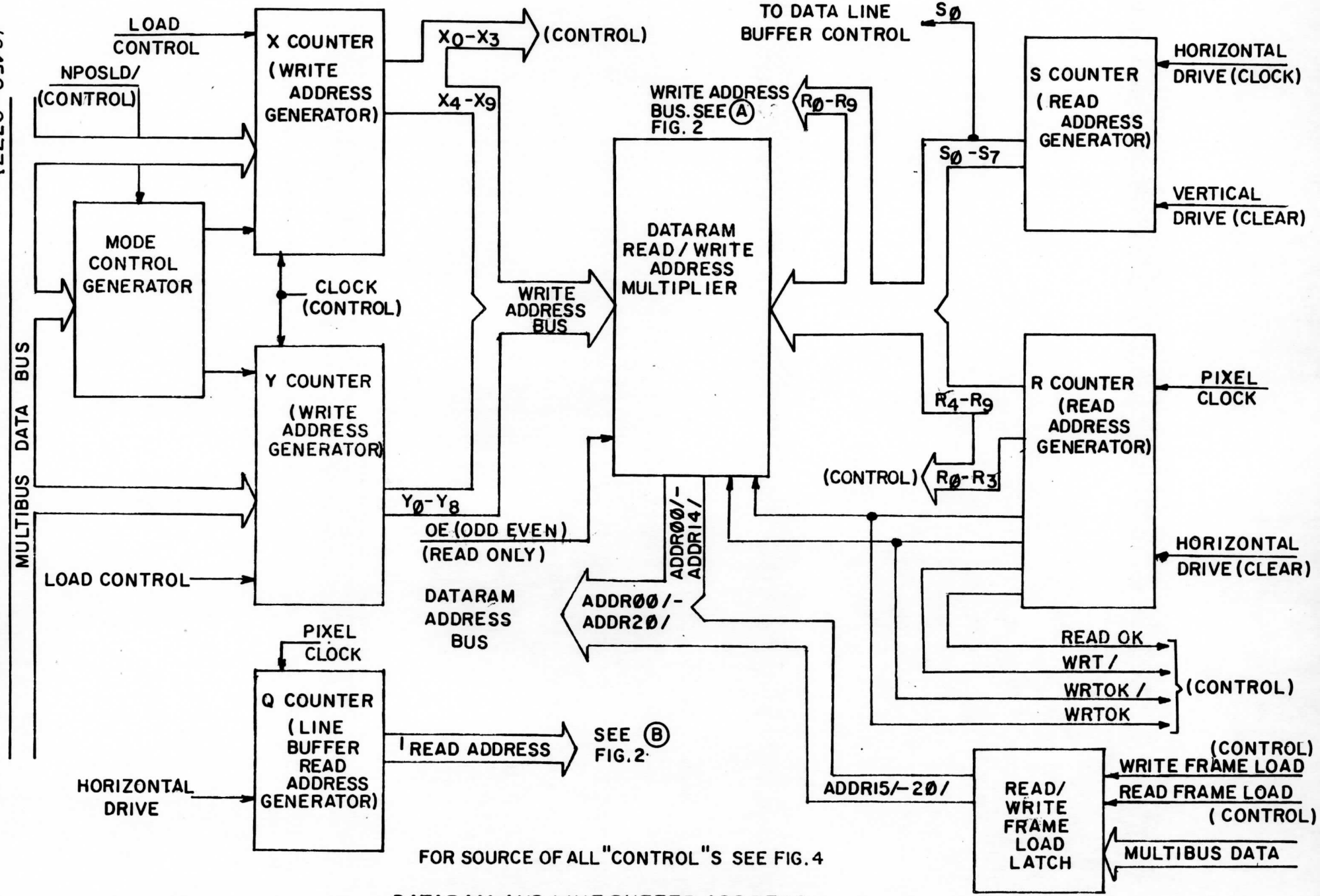
Figure 3 is a function block diagram of the DATARAM address bus generator. While the 21-bit address bus within the DATARAM is common to both the read and write functions, two separate address generation sources are required because of the different read and write functional requirements. The write address generator must be presettable to any pixel address prior to the storage of each pixel, while the read address generator simply needs to be incremented each time a word is read from the DATARAM.

Two counters, X and Y, make up the lower 15 bits of the write address; the S counter, R counter, and OE (odd/even signal from the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board) make up the lower 15 bits of the read address. The OE signal is used for interlacing the video images during the read process and will be discussed in the Detailed Circuit Description Section.

The Y counter is a nine-stage presettable Up/Down binary counter. The X counter, a 1Ø-stage counter, is similar to the Y counter except that the least significant four bits function as a BCD (binary-coded decimal) counter. The BCD portion of the X counter is used only to form the "Write Select" control signals shown in Figure 2. Both counters are clocked by a common clock generated in the Control Section. The clock is pulsed low each time a data write to the DATARAM is completed. If the X counter is in a count up mode, 1Ø clock pulses are required for each increment of the non-BCD portion of the counter (X_4-X_9). If the Y counter is inhibited while X is in a count up mode, 1Ø data writes to each address occur. This is exactly what occurs during an image storage process. Since only one pixel partition at a time is written to memory, 1Ø data R/M/W cycles are required to write 1Ø partitions (one complete word). X_0-X_3 select the pixel to be written into.

The non-BCD portion of the X counter acts as a six-stage binary word counter. The six stages have a full count of 64, the number of words in a horizontal line. During an image load process, the Y counter is allowed to increment on every 64Øth pixel. Thus, the Y counter is a line address generator.

Both X and Y counters are fully programmable. They can count in either direction or be inhibited; they can be preloaded with any count



DATARAM AND LINE BUFFER ADDRESS GENERATOR SECTION

FIGURE 3

from zero to their maximum count. The memory mapped Mode Control Generator is the source of all X and Y counter mode controls. The Mode Control Generator consists of a PROM whose address inputs are driven by latched MULTIBUS data lines. The latch is enabled by the control signal NPOSLD (Next Position Load). A single eight-bit MULTIBUS data byte, latched by NPOSLD/, controls the modes of both counters. The counters are preloaded with data from the MULTIBUS data bus under the control of signals from the Control Section (memory mapped also).

The R and S counters function as the Read Address Generator. The R and S counters are very similar in function to X and Y respectively. Instead of preset inputs, both the R and S counters have a "clear" input. Since the R counter is the word counter, it is cleared at the beginning of each horizontal scan line and is clocked by pixel clock. Because the only inputs to the R counter are pixel clock and horizontal drive, the counter is always active and always counts up. It is, therefore, an ideal section for generation of all basic sub-line control signals. The following four control signal outputs from the R counter are used by the Control section to produce read/write cycle control as well as refresh gating:

- READOK
- WRT/
- WRTOK
- WRTOK/

The RØ-R3 outputs are used to generate Read Select signals (see Figure 2) while all 1Ø R outputs are used as Line Buffer load addresses (see Figure 2) and inputs to the DATARAM Read/Write Address Multiplexer. The S counter is a line counter, clocked by horizontal drive and cleared at the beginning of each vertical field by vertical drive. The least significant bit from the S counter (SØ) toggles to the opposite state with each input of the clock (horizontal drive). SØ toggles the Line Buffer Multiplexer (see Figure 2).

The DATARAM Read/Write Address Multiplexer selects either the 15 write address inputs or the 14 read address inputs and OE as a function of control signals WRTOK and WRTOK/.

The upper six bits of the DATARAM address bus are provided by the Read/Write Frame Load Latch. The Read and Write Frame Load control signals are used as latching signals by the Read/Write Frame Load Latch section. The address to be latched is supplied by the data bus.

The Q Counter (Figure 3) generates the Line Buffer unload (read) addresses. The only inputs to the counter are a horizontal drive (resets counter) signal and pixel clock. There are a total of 78Ø pixels/horizontal period but only 64Ø are stored and retrieved. Therefore, the 64Ø-pixel field should be centered on the display. To achieve this, the Q counter has an internal programmable delay which may be programmed to position the image as desired.

CONTROL AND HANDSHAKE

Figure 4 is a Functional block diagram of the Control and Handshake Section.

CONTROL

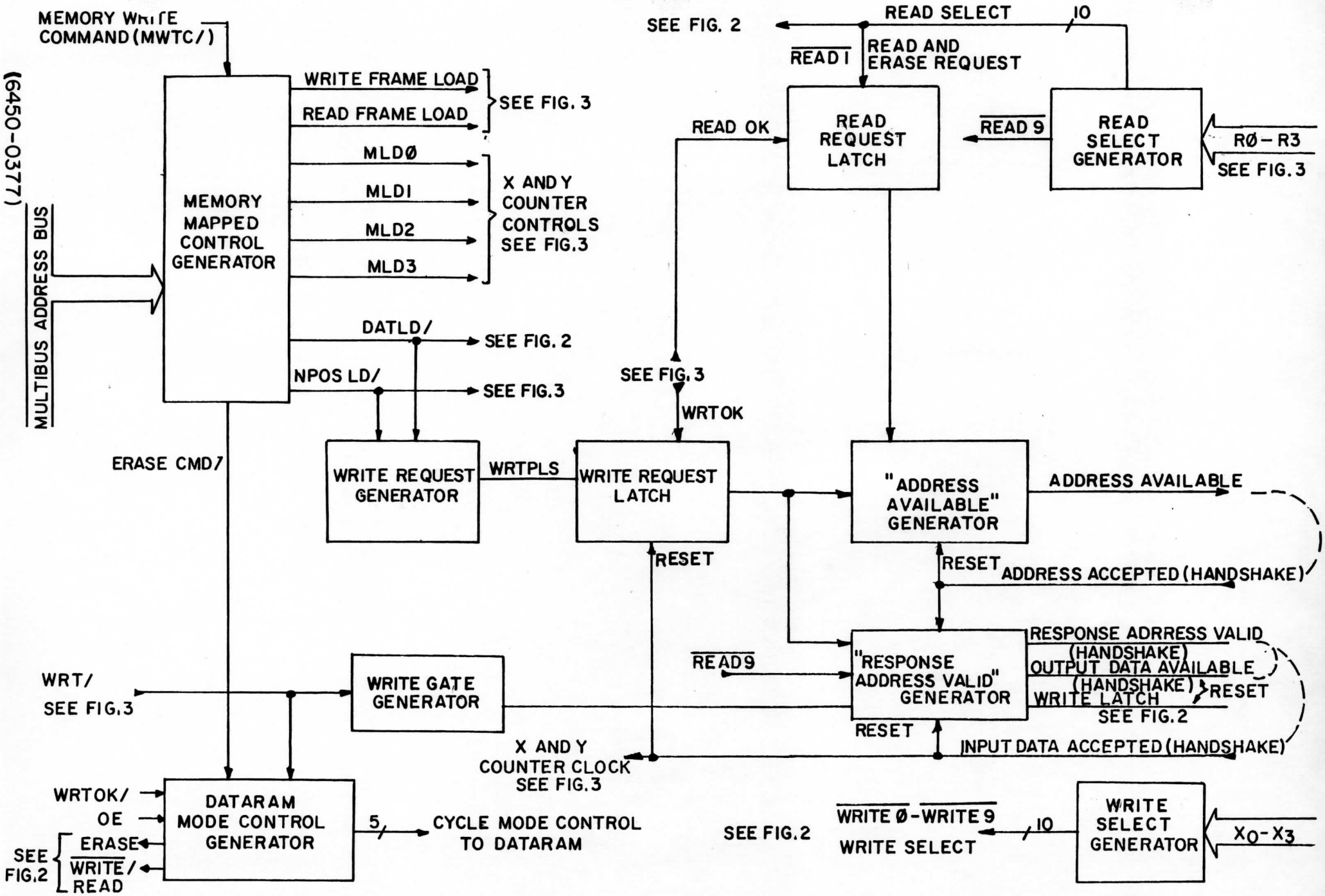
Memory-Mapped Control Generator

The Memory-Mapped Control Generator consists of two PROMS, driven by the entire MULTIBUS address bus. This section also contains a programming carrier which encodes the unit number (unit Ø, 1, or 2). This section produces nine memory-mapped output signals. Signals MLODØ - MLD3 preload the X and Y counters. The Read and Write Frame Load commands are latch enables for latching the frame address (see Figure 3). Signal DATLD/ (Data Load) latches new pixel partition data into the Data Latch (see Figure 2). Signal NPOSLD/ (Next Position Load-active low) activates the X and Y counter memory-mapped Mode Control Generator. Signal ERASE CMD/ (Erase Command) is an input to the DATARAM Mode Control Generator. This signal initiates a frame erase cycle.

DATARAM Mode Control Generator

The DATARAM has several modes of operation. A 32-bit unit can do 16-bit as well as 32-bit data reads, writes, or data read/modify/writes (R/M/W). A total of five cycle mode control signals determine the mode of operation. Four of these lines are driven physically from the same source on the SSEC DATARAM CONTROL board, thus limiting the number of modes used to the following three:

- 32-bit data read (we use only 3Ø bits)
- 32-bit R/M/W
- 32-bit write (erase only)



CONTROL AND HANDSHAKE SECTION - FIGURE 4

The OE signal is used as a clock by the generator to synchronously gate an ERASE CMD/ signal. This causes an erase process to begin only in synchronism with the beginning of a frame field. When the generator is in the erase mode, it effectively replaces the 3Ø-bit data read cycles with 3Ø-bit erase write cycles. Thus 64 words (64Ø pixels) are cleared during each horizontal drive period. This allows an entire frame to be cleared in a single frame period (.033 sec). The $\overline{\text{WRITE}}$/READ signal controls the Bidirectional Bus Driver (see Figure 2). When $\overline{\text{WRITE}}$/READ is high, the driver is in the read mode.

Write Select Generator

The Write Select Generator decodes the BCD inputs ($X_Ø$-X_3) into ten Write Select lines. Each line controls a pixel partition in the Write Data Selector (see Figure 2).

Read Select Generator

The Read Select Generator operation is identical to the Write Select Generator. Because the Read Select Generator is always running, it is a convenient source of cyclic timing waveforms. For example, READ9/ is used by the Response Address Valid Generator and READ1/ is used by the Read Request Latch. Primarily, the Read Select Generator Signals (READØ/ - READ9/) gate the read data pixel partitions onto the Read Bus (see Figure 2).

HANDSHAKE

All remaining blocks in Figure 4 constitute the MULTIBUS side of the handshake system. As explained earlier, the DATARAM Mode Control Generator establishes the mode of operation (read, write or R/M/W) and must be set up before a read, write or R/M/W cycle.

Address Available Generator

All cycles begin by generating the handshake signal ADRAVN (Address Available). The Address Available Generator produces this signal when triggered by the Read Request Latch during read cycles or the Write Request Latch during Write and R/M/W cycles.

Read Request Latch

The output of the Read Request Latch initiates read cycles. Control signal READOK gates request signal READ1/ into the latch.

Write Request Generator

When writing pixels into an image frame, the last setup operation performed is latching the pixel partition data into the Data Latch (see Figure 2). DATLD/ is the latching signal and is also an input to the Write Request Generator. Thus, the action of latching the partition data also prompts a Write Request. When writing pixels to a graphics frame, the Next Position Load (NPOSLD/) command is normally the last setup operation and also initiates a Write Request.

Write Request Latch

The Write Request Latch latches the request signal from the Write Request Generator and prompts the Address Available Generator at the proper time (determined by signal WRTOK).

Response Address Valid Generator

After the ADRAVN signal is initiated by the Read or Write Request Latches, the signal remains on until turned off by the "Address Accepted" (ADRACN) response (a few nanoseconds). This response also initiates the beginning of the next handshake signal "Response Address Valid" (RADVLDN).

RADVLDN is poorly named; it plays varying roles as a function of the mode. During a data read or R/M/W mode, the signal informs the DATARAM that the MULTIBUS is ready to accept the requested input data. During a data write mode, the signal informs the DATARAM that the data on the 3Ø-bit data bus is valid. During an R/M/W cycle, "Response Address Valid" must go true twice. The first time is for the read portion of the cycle and operates as explained above; the second time is for the write portion of the cycle. In all cycles, the DATARAM responds within a few nanoseconds with either an "Output Data Available" (read or read portion of R/M/W cycle) or "Input Data Accepted" (write or write portion of an R/M/W cycle). Either of these signals resets the Response Address Valid Generator. For read or write cycles, this is the final handshake action. For R/M/W cycles however, a write cycle must be completed. To complete the

write cycle, another "Response Address Valid" command must be issued to inform the DATARAM that the "Write" data is ready (valid). When an R/M/W or Write cycle is initiated, the output of the Write Request Latch is passed to the Response Address Valid Generator. This signal functions as an "arming" signal which re-triggers the Response Address Valid Generator during the write portion of an R/M/W cycle. "Output Data Available" (normally a read cycle response) can go true during a requested write cycle only if the requested cycle is an R/M/W cycle at the end of its read portion. This signal is combined with the output of the Write Gate Generator to produce an "arming" signal gate; this re-triggers the Response Address Valid Generator for the Write portion of the R/M/W cycle. The DATARAM responds with "Input Data Accepted," used to reset the Write handshake logic and trigger the X and Y counters (write address counters - see Figure 3).

DETAILED CIRCUIT DESCRIPTION

The schematic diagrams of the DATARAM Control Board are shown on SSEC drawing #645Ø-Ø377 (Modification F, dated 4/23/84) sheets 1-1Ø. The schematic circuit analysis is accomplished by analyzing groups of components which represent single blocks on the respective functional block diagrams.

The SSEC circuit schematics are labelled by the column and row in which pin #1 of that chip resides. This is very helpful for troubleshooting, since the symbol ID is also the chip location; however, IC gates, flips-flops, buffers and inverters usually have several identical logic circuits packaged on the same IC. Therefore, when reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and a section identification letter. The symbol ID number alone is used to refer to single function ICs.

DATA FORMATTING

Refer to Figure 2 for the Functional block diagram of the Data Formatting Section. Most of the circuitry for this section is contained in sheets 1-4 of the schematics.

Bidirectional Bus Driver

The Bidirectional Bus Driver is made up of 1Ø Intel 8216 bidirectional bus driver chips. The 1Ø ICs which constitute the driver are: Y3ØX8, Y27X8, Y24X8, Y21X8, Y18X8, Y15X8, Y12X8, Y9X8, Y6X8 and Y3X8. The first four are located on sheet 1, the second four on sheet 2 and the last two are on sheet 3.

Each chip is capable of handling four bits but only three (bits Ø, 1, and 2) bits on each chip are used. Therefore, each chip handles one pixel partition. The control signal $\overline{\text{WRITE}}$/READ is paralleled to pin 15 (DIEN - Data In Enable) of each chip. When pin 15 is low (write), pins 4, 7, and 9 are connected to bidirectional bus pins 3, 6, and 1Ø respectively. When pin 15 is high (read), bidirectional bus pins 3, 6, and 1Ø are connected to pins 2, 5, and 11 respectively. For detailed information about the control signal, consult the Handshake and Control Section.

Read Data Modifier

The Read Data Modifier (see Figure 2) comprises ten 74LS157 data selector/multiplexer chips. The 1Ø ICs which make up this block are Y3ØX17, Y27X17, Y24X17, Y21X17, Y18X17, Y15X17, Y12X17, Y9X17, Y6X17 and Y3X17.

These ICs are distributed identically to those of the Bidirectional Bus Driver. Each of these chips have two 4-bit data sources and one 4-bit data output. Like the bus driver, only three bits are used and represent a pixel partition. Selection of the data source (A or B) to be channeled to the output (Y) is determined by the control signal applied to pin 1 of each chip. Data input signals (ØDATA, 1DATA, and 2DATA) are applied to the A input (pins 2, 5, and 11 respectively) of all 1Ø chips. The B input (pins 3, 6, and 1Ø) of each chip is driven by the Data Output Lines ($DO_Ø$, DO_1, and DO_2 respectively) of a corresponding bus driver chip. Thus, the B input of each 74LS157 is driven by a read pixel and the A input is driven by new data. A separate control line (WRITEØ/ - WRITE9/) drives each chip. For more information on the control lines, consult the Handshake and Control section. At present, it is sufficient to know that only one control line can be active low at one time. Therefore, if WRITE1/ goes low while a 3Ø-bit word is read in, the latched data (ØDATA - 2DATA) replaces the second pixel partition. At this time, pixels Ø and

one, and 3-9 pass from the respective Bidirectional Bus Driver chip to the Y output of the respective Write Data Selector chip. The latched input data appears at the Y output of Y27X17 only. The process just described happens in the Read/Modify portion of the Read/Modify/Write Cycle. During a read cycle, none of the Write Select Lines are allowed to go low, thereby passing all 1Ø partitions on to the Partition Read Latch and Selector block unmodified.

Write Data Latch

The output of the Read Data Modifier is presented to both the Write Data Latch (used in Write or R/M/W modes) and the Read Latch and Partition Separator blocks of Figure 2.

The Write Data Latch consists of five 8-bit latch chips (74LS273) located at Y15X37 (pixels Ø and 2), Y12X37 (pixels 1 and 3), Y9X37 (pixels 4 and 6), Y6X37 (pixels 5 and 7), and Y3X37 (pixels 8 and 9). The first two chips are located on sheet 1, the second two chips are on sheet 2 and the last chip is on sheet 3. The chips are clocked by control signal WRTLCH (Write Latch). These chips latch on the positive-going edge of the clock, while the data is present at the output of the Read Data Modifier. During a write cycle or the write portion of an R/M/W cycle, Bidirectional Bus Driver control signal $\overline{\text{WRITE}}$/READ goes low one pixel clock time after WRTLCH latches the data, gating the Write data onto the 3Ø-bit DATARAM bidirectional data bus. Note that all latch chips have the control signal ERASE/ applied to the clear inputs. Regardless of the input data, if ERASE/ is low, the latch outputs are all binary zeros. For more information on WRTLCH and ERASE, consult the Handshake and Control Section.

Read Latch and Partition Separator

The Read Latch and Partition Separator block of Figure 2 consists of ten 4-bit tri-state D-type register chips located at Y3ØX26, Y27X26, Y24X26, Y21X26, Y18X26, Y15X26, Y12X26, Y9X26, Y6X26, and Y3X26. These chips are distributed on sheets 1-3 in a manner identical to the Bidirectional Bus Driver and Read Data Modifier blocks, and are associated with pixels Ø-9 respectively. The tri-state control for these chips is pins 1 and 2. When both (or either) pins are high, the output is in a high impedance state, though input data can still be loaded and latched. The

output of each chip is connected to a common three-bit (pixel partition) Read Bus. Ten #3 pins, one from each of ten chips, are connected to form ØVID. Pins 4 and 5 do the same for 1VID and 2VID respectively. The 3Ø-bit word is parallel-loaded into the Read Latch and Partition Separator on the first rising edge of PXLCK, following an active low at the latch enable pin (pin 9). RDLCHEN/ (Read Latch Enable - active low) is parallel-connected to all 1Ø chips and is described in detail in the Handshake and Control section. As soon as the data is latched, any pixel can be output to the Read Bus by bringing that pixel's tri-state control pins (pins 1 and 2) low. Pins 1 and 2 of all 1Ø chips are driven by READØ/ - READ9/; they enable pixel partitions Ø-9 respectively. For more information on READØ/ - READ9/, see the Handshake and Control Section.

Data Latch

Input write data is supplied to the input Data Latch via the MULTIBUS data bus bits DATØ - DAT2. The Data Latch is a single 74LS174, shown at the bottom of sheet 6 of the schematics. The latch is enabled by the memory-mapped control signal DATLD/. The output of the latch, ØDATA - 2DATA, is paralleled to the A input of the 1Ø Read Data Modifier chips.

Line Buffer Multiplexer

The Line Buffer Multiplexer, and Multiplexer Control sections are shown on sheet 4 of the schematic.

The Line Buffer Multiplexer performs two major tasks. First, it channels Read Bus data to the Write Buffer (off-line buffer) and channels the Read Buffer (on-line buffer) data to the output. Second, it connects the R counter outputs to the address inputs of the off-line buffer and connects the Q counter outputs to the address inputs of the on-line buffer. At the end of each horizontal line, the multiplexer must exchange the on-line and off-line buffers.

The output of NAND gates Y45X41-A and -B provides the control signals for the multiplexer. The NAND gates combine PXLCK, READOK, SØ, and SØ/ to produce WE1/ and WE2/. Note that PXLCK and READOK go to both NAND gates and that SØ/ goes to the A NAND gate while its complement (SØ/) goes to the B NAND gate. SØ is the LSB output of a horizontal line counter and therefore toggles to its opposite state at the beginning of each horizontal

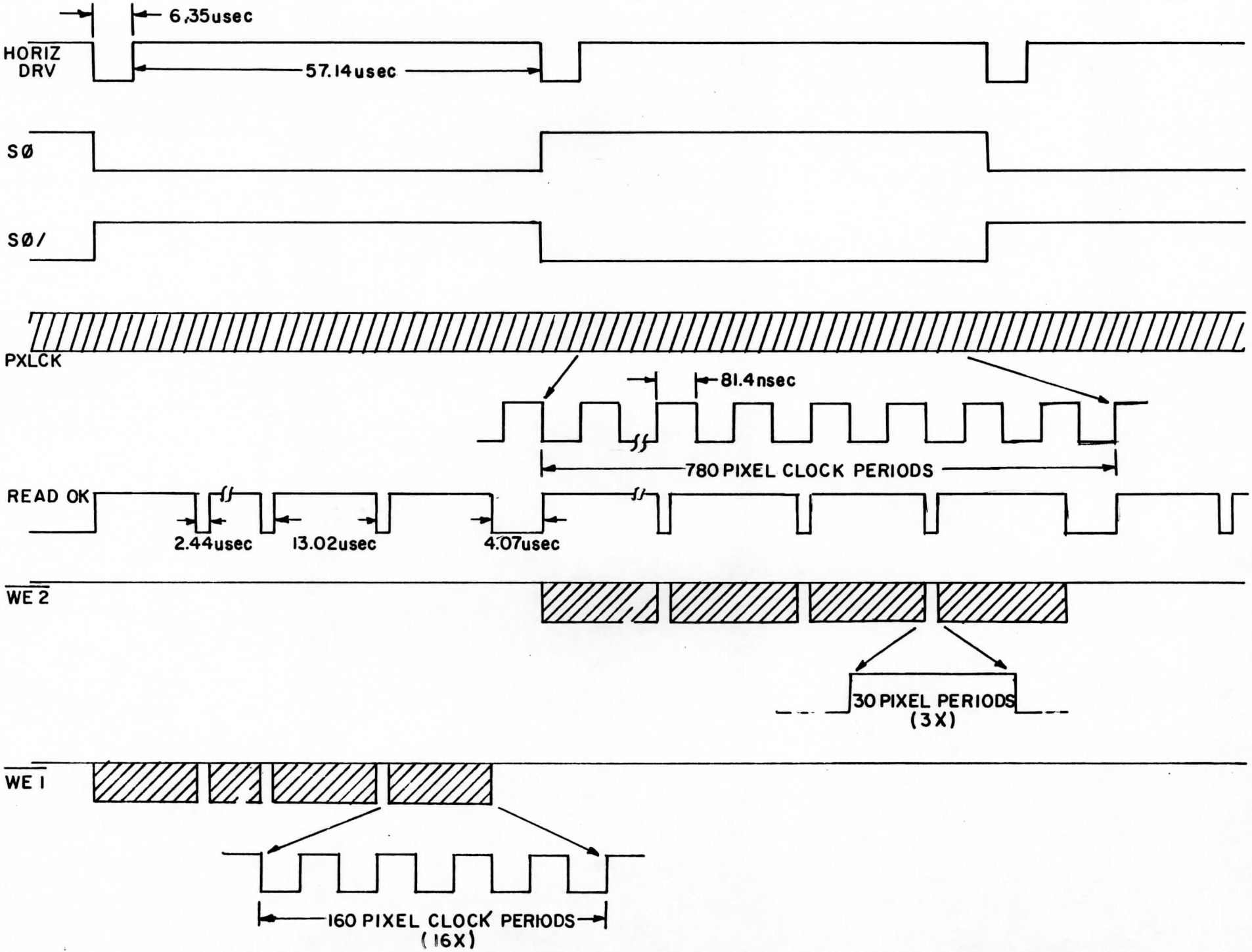
scan. Timing Diagram 1 shows the outputs of the NAND gates. The result of combining these waveforms is a gated pixel clock (PXLCK) which occurs only during read time. The gate that has a logic low at its SØ or SØ/ input has a steady high output while the other gate produces the READOK gated and inverted PXLCK. Signals WE1/, WE2/, SØ, and WE2 constitute the Buffer Multiplexer Control signals shown in Figure 2.

The Line Buffer Multiplexer shown in Figure 2 consists of tri-state octal buffer Y33X38, quad 2 input multiplexer Y39X37, and five quad 2 input data selectors Y3ØX37, Y27X37, Y24X37, Y21X37, and Y18X37. The Line Buffer consists of RAM chips Y33X38 and Y36X38.

The five data selectors function as the address switches for the buffer RAMS. The "load" addresses (RØ - R9) are applied to the A inputs of the selectors, which drive Y36X38, while the "unload" addresses ($Q_Ø$ - Q_9) are applied to the B inputs. The same signals are applied to the opposite inputs of those selectors which drive Y33X38. Since all selector chips are switched by SØ, one buffer is driven by R signals while the other is driven by Q signals. When SØ is low, the A inputs drive the corresponding buffer.

Refer to Timing Diagram 1. Pin 1Ø, the active low write enable input of the buffer RAMS, is driven by WE_1/ on RAM chip Y36X38 and by WE_2/ on RAM chip Y33X38. Note that WE_1/ is active when SØ is low. Thus, Y36X38 is in the Write mode (load) while the A inputs (RØ - R9) are driving the address lines. At the same time, Y33X38 is in the read mode and its address lines are driven by the $Q_Ø$ - Q_9 signals. When SØ goes high, the opposite signals drive the respective buffer address inputs and the buffers swap read/write modes.

Tri-state octal buffer Y33X38 functions as the "write" data switch while the quad 2 input multiplexer (Y39X37) functions as the "read" data switch. Y33X28 is organized as two quad buffer sets, each having a separate tri-state enable input. The multiplexer (Y39X37) uses SØ/ as the word select input. When SØ/ is low, A_1 - C_1 are gated to the output (Q_A - Q_C). When SØ/ is high, A_2 - C_2 are gated to the output. In summary, if SØ/ is low, WE_1/ is active, WE_2 is inactive low, RAM Y36X38 is in the "load" mode, RAM Y33X38 is in the unload mode, ØVID - 2VID are directed to RAM Y36X38, and RAM Y33X38 read data is selected by the multiplexer. Conversely, if SØ/ is high, input data (load) is directed to Y33X38 and "unload" (read) data from Y36X38 is selected by the multiplexer.



TIMING DIAGRAM 1 - LINE BUFFER MULTIPLEXER CONTROL
(6450-0337)

DATARAM ADDRESS AND LINE BUFFER ADDRESS GENERATOR

Refer to Figure 3 for the functional block diagram of the DATARAM and Line Buffer Address Generator sections. Most of the circuitry for this section is contained on sheets 5, 6, and 8 of the schematic diagrams.

DATARAM Write Address Generation Section

The circuitry for this section is shown on sheet 6 of the schematic. The 15 LSBs of the DATARAM write address are generated by the X and Y counters.

Y Counter Section

The Y Counter consists of three cascaded binary counters: Y72X39, Y69X39 and Y66X39. These 74LS191 counters are fully-programmable synchronous binary up/down counters featuring an asynchronous load. The data inputs to the counter are supplied by the MULTIBUS data bus. Control signal MLD2/ is the pre-load strobe for Y72X39 and Y69X39 while MLD3/ serves the same purpose for Y66X39. Clock signal XYINC/ (XY Increment) is applied to all X and Y counter chips. These control and clock signals are covered in the Control Section. Mode control signal YDU (Y Down/Up) controls the direction of counting (incrementing or decrementing). Mode control signal YEN/ (Y Enable) enables (active low) or disables counting. YEN and YDU controls are generated by the Memory Mapped Control Generator (see Figure 4) located in the Control Section.

X Counter Section

The X Counter is similar to the Y Counter with the exception of the least significant counter chip and the data pre-loading scheme. The counter consists of Y72X48, Y69X48 and Y66X48. Y72X48, the least significant counter chip, is a BCD counter chip while the other two are binary counters. The ripple carry output from the BDC counter is used as the input to an eight-stage binary counter consisting of Y69X48 and Y66X48.

Since the overall counter counts in a combination of BCD and binary, preloading would be complicated (for programming) unless a binary-to-BCD/binary converter is incorporated. The converter consists of EPROM Y37X12 and latches Y6ØX32 and Y6ØX21. Control signal MLDØ, the latching signal for Y6ØX32 latches the eight least significant pre-load bits while MLD1/ pre-loads the two MSBs (Y6ØX21). The inputs to the latches are

supplied by the buffered MULTIBUS data bus. The latched data, along with MLD2/ are used as address inputs to the EPROM. The EPROM, a 2716, functions as a look-up table. When MLD2/ is inactive high, the EPROM is switched to its BCD decode section and the four LSB output bits represent the BCD portion of the pre-load term. At this time, MLD3/ is brought active low, latching the BCD pre-load data into Y72X48. Next, the pre-load control (MLD2/) for the binary portion of the counter is brought low (MLD3/ returns to inactive high). The MSB address input to the EPROM is low, switching it to the binary decode section. The eight EPROM output bits now contain the pre-load data for the binary portion of the counter. Note that MLD2/ acts as both the EPROM MSB input and the pre-load control for the binary portion of the counter. Mode control signals XEN/ and XDU are generated by the Mode Control Generator which also generates the Y Counter mode controls. The X and Y counters use the same clock (XYINCR/). As explained in the Functional Description Section, data is written into memory in the R/M/W mode of the DATARAM, one pixel partition (three bits) at a time. X Counter output bits XØ-X3 (BCD portion) are used as the pixel partition address since 1Ø pixel partitions reside at each word address. This is the reason for a BCD counter chip in the X Counter. X Counter output bits X4-X9 form the five LSBs of the word address (Ø-63). Therefore, the X Counter provides the addressing of any pixel on a 64Ø pixel horizontal line. The nine-bit Y address generator output (YØ-Y8) allows a full count of 512, the number of horizontal lines in a frame. Thus, the Y Counter addresses the horizontal line.

Mode Control Generator

The Mode Control Generator consists of data latch Y65X3Ø and PROM Y63X48. The latch is driven by DATØ-DAT2, the three LSBs of the buffered MULTIBUS data bus. The latch is controlled by control signal NPOSLD/, generated by the Memory Mapped Control Generator, located in the Control Section. The four PROM outputs are used as mode (up/down) and enable control signals for both counters. The table below shows the inputs, outputs, and meanings of the PROM.

Data Input (binary)	Data Output (binary)	Results
ØØØ	1ØØØ	Y disabled, X counts up
ØØ1	1ØØ1	Y disabled, X counts down
Ø1Ø	Ø1ØØ	Y counts up, X disabled
Ø11	Ø11Ø	Y counts down, X disabled
1ØØ	ØØØØ	both count up
1Ø1	ØØØ1	X counts down, Y counts up
11Ø	ØØ1Ø	X counts up, Y counts down
111	ØØ11	both count down

If the CPU is directed, under firmware control, to write a zero to the address assigned to NPOSLD/, the Y Counter is disabled and the X Counter is in a count-up mode. Until changed by a new mode command, the X counter increments each time an active low clock pulse (XYINCR/) is received.

DATARAM Read Address Generation Section

The circuitry for this section is shown on sheet 8 of the schematic. The 15 LSBs of the DATARAM read address are generated by the R and S Counter.

R Counter Section

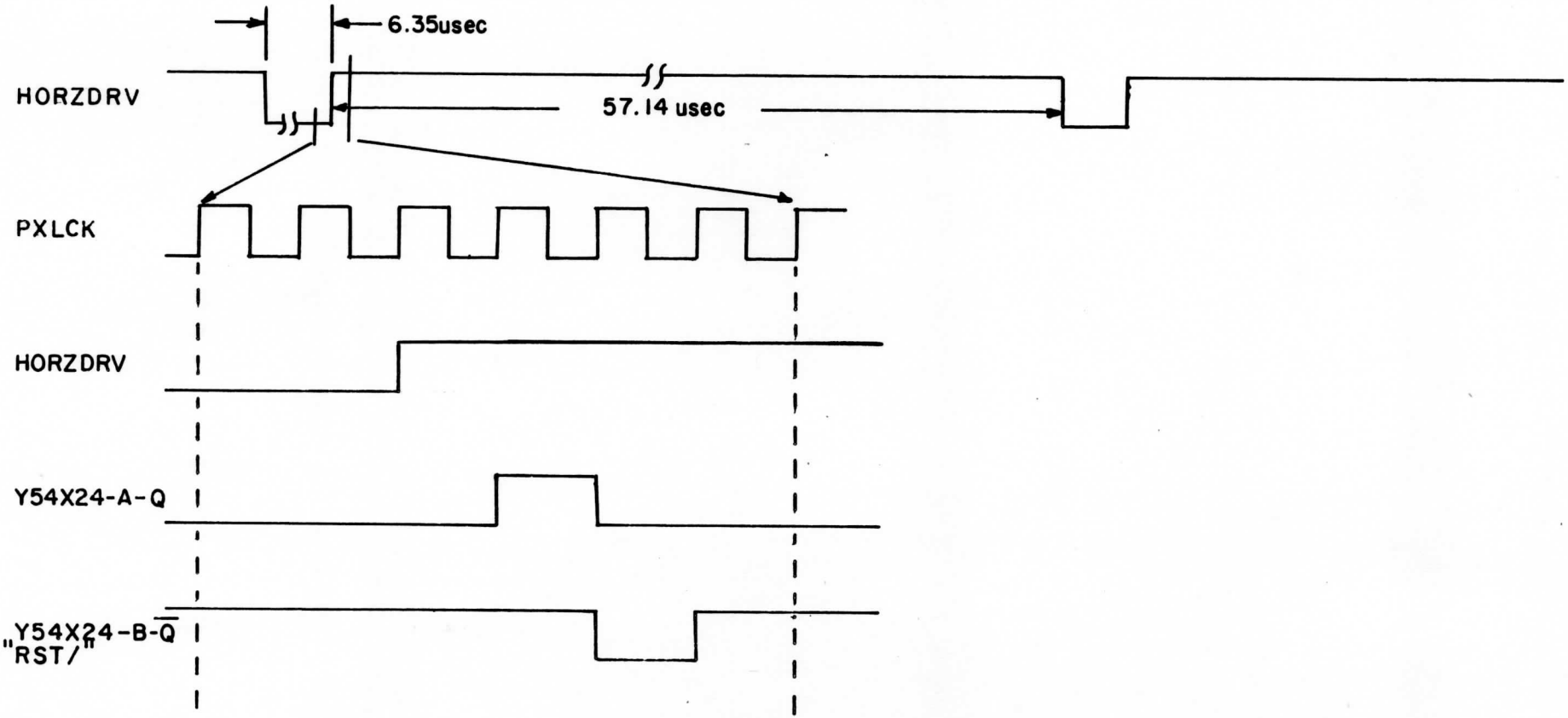
The R Counter is shown on the bottom third of sheet 8 of the schematic diagram. As explained in the Functional Description, the counter not only produces address inputs used for DATARAM "reads," it also produces many primary control signals used in refresh and write timing. The counter essentially generates four repeating timing cycles. A timing cycle consists of addressing 16Ø consecutive pixel partitions (16 word times), followed by a 1Ø-pixel-wide refresh cycle (1 word time) and concluded with a 2Ø-pixel-wide R/M/W cycle (2 word times). Therefore, a timing cycle is 19 word times in length and is referred to as a 19X cycle (where X = one word time = Ø.814 μsec). The fourth cycle is slightly longer (21X) than each of the first three cycles, but is still referred to as a 19X cycle.

The primary components of the R Counter are BCD counter Y42X48 and binary counters Y48X48 and Y36X48. The only external drive signals to the counter are horizontal drive (HORZDRV) and pixel clock (PXLCK). All 19X cycle waveforms are produced by controlling the counter enables and clear inputs. HORZDRV is a master clear for the counter. PXLCK is the 12.285-Mhz clock applied to all R counter chips.

HORZDRV is applied to a positive-edge detector consisting of data latches Y54X24-A and -B. The static conditions of the A and B sections are set and reset respectively. Refer to Timing Diagram 2. The rising trailing edge of HORZDRV latches a "one" into the Q output of section A. Since the B section is clocked by PXLCK, the first rising edge of PXLCK following a high input from section A causes the Q/ output of section B to go to "zero". The Q/ output of section B acts as the reset for the counters and Y54X24-A. Since a 74LS74 features an asynchronous clear, the Q output of section A returns to "zero" a few nanoseconds after the Q/ output of section B goes to zero. This places a "zero" input to the B section; the next PXLCK returns the Q/ output of section B to a "one". Thus, the reset is one PXLCK period long.

Y42X48, the BCD counter, counts continuously between reset pulses. The ripple carry output (pin 15) is applied to triple input AND gate Y42X39-C. The ripple carry is active high while the counter has an output of 9 (1ØØ1B). The other two inputs to Y42X39-C are the inverted ripple carries from both binary counters.

These counters have an active high ripple carry any time they are at their maximum count (15D or 1111B). Therefore, the BCD counter's ripple carry output is allowed to pass to the first binary counter as long as neither binary counter is at a full count. Since counter Y39X48 increments only once for each 1Ø count cycle from the BCD counter, the ripple carry output from Y39X48 goes high on the $15Ø^{th}$ count (1Ø·15), disabling AND gate Y42X39 and providing a high input to pin 5 of AND gate Y42X39-B. The ripple carry of the BCD counter and the inverted ripple carry from counter Y36X48 are also applied to AND gate Y42X39-B. Thus, the ripple carry outputs from the BCD counter are now channeled into counter Y36X48. When the BCD counter output goes to 9 (total count = 159), counter Y36X48 is enabled. The next clock pulse overflows the BCD counter to "zero" and increments Y36X48 to a count of "one" (QA active high). Counter Y39X48



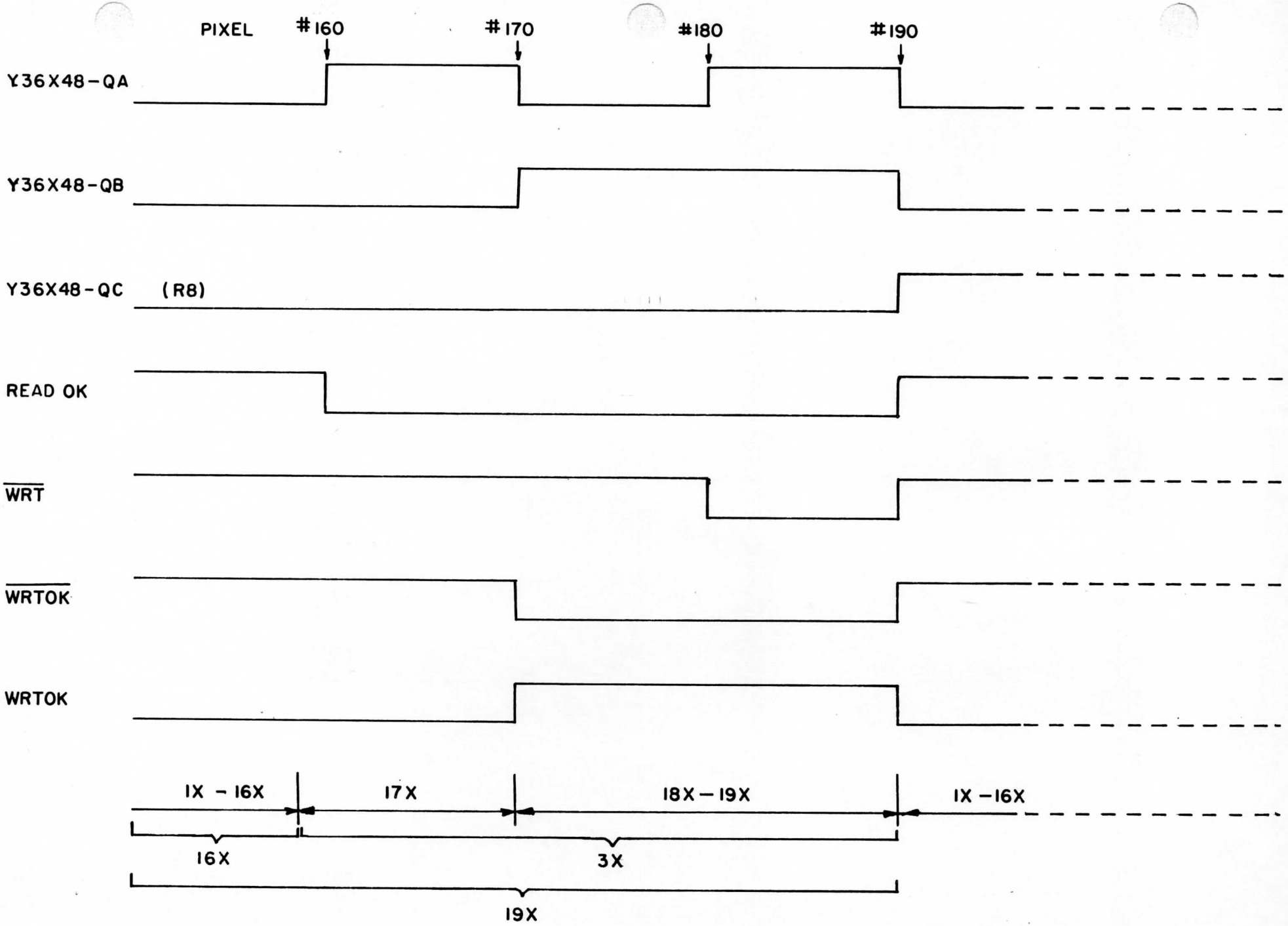
TIMING DIAGRAM - 2 "R" COUNTER RESET

(6450-0377)

does not change and still has a high ripple carry output. At this time, RØ-R9 indicate a count of 15ØD. The BCD counter repeats the cycle with counter Y36X48 incrementing to "two" (QB active high). Again, RØ - R9 count from 15Ø-159 and reset to 15Ø. The BCD counter repeats its cycle again, incrementing Y36X48 to "three" (QA and QB active high) and the RØ-R9 output cycles from 15Ø through 159 and back to 15Ø. Note that, at this time, pins 2 and 13 of AND gate Y42X49-A are qualified. When the BCD counter reaches a count of 9 and generates a ripple carry output, counter Y36X48 increments to "four" (QC active high) and AND gate Y42X39 is qualified, resetting counter Y39X48. The RØ-R8 outputs indicate a count of 16Ø ($1Ø \cdot 2^4$).

In summary, RØ-R9 count normally from Ø-159, reset to 15Ø, count up to 159, reset to 15Ø, count to 159, reset to 15Ø, count up to 159, reset to 15Ø, and count up to 16Ø. The three partial resets require 3Ø pixels to increment from 159 to 16Ø. This completes one 19X cycle (19Ø pixels or 19 word times). This process repeats four times in each horizontal cycle.

QA and QB outputs of counter Y36X48 provide a convenient source of timing signals for the refresh and R/M/W cycles. Timing diagram 3 shows the relationships between READOK, WRT/, WRTOK/, Y36X48-QA and -QB, and the 19X cycle. Inverters Y45X39-D and Y48X4Ø-F and AND gate Y42X31-C function as a negative logic NOR gate and produce an inactive low output if QA, QB, or both QA and QB are active high. The output of this gate is READOK. Before the generation of WRTOK/ and WRT/ is explained, J-K flip-flop Y45X48-A should be addressed. Remember that the 4th 19X cycle is actually 21 word lengths long. At the end of the 19th word, counters Y36X48 and Y39X48 both have full counts of 15D (1111B). Therefore, the ripple carry from both counters is active high, preventing any further counting by these counter stages, because AND gates Y42X39-C and Y42X39-B are both disqualified. Until a new master reset (RST/) is received, the only counter chip which continues to count is Y42X48 (counts from Ø-9 and overflows back to zero). Therefore, QA and QB outputs from Y36X48 both remain active high for two word times (2Ø and 21) longer than normal. The purpose of flip-flop Y45X48 is to terminate WRTOK/ and WRT/ at the end of 19X on the fourth cycle in each horizontal time. To accomplish this, the K input is driven by RST/ and is low for only one pixel clock period during the master reset. During the master reset, all counters go to zero



TIMING DIAGRAM 3 - R COUNTER-CYCLE RESET

(6450-0377)

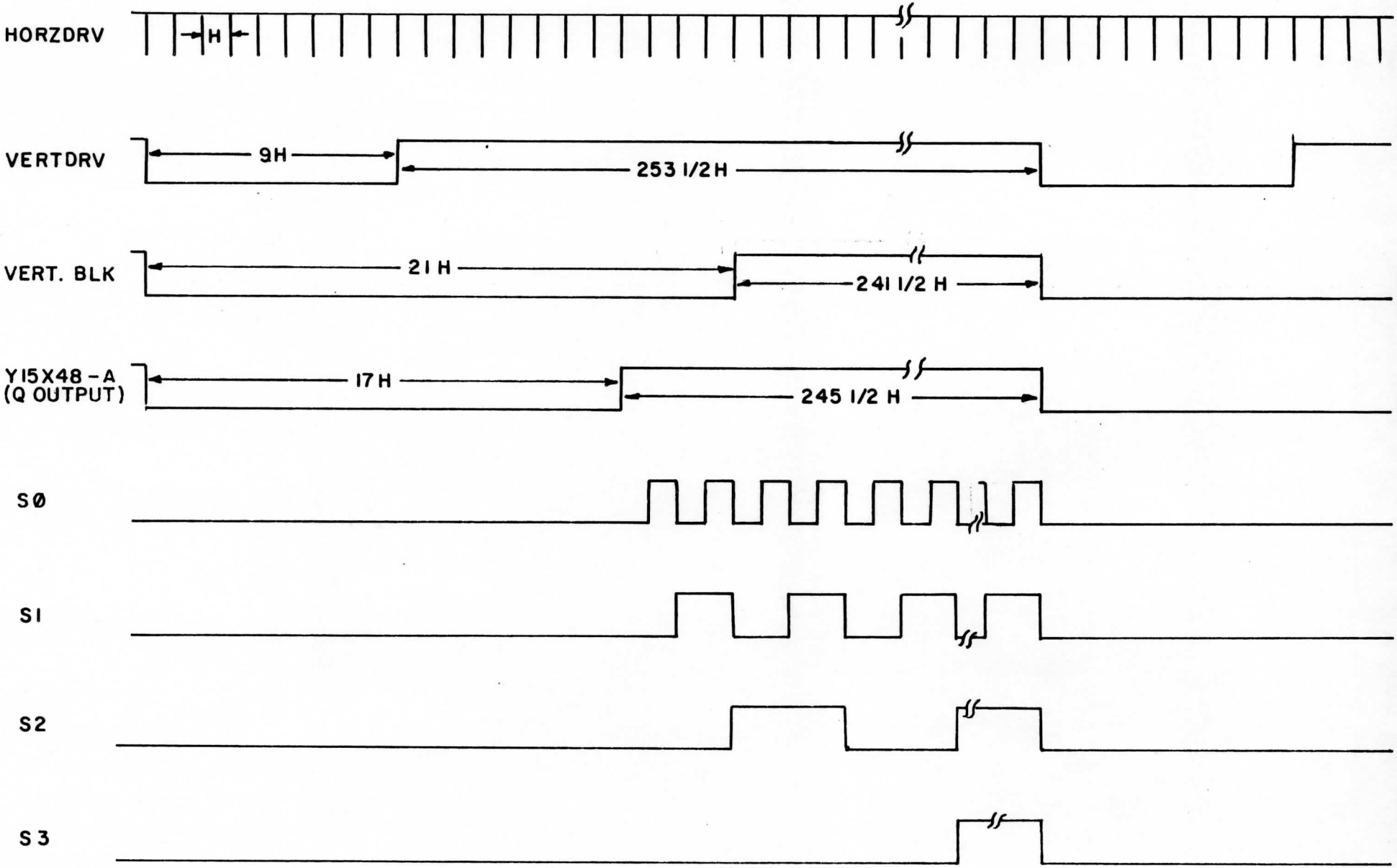
and AND gate Y42X41-B is disqualified, placing a low on the J input of the flip-flop. Now, when the next rising edge of PXLCK arrives (coincident with trailing edge of RST/) the flip-flop resets, placing a high on the Q/ output. When both Y36X48 and Y42X48 generate coincident ripple carries (end of 19Øth pixel of 4th cycle only), AND gate Y42X31-B places a high on the J input (the K input is also high). On the next PXLCK clock cycle, flip-flop Y45X48-A sets, placing a zero on the Q/ output. Since the Q/ output is NANDed with QA and QB, WRT/ and WRTOK/ are always 1X and 2X in duration, respectively, regardless of which 19X cycle is being generated.

Since RØ-R3 are BCD outputs, they are used to select the pixel partitions within a 3Ø-bit word, while outputs R4-R9 are used to address the words in a horizontal line (Ø-63). RØ-R9 are used to address the Line Buffers (Write Address Bus - see Figure 2).

S Counter Section

The S Counter Section is used as the horizontal line address generator. It is shown at the top of sheet 8 and consists of binary counters Y6X48, Y3X48 and Y9X48 and J-K flip-flop Y15X48-A. The actual counter consists of Y6X48 and Y3X48. Counter Y9X48 and J-K flip-flop Y15X48-A form an eight-horizontal-scan delay which centers the image on the display screen.

To understand the need for the delay, a brief review of the TV timing waveforms may be useful (see Timing Diagram 4). First, let's review VERDRV. This signal goes low at the beginning of each 262.5-horizontal-line field and stays low for nine horizontal scans. Next, there is a vertical blanking signal (part of composite blanking) which blanks the CRT for 21 horizontal scans, beginning with the start of VERTDRV. Thus, there are 12 horizontal lines blanked between the time that VERTDRV goes high and the end of the vertical retrace blanking period. VERTDRV is used as a pre-set for counter Y9X48 whose MSB preset input is tied high. Note that VERTDRV is used to clear the flip-flop. Therefore, VERTDRV causes counter Y9X48 to preset to a count of eight and flip-flop Y15X48-A to clear, causing counters Y6X48 and Y3X48 to clear. Seven horizontal drive pulses are required (after VERTDRV goes high) for Y9X48 to reach a full count and generate a ripple carry out. The eighth HORZDRV pulse sets Y15X48-A and removes the clear pulse from Y6X48 and Y3X48. Therefore, the S counter



TIMING DIAGRAM 4 -"S" COUNTER
(6450-0377)

begins counting with the 9th HORZDRV pulse following the positive-going edge of VERTDRV. Inserting the eight-horizontal-line delay moves the image down, reducing the number of blanked data lines from 12 to four. Once the clear is removed from the counter, it counts each horizontal drive pulse until it is cleared again by the flip-flop. The counter reaches a maximum count of about 245 decimal.

Q Counter

The Q Counter generates the Line Buffer Read Address Bus (see Figure 2). The Q counter is a BCD counter whose ripple carry output drives a six-bit binary counter. The BCD counter is counter chip Y33X48 and the binary counter consists of counter chips Y3ØX48 and Y27X48. All counter chips are clocked by PXLCK. The "clear" input of counters Y33X48 and Y3ØX48 is connected to the pre-set input of counter Y27X48 and driven by VIDEN (video enable - AND gate Y54X32-D). Thus, when VIDEN goes low, the counter is preset to a count of 192ØD (full count = $1Ø \cdot 2^8$ = 256Ø). Therefore, the counter develops a one-pixel-wide ripple carry on the 64Øth count of PXLCK.

There are 648 visible pixels (plus or minus a few) in each horizontal line (132 are blanked by horizontal blanking), but only 64Ø pixels of data. An adjustable delay, consisting of binary counters Y21X48 and Y18X48, programmed by carrier Y24X48, allows the image to be centered on the screen. The nominal delay for image units is 53 pixels while for graphics it is 55. The slight difference is due to differences in channel processing delays. Both channels have inherent delays of about 8Ø pixels. Thus, the total delay is about 133-135 pixels, slightly more than enough to prevent display of data during the blanking period and thereby centering the image.

The ripple carry output from the delay counter (pin 15 of Y18X48) is applied to the J input of J-K flip-flop Y15X48-B. The K input of this flip-flop is driven by the inverted ripple carry output of the Q Counter and remains high until the terminal count of the Q Counter and (64Øth pixel) is reached. Therefore, when the J input of Y15X48-B goes high and a rising edge of PXLCK occurs at the clock input, the flip-flop sets, bringing VIDEN high and enabling the Q Counter. The flip-flop remains set until the Q Counter ripple carry output causes the K input of Y15X48-B to

go low. When this happens, the flip-flop resets on the next clock pulse because the J input is also low. Therefore, the signal VIDEN is active high and 64Ø pixels long, centered in the unblanked horizontal scan time. VIDEN is applied to latch Y51X4Ø-A, which is clocked by PXLCK. Thus, the output of Y51X4Ø-A (VIDENA) is identical to VIDEN but delayed by one PXLCK period (81.4 nsec). VIDENA gates the Line Buffer partition data to the output line drivers (see Y54X32 and Y57X8 on sheet 4).

DATARAM Read/Write Address Multiplexer

The DATARAM Read/Write Address Multiplexer is shown on sheet 5 of the schematic diagram. The multiplexer consists of inverting tri-state octal bus drivers Y48X21, Y48X1Ø, Y51X21, and Y51X1Ø. The X and Y write addresses are applied to Y48X21 and Y51X21 enabled by WRTOK/ (WRTOK/ is shown in Timing Diagram 3). The R and S read addresses are applied to Y48X1Ø and Y51X1Ø, enabled by WRTOK.

Momentarily, let's focus our attention on S8, the A7 input of Y41X1Ø. S8 is generated on sheet 8 of the schematic. The signal OE (Odd/Even) originates on the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board. It has a frequency of 6Ø hz (or 5Ø hz) and is always active high during the first field of every frame. The bipolar output of the line drivers on the 6Ø/5Ø Hz TV Timing and Colorizer-Brooktree board are applied to the inputs of line receiver Y54X8-D. Note, however, that the inverted drive is applied to the non-inverting input of the receiver while the non-inverted drive is applied to the inverting input. Thus, S8, the output of Y54X8-D is inverted and is <u>low</u> during the first field of each frame.

S8 forms the 7th LSB of the read address. The six LSBs form the word address for each horizontal line of data (Ø-63). Remember that RØ-R3 are used to address the pixel within each word. Since S8 remains low for the entire first field (256½ lines), data is read from every other 64-word block. For example, assume we are reading a frame (even and odd field) which begins at address ØØØØØØH. We read words Ø-63, 128-191, 256-319, 384-447, ...3Ø,72Ø - 3Ø,783. Now, S8 goes high (second field) and all R and S address lines reset to "zero". This time, we address 64-127, 192-255, 32Ø-383, ...3Ø784-3Ø847. Thus, we read out of memory in an interleaving fashion. Therefore, the data must be written in an identical manner. During data storage, the pixels are converted to partitions and

written into memory one partition at a time. When a line (64 words), is completed the X and Y addresses are re-indexed so that the next line will be in the proper 64-word block for interleaved data read out.

Read/Write Frame Load Latch

The Read/Write Frame Load Latch section is shown on the top half of sheet 5 of the schematics. Refer to sheet 6. The MULTIBUS data bus enters the board from the P1Ø connector and is inverted by inverting tri-state octal buffer Y69X1Ø. The non-inverted data bus is applied to another tri-state inverting octal buffer (Y51X32) located on sheet 5.

The inverted data bus (DATØ/ - DAT7/) is applied to Write and Read Frame Latches (Y45X21 and Y45X1Ø respectively) which are latched by corresponding memory-mapped control signals WRITE FRAMLD/ and READ FRAMLD/. For more information on these control signals, see the Control and Handshake Section. The latched outputs are placed on the ADDR15/ - ADDR2Ø lines by enabling one of the latch's tri-state controls. The write and read latches are enabled by WRTOK/ and WRTOK respectively. For more information on these signals, see the R Counter description and/or Timing Diagram 3.

WRITE FRAMLD/ is applied directly to Y45X21 via inverter Y57X32-D. READ FRAMLD/ is applied to Y45X1Ø via data latch Y51X4Ø-B, inverter Y57X32-B, and AND gate Y42X31-D. Since READ FRAMLD/ is inactive high at all times except during an actual frame address load, and is applied to both the D input of Y51X4Ø-B and the inverter, AND gate Y42X31-D normally has both inputs low. When READ FRAMLD/ goes active low, pin 13 of the AND gate is qualified immediately by the inverter output. The CPU continues to hold READ FRAMLD/ low until it receives a transfer acknowledge (XACK/) or times out. Latch Y51X4Ø is clocked by the rising edge of WRTOK which occurs at the end of a 19X cycle (same as the beginning of the next 19X cycle, the beginning of the 16-word read section). The rising edge of WRTOK latches the active low D input, causing the Q/ output (pin 8) to go high. This qualifies the AND gate, latching the Read Frame Latch and initiating the XACK/ response. Thus, a new Read Frame Load command is processed only at the beginning of a 19X cycle.

THE CONTROL AND HANDSHAKE

The circuitry for this section is contained primarily on sheets 7 and 9 of the schematic diagrams. Figure 4 is the functional block diagram for this section.

Control Section

Memory Mapped Control Generator

The entire MULTIBUS address bus is applied to two PROMs, via two octal buffers, for address decoding (refer to sheet 7). This section decodes the address mapped control signals into one of three sets of controls. The particular set of controls is a function of the unit number (Ø, 1 or 2). A board produces one of the following sets of control signals: FCØ1H - FCØ9H, FC1ØH - FC19H, or FC2ØH - FC29H. The particular set is selected by carrier Y57X16, as explained in the next paragraph.

MULTIBUS address lines ADR5/ - ADRC/ are applied to buffer Y63X1Ø, whose outputs drive A1-A8 of PROM Y66X21. AØ of the PROM is driven by ADR4/ via buffer Y66X1Ø. The function of PROM Y66X21 is to "activate" PROM Y63X21 by placing a logic low on A8 of PROM Y63X21. PROM Y66X21 screens out all binary addresses which do not meet the criteria: XXX1 11ØØ ØØAA XXXX, where X = don't care and AA = unit code (ØØ = unit Ø, Ø1 = unit 1, and 1Ø = unit 2). Address XXX1 11ØØ ØØØØ XXXX generates a low at pin 12 (O_1), XXX1 11ØØ ØØØ1 XXXX generates a low at pin 11 (O_2), and XXX1 11ØØ ØØ1Ø XXXX generates a low at pin 1Ø (O_5). Carrier Y57X16 selects one of the active low outputs and passes it on to PROM Y63X21. As an example, assume this is unit 1. Pin 2 of the carrier is jumpered to pin 13, providing a low to PROM Y63X21 for addresses XXX1 11ØØ ØØØ1 XXXX only.

All of the active low outputs from PROM Y63X21 occur in the first (lowest addressed) 32 words in memory. Therefore, to address this area, A5-A7 of PROM Y63X21 must be "zero"s. Since these inputs are driven by the inverted address lines ADRE/ - ADRF, the corresponding non-inverted address lines must be all "one"s. Therefore, the only addresses that can produce control signals are FCØXH, FC1XH, and FC2XH, where X = don't care. ADRØ - ADR3/ are decoded by PROM Y66X21 to produce the following active low outputs:

O_1 = FCX1 - FCX7

O_2 = FCX8 - FCX9

O_3 = FCX1 - FCX9

where X = unit number (Ø, 1 or 2 for graphics, image #1 or image #2 respectively)

Output O_1 (PARLD/) is further decoded by 3-to-8 line decoder Y69X3Ø, O_2 (GLOAD/) is further decoded by 2-to-4 line decoder Y66X3Ø, and O_4 (STBGEN/) initiates the transfer acknowledge and limits the duration of the Y66X3Ø outputs.

PARLD/ enables 3-to-8 line decoder Y69X3Ø. Inverted address lines ADRØ - ADR2/ are uninverted by inverters Y67X32-A, -B and -C and applied to the A, B and C inputs of the 3-to-8 line decoder. The decoder provides five memory-mapped outputs, defined as follows:

Output	Address	Control (see sheet 7 except as noted)
Y_1	FCX1	WRITE FRAMLD/ (see sheet 5)
Y_4	FCX4	MLDØ/ 8 LSB X Counter Preload Latch
Y_5	FCX5	MLD1/ 2 MSB X Counter Preload Latch
Y_6	FCX6	MLD2/ X and Y Counter binary load strobe
Y_7	FCX7	MLD3/ X Counter BCD load strobe

STBGEN/ is normally high and is applied to the 1D input of quad D latch Y72X3Ø. This latch is clocked by PXLCK and results in a low at 1Q/ and 2Q/, and a high at 1Q and 2Q (note that output 1Q is connected to the 2D input). Thus, NAND gate Y51X48-A is normally disqualified (high), forcing a high at OR gate (shown as inverted input NAND gate) Y6ØX4Ø-D. Since STBGEN/ goes low when either PARLD/ or GLOAD/ goes low, assume GLOAD/ went low, qualifying the pin 12 input of the OR gate. At this same time, the 1D input of the latch is also low. On the rising edge of the next PXLCK, 1Q/ goes high, qualifying NAND gate Y51X48-A and placing a qualifying low at the pin 13 input of the OR gate. The OR gate now produces a low output, enabling 2-to-4 line decoder Y66X3Ø. This decoder is qualified

for one PXLCK only, because the next PXLCK latches a "zero" into the 2Q output of Y72X3Ø, disqualifying NAND gate Y51X48-A and OR gate Y6ØX4Ø-D. At this time, latch output 2Q/ is high, enabling NAND gate Y61X48-C (pin 1Ø input was already high, as we will see later). The low outputs of Y51X48-C and STBGEN/ produce a low at the output of OR gate Y57X57-A, causing pin 12 of AND gate Y57X4Ø to go low (XXACK/). XXACK/ is applied to line driver Y57X8-D, where it becomes XACK/, the transfer acknowledge signal. When PARLD/ goes low, the XACK/ is generated in an identical manner, however, the 2-to-4 line decoder never qualifies.

In the previous paragraph, we saw how XACK/ was generated and how the 2-to-4 line decoder Y66X3Ø becomes enabled. Now, we will see how GLOAD is decoded. The decoder is enabled by GLOAD/ (FCX8 or FCX9) for one PXLCK pulse. Note that ADRØ is applied to the A input and UNITØ/ (O_1 output of PROM Y66X21) drives the B input. The B input is low for unit Ø addresses. Therefore, $Y_Ø$ and Y_1 outputs of the decoder are used by graphics units and Y_2 and Y_3 are used by image units. ADRØ/ is used to separate those addresses ending in "8" (Y_0, Y_2) from those ending in "9" (Y_1, Y_3). The four Y outputs from Y66X3Ø are applied to three inverting input NOR gates (Y57X48-A, -B and -C). Gate A combines Y_1 and Y_3 (addresses ending in 9), gate C combines Y_0 and Y_3 (addresses ending in 8) and gate B combines Y_0 and Y_3 to produce WRTSTRT/ (Write start). The output of the gates are summarized as follows:

GATE	ADDRESS	UNIT	2-4 OUTPUT	SIGNAL
Y57X48-A	FCØ9, FC19, FC29	Ø, 1, 2	Y_1, Y_3	DATLD/
Y57X48-B	FCØ8, FC19, FC29	Ø, 1, 2	$Y_Ø$, Y_3	WRTSTRT/
Y57X48-C	FCØ8, FC18, FC28	Ø, 1, 2	$Y_Ø$, Y_2	NPOSLD/

WRTSTRT/ initiates the request for an R/M/W cycle. Therefore, all required setup steps (address, X and Y counter modes, data loading etc.) must be completed prior to any action which generates a WRTSTRT/. As shown above, WRTSTRT/ is initiated by a NPOSLD/ to unit Ø (graphics) or a DATLD/ to units 1 or 2 (image). A DATLD/ to units 1 or 2 or a NPOSLD/ to unit Ø are the final CPU action in a pixel storage activity. DATLD/ is

the latching signal used to latch a three-bit data partition into the Data Latch (see Figure 2 and sheet 6 of the schematic). When loading an image, three-bit data partitions are stored consecutively within a 3Ø-bit word; each 64-word packet, which makes up a horizontal line, is consecutive. Once set up, the X and Y address counters automatically index to the next address each time a partition is written (the Y counter is indexed at the end of each horizontal line of data). This means that writing the next pixel, to units 1 or 2, is initiated by DATLD when the pixel partition is latched.

Since the data, which is written into a graphics frame, is generally constant (points of equal intensity which form lines etc.), the data is written initially by doing a DATLD/ command. Thereafter, a new pixel is written automatically by doing a NPOSLD/. NPOSLD/ is used to latch X and Y counter mode controls (see Figure 3 and sheet 6 of the schematics). Note that several other commands (MLDØ/ - MLD3/) may be required before actually performing the NPOSLD/ command.

The two signals from the Memory-Mapped Control Generator that have not been addressed yet are READ FRAMLD/ (Read Frame Load) and ERASE CMD/ (Erase Command). These signals are developed by PROMs Y72X21 and Y69X21, and carrier Y57X16. Y72X21 is driven by the eight MSBs of the MULTIBUS address bus and is programmed to produce an active low at output O_1 for addresses FCØØH - FCFFH only. The active low from Y72X21 drives the MSB input of PROM Y69X21. The lower eight address inputs of PROM Y69X21 are driven by the eight LSBs of the MULTIBUS address bus. PROM Y69X21 is programmed to produce active outputs for the following four addresses only:

- O_1 = FCØØH
- O_2 = FC1ØH
- O_3 = FC2ØH
- O_4 = FCØ3H

The outputs are applied to the unit programming carrier (Y57X16) where O_1, O_2, or O_3 are selected for the READ FRAMLD/ command. If this is unit Ø (graphics unit), pin 7 of the carrier also is connected to pin 8 and is used as the ERASE CMD/ signal. Thus, only unit Ø can be erased. Also note that the erase command is used as an input to the XACK/ generator.

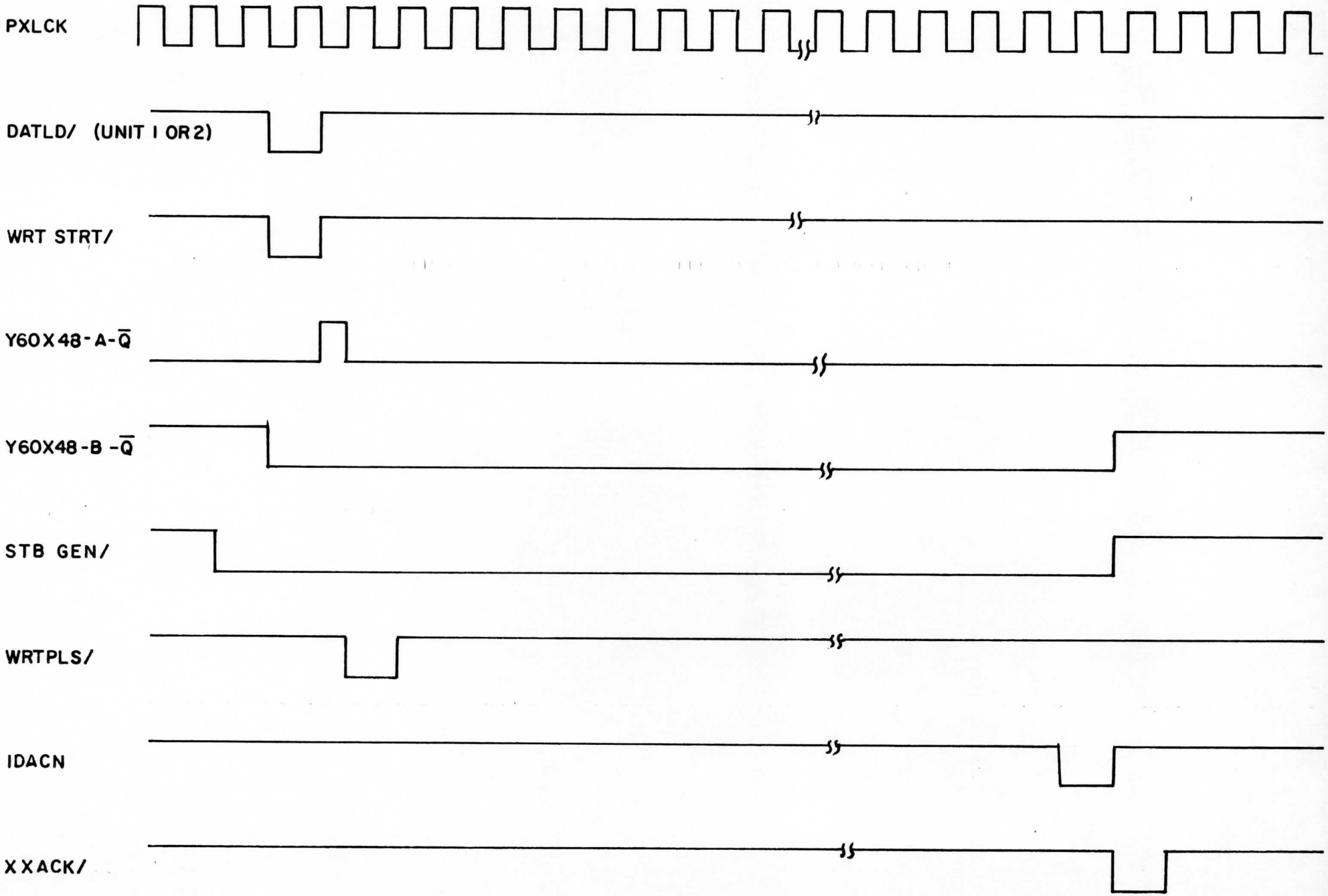
Table 1, below, summarizes the outputs from the Memory-Mapped Control Generator.

FCØØ = READ FRAMLD/	unit Ø
FCØ1 = WRITE FRAMLD/	unit Ø
FCØ2 = Not used	
FCØ3 = ERASE CMD/	unit Ø
FCØ4 = MLDØ/	unit Ø
FCØ5 = MLD1/	unit Ø
FCØ6 = MLD2/	unit Ø
FCØ7 = MLD3/	unit Ø
FCØ8 = NPOSLD/, WRTSTRT/	unit Ø
FCØ9 = DATLD/	unit Ø
FC1Ø = READ FRAMLD/	unit 1
FC11 = WRITE FRAMLD/	unit 1
FC12 = Not used	
FC13 = Not used	
FC14 = MLDØ/	unit 1
FC15 = MLD1/	unit 1
FC16 = MLD2/	unit 1
FC17 = MLD3/	unit 1
FC18 = NPOSLD/	unit 1
FC19 = DATLD/, WRTSTRT/	unit 1
FC2Ø = READ FRAMLD/	unit 2
FC21 = WRITE FRAMLD/	unit 2
FC22 = Not used	
FC23 = Not used	
FC24 = MLDØ/	unit 2
FC25 = MLD1/	unit 2
FC26 = MLD2/	unit 2
FC27 = MLD3/	unit 2
FC28 = NPOSLD/	unit 2
FC29 = DATLD/, WRTSTRT/	unit 2

Table 1

Read and Write Select Generator Sections

The Read and Write Select Generators are shown on sheet 3 of the schematics. The Read Select Generator outputs drive the 1Ø Read Select input lines to the Partition Read/Latch Selector block shown in Figure 2. The generator consists of Y33X17, a BCD-to-Decimal decoder, driven by RØ - R3. Timing Diagram 5 shows the outputs of the Read Select Generator. Outputs READ1/ and READ9/ are also used as control inputs to the Handshake Section.



TIMING DIAGRAM - 5 - WRITE REQUEST INITIATION
(6450-0377)

The Write Select Generator consists of BCD-to-Decimal decoder Y36X17 and is driven by XØ - X3. The outputs from this section drive the Write Data Selector block shown in Figure 2. Note that WRTOK/ is ORed with X2 and X3 to produce the C and D inputs of Y36X17 respectively. WRTOK/ is high at all times except during the 18X - 19X time shown in Timing Diagram 3. Therefore, only during this time can there be a valid BCD input to the BCD to Decimal decoder. Invalid inputs result in inactive high outputs from Y_0 - Y_9. Thus, WRTOK/ is used to disable the Write Select Generator at all times except during a write cycle.

DATARAM Mode Control Generator

There are five mode-control signals that the DATARAM uses to determine whether an operation is a Read, Write or R/M/W. In addition, these same five lines determine whether the operation is to be performed on a 16- or 32-bit word.

The generator is shown at the bottom of sheet 9 of the schematics and consists of Y48X32-A and -B, and AND gates Y42X23-A and -B. Four of the five control lines are tied together and driven by a common source. These signals are MWRLBN (Memory Write Lower Byte), MWRUBN (Memory Write Upper Byte), MWRLBAN (Memory Write Lower Byte Upper Word) and MWRUBAN (Memory Write Upper Byte Upper Word). Tying these lines together results in 32-bit operations only. Whether an operation is a 32-bit read, write or R/M/W is determined by the relationship between this group of controls and the control signal MRDRN (Memory Read). The relationships between these signals and the operations which result are shown below:

MRDRN	Four Line Group	Operation
Low	Low	R/M/W 3Ø-bit word
Low	High	READ 3Ø-bit word
High	Low	WRITE 3Ø-bit word (erase)
High	High	Invalid, not used

D latch Y48X32-A is clocked by ERASE CMD/ and the D and CLR inputs of the latch are driven by the Q/ output of D latch Y48X32-B. Since latch Y48X32-B normally is reset, the D input of Y48X32-A normally is high. Therefore, if an ERASE CMD/ is generated, a high is latched into Y48X32-A, driving its Q output high. This high output is latched into Y48X32-B by S8, the odd/even (OE) signal. S8 is positive going at the beginning of the second field of each two-field frame. On the rising edge of S8, Y48X32-B sets, driving the Q output high and the Q/ output low. The Q/ output resets Y48X32-A, which places a low at the input of Y48X32-B. On the next rising edge of S8, Y48X32-B also resets, removing the clear input to Y48X32-A. Thus, when an ERASE CMD/ is generated, Y48X32-B sets on the next rising edge of S8 and resets on the following S8 rising edge. The Q/ output is applied to the Write Data Latch (see Figure 2) which causes all "zero"s to be written into all ten pixel partitions simultaneously. Note that Q/ is also applied to AND gate Y42X23-A and -B. Gate Y42X23-A ANDs the Q/ output of Y48X32-B with WRTOK/ to produce the four control line group. Therefore, the Q signal is low during a frame erase and during the 18X - 19X time shown in Timing Diagram 3 (Write phase of an R/M/W cycle). This gate produces a high output during Read time only. Y42X23-B ANDs the Q/ output of Y48X32-B with WRT/ to produce $\overline{\text{WRITE}}$/READ. This signal controls the direction of data flow through the Bi-Directional Data Bus Driver (see Figures 1 and 2). This signal is high during read time, placing the bus driver in the input mode. WRITE/READ, ERASE/ and the four control line group all go low during a frame erase. The Q output of Y48X32-B drives the MRDRN control signal and is low only during the erase cycle. It is high during Read and R/M/W cycles.

Handshake Section

The Handshake Section consists of the six blocks in Figure 4 not yet discussed. With exception of the Write Request Generator block, all circuitry is located on sheet 9 of the schematics. The Write Request Generator is contained on sheet 7.

Write Request Generator

The Write Request Generator consists of D-latches Y6ØX48-A and -B, AND gate Y51X48-B, and sections 3 and 4 of quad D latch Y72X3Ø. In

addition, NAND gate Y51X48-C and OR gate Y57X57-A are used to generate a Write XACK/ response signal. Timing waveforms for this section are shown in Timing Diagram 5. The timing diagram assumes that a DATLD/ command has just been issued to an image unit (unit 1 or 2), resulting in a one-PXLCK-clock-wide WRT STRT/ pulse which presets latch Y6ØX48-B. This latch remains set until the completion of the R/M/W cycle and is used to generate an input to the XACK/ (transfer acknowledge) generator. Input to the XACK/ generator informs the CPU that the storage operation is complete.

WRT STRT/ is also applied to the clock input of Y6ØX48-A and resets the latch on the trailing positive edge of WRTSTRT/. When the latch resets, it outputs a logic "one" from the Q/ output which is then applied to the 3D input of quad D-latch Y72X3Ø. On the following rising edge of PXLCK, the logic one is latched, resulting in a high at pin 4 of NAND gate Y51X48-B, and the 4D input of Y72X3Ø. At this time, the NAND gate is qualified because the previous input to 4D was a "zero", resulting in a high at 4Q/. The logic zero output from NAND gate Y51X48-B presets Y6ØX48-A. WRTPLS/ (Write Please), the output of the NAND gate, is the Write request. When Y6ØX48-A is preset by WRTPLS, it outputs a zero from the Q/ output. The logic zero output is applied to the 3D input of the quad latch and is latched on the next rising edge of PXLCK. This disqualifies the NAND gate, limiting the length of WRTPLS/ to 81.4 nsec (one clock period).

Write Request Latch

Refer to sheet 9 of the schematics. The Write Request Latch consists of D-latches Y54X48-A, Y42X15-B, and Y39X17-B, and inverter Y54X4Ø-A. The inverter applies the inverted WRTPLS/ to the clock input of Y54X48-A. Therefore, the leading edge of WRTPLS/ causes a "zero" to be latched into Y54X48-A, driving the Q output WRTGNT/ (Write Granted) low. WRTGNT/ is applied to the clock input of Y6ØX48-B (see sheet 7) and to the D input of Y42X15-B. The negative going input to Y6ØX48-B has no effect because the latch only responds to rising edges. The logic low input to Y42X15-B is latched by WRTOK, which goes positive at the beginning of the 18X word time (see Timing Diagram 3). The logic low Write Request at the output of Y42X15-B is applied to the D input of latch Y39X17-B. The purpose of this latch is to delay processing of the request until the beginning of READ2/

(same as the end of READ1/). The positive-going, trailing edge of READ1/ is used as the clock input to Y39X17-B. The Q output of Y39X17 is applied to pin 1Ø of NAND gate Y48X48-C. This NAND gate is part of the Address Available Generator block shown in Figure 4. The other input to the NAND gate is the output of the Read Request Latch (D-latch Y54X48-B).

Read Request Latch

The Read Request Latch consists of D-latch Y54X48-B, clocked by PXLCK and preset by READOK. When READOK is high (1X-16X word times), an active low READ1/ is latched into Y54X48-B by PXLCK. The output of this latch is applied to pin 9 of NAND gate Y48X48-C, part of the Address Available Generator.

Address Available Generator

The Address Available Generator consists of NAND gate Y48X48-C and D-latch Y42X15-A. The NAND gate multiplexes the requests from the Read and Write Request latches. Because the D input of the latch is grounded, it outputs a "zero" on each rising edge of the NAND gate output. ADRAVN (Address Available), the Q output of Y42X15-A, informs the DATARAM BSC board that an operation is requested (Read, Write or R/M/W), and the data on its address bus is valid. Within about 80 nsec, the DATARAM BSC board responds by bringing ADRACN (Address Accepted) low. ADRACN presets Y42X15-A back to a high output on Q and is applied to AND gate Y42X23-C (pin 9), part of the Response Address Valid Generator Section.

Response Address Valid Generator

Refer to sheet 9 of the schematics. The Response Address Valid Generator consists of:

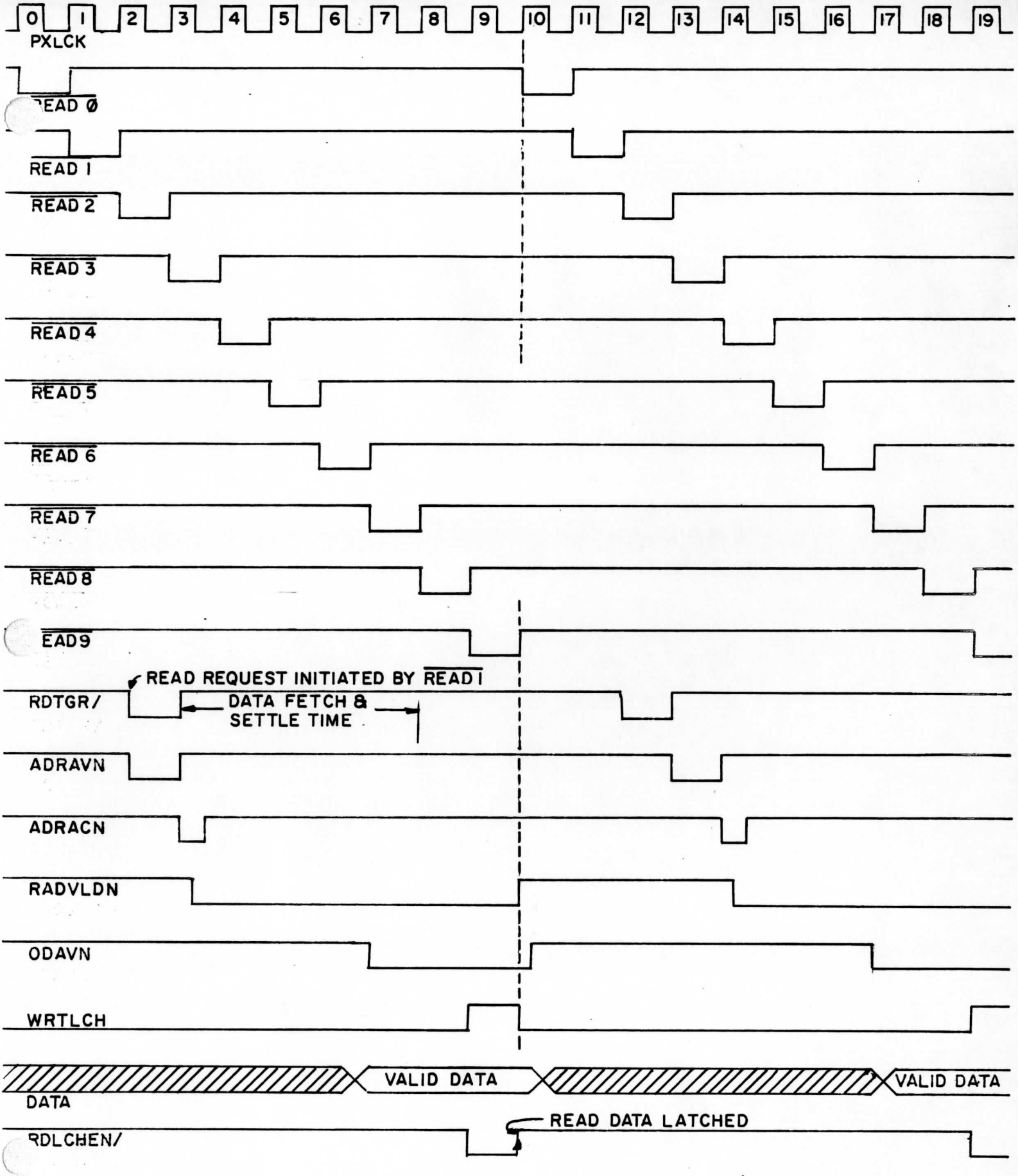
- latches Y42X7-A and -B (center right of sheet)
- latch Y39X25-B (bottom center of sheet)
- inverters Y48X4Ø-C and -D (center of sheet)
- inverter Y54X4Ø-F (bottom left of sheet)
- NAND gate Y48X48-D (center of sheet)
- AND gate Y42X23-C (center right of sheet)

As discussed earlier in the Functional Description, RADVLD/ (Response Address Valid) plays a different role in each of the three modes (read,

write or R/M/W). In the read mode, the RAVLD/ signal tells the BSC board to send the requested data as soon as possible. During the write mode, this signal tells the BSC board that the data on the input data lines to the BSC board are valid. During the R/M/W cycle, this signal performs both of the above functions. Thus, it must go active low twice during an R/M/W cycle, once for the read portion and once for the write. The handshake response from the BSC board is ODAVN (Output Data Available) or IDACN (Input Data Accepted) for read and write cycles respectively. These handshake signals terminate the RADVLD/ signal. RADVLDN is initiated by ADRACN for read, write, and the read portion of the R/M/W cycles. During the Write portion of the R/M/W cycle, RADVLDN is initiated by WRTG.

Refer to Timing Diagram 6. During a read cycle, AND gate Y42X23-C (pin 10) is high and an incoming active low ADRACN causes a low at the CLR input of Y42X7-B. This clears the latch and generates an active low RADVLDN. When the requested data is available in the BSC board, the BSC board generates ODAVN. ODAVN informs the DATARAM Control Board that the requested data is available. ODAVN enters the board at P9-41 and is applied to OR gate Y6ØX4Ø-C. Because ODAVN remains active low until RADVLDN goes high, ODAVN is ORed with READ9/ to produce an active low coincidence pulse. This active low pulse drives NAND gate Y48X48-D low. That is the clock input to Y42X7-B. At the end of READ9/, the output of the OR gate (and therefore the clock input of Y42X7-B) goes high. This latches a logic one into Y42X7-B and ends RADVLDN. When RADVLDN goes high, the BSC board brings ODAVN high, ending the cycle. The signal WRTLCH is used to latch data into the Write Data Latch (see Figure 2) but serves no useful function during the Read cycle.

The Write cycle (used in erase only) is very similar to the Read cycle, except that we receive an active low IDACN in response to RADVLDN. In fact, the Write cycle is conducted only during the 1X-16X word times. Sixteen words are erased (instead of read) during each 19X cycle. The IDACN pulse enters the board at P9-37 and drives the output of AND gate Y42X23-D low. This presets all of the D-latches in the Write Request Latch section and terminates RADVLDN. It also functions as a clock for the X and Y counters (XYINCR/). Thus, an X/Y clock pulse is generated each time the DATARAM acknowledges a data write.



TIMING DIAGRAM-6 - DATA READ CYCLE
(6450 – 0377)

Refer to Timing Diagram 7. The R/M/W cycle is identical to the Read cycle until RADVLDN returns to an inactive high. At this point, the data has been received and one of the partitions has already been substituted with new write data. The modified word was latched into the Write Data Latch by WRTLCH. Now, RADVLDN must be driven low to initiate the Write phase of the R/M/W cycle. Since this cycle is initiated by the Write Request Generator, latches Y54X48-A and Y42X15-B are reset, providing an active low input to Y42X7-A. To generate another RADVLDN signal, a clock pulse is needed at the clock input of Y42X7-A. WRT/ is active low during the 19X cycle time only. Therefore, when inverted, WRT/ produces a rising edge in coincidence with the beginning of the 19X word time. WRT/ is inverted by inverter Y54X4Ø-F and applied to the D input of latch Y39X25-B. Therefore, the output of the latch is positive-going one PXLCK after the beginning of the 19X cycle. The Q output of Y39X25-B is used as the clock input of Y42X7-A, thereby generating the second active low RADVLDN.

Miscellaneous Control Signals

The control signal "Read Latch Enable" (RDLCHEN/) has not been described elsewhere. This signal is shown on sheet 3 of the schematic and consists of D-latch Y39X25-A. The signal latches the read data output of the Read Data Modifier (see Figure 2) into the Read Latch and Partition separator. Refer to Timing Diagram 6. Because READ8/ is applied to the D input and the latch is clocked by PXLCK, RDLCHEN/ goes active low in synchronism with READ9/; the latch must wait until PXLCK goes positive. It is the positive-going edge of RDLCHEN/ which actually latches the data, coincident with the beginning of READØ.

4/PCAT/06

SECTION 7
DATARAM/MULTIBUS INTERFACE
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DATARAM/MULTIBUS INTERFACE

(SSEC DRAWING 645Ø-Ø379, MODIFICATION D and E, DATED 3/17/86)

INTRODUCTION

The DATARAM/MULTIBUS Interface provides the hardware interface between the MULTIBUS and the three DATARAM dynamic RAM storage units. The protocol interfacing is accomplished on the DATARAM Control Board located in each DATARAM chassis.

FUNCTIONAL DESCRIPTION

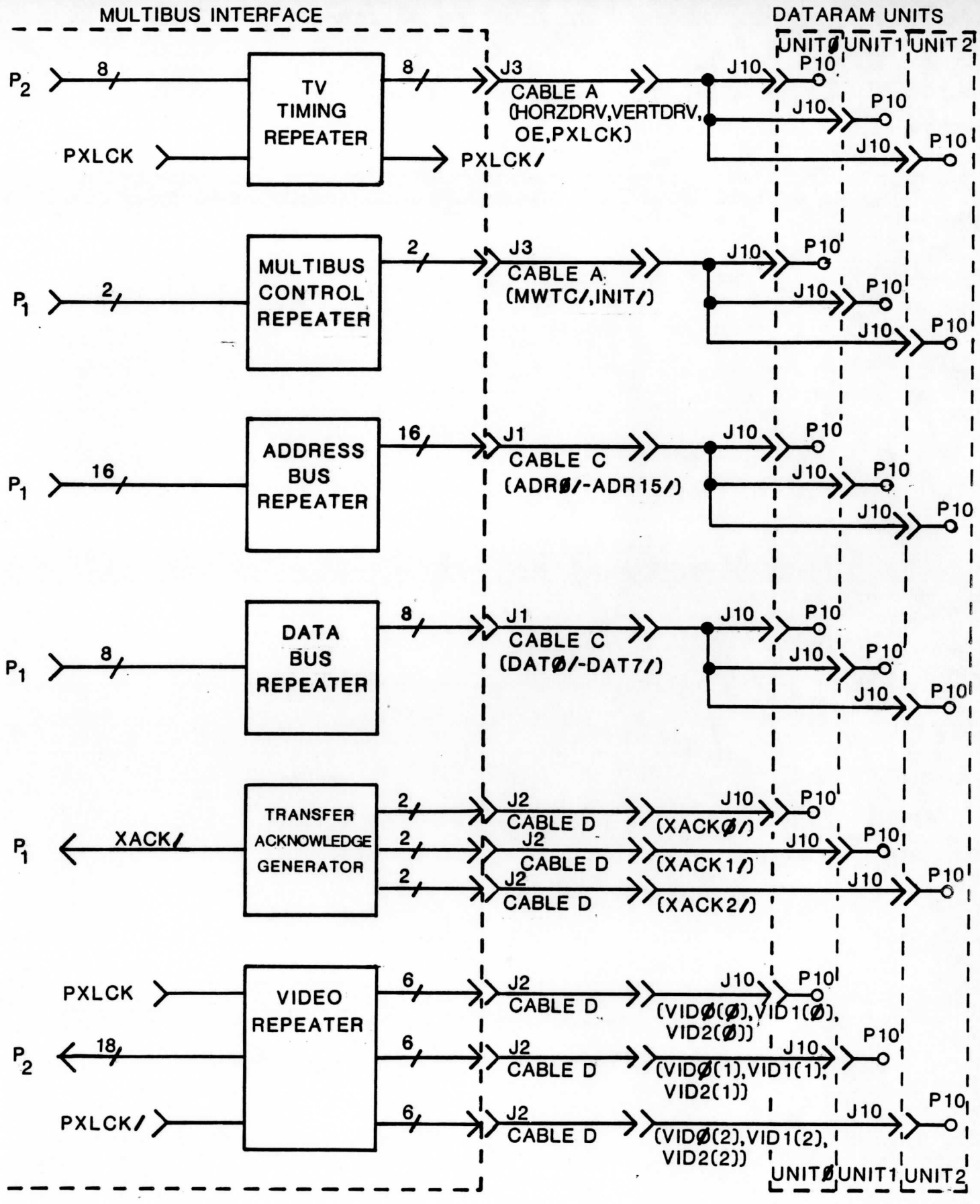
Refer to Figure 1, the functional block diagram of the DATARAM/ MULTIBUS Interface. The following six groups of functional signals are transmitted either from the MULTIBUS to the DATARAMs or from the DATARAMs to the MULTIBUS:

- TV timing signals
- MULTIBUS control signals
- address bus signals
- data bus signals
- the transfer acknowledge signal
- DATARAM digital video output signals

The first four groups of signals are originated by the MULTIBUS while the last two are originated by the DATARAMs.

TV TIMING REPEATER

The TV Timing Repeater receives PXLCK, HORZDRV, VERTDRV, and OE signals from the MULTIBUS P2 bus. These signals are received and re-transmitted as differential signals. The re-transmitted signals leave the interface board via J3 through a 4Ø-conductor ribbon cable (cable A). The ribbon cable is piggy-backed to the A-cable connector on each DATARAM chassis. Within each DATARAM chassis, the A, B, C, and D cables are hard-wired to the J1Ø connector. The P1Ø connector pins on the DATARAM control board connect directly to J1Ø, completing the path from the interface board to the DATARAM control board.



DATARAM/MULTIBUS INTERFACE FUNCTIONAL BLOCK DIAGRAM

FIGURE-1

(6450-0379)

MULTIBUS CONTROL REPEATER

The MULTIBUS control signals MWTC/ and INIT/ enter the interface board from the MULTIBUS P1 bus and are re-transmitted by the MULTIBUS Control Repeater. These signals pass through the same connectors and cables as the TV timing signals (see TV Timing Repeater section above).

ADDRESS BUS REPEATER

MULTIBUS address bus lines ADRØ/-ADR15/ are originated by the MULTIBUS P1 bus and are re-transmitted by line drivers. The re-transmitted signals exit the interface board via the J1 connector, which is connected to the C cable. The C cable is connected to the C connector on the DATARAM chassis. The C connector is wired to J1Ø.

DATA BUS REPEATER

MULTIBUS data bus signals DATØ/-DAT7/ originate in the MULTIBUS P1 bus. The signals are processed exactly as the address bus signals and travel through the same connectors and cables.

TRANSFER ACKNOWLEDGE GENERATOR

When the microprocessor performs a memory read or write to the DATARAM units, it enters a wait state (maximum of 10 msec) until the appropriate unit acknowledges completion of the operation. Because there are three DATARAM units, there are three separate acknowledge outputs (XACKØ/, XACK1/, and XACK2/, output from DATARAM units Ø, 1, and 2 respectively). The three separate acknowledge signals are combined into one signal by the Transfer Acknowledge Generator that drives the tri-stated MULTIBUS transfer acknowledge signal XACK/.

Each of the DATARAM transfer acknowledge signals exit the DATARAM Control Board via a dedicated pin on the P1Ø connector. From the P1Ø connector, the signals pass through the J1Ø connector to the D-cable connector and cable. The D cable is connected to the J2 connector on the interface card. XACK/, the MULTIBUS transfer acknowledge signal, exits the interface board via the MULTIBUS P1 bus.

VIDEO REPEATER

Each DATARAM outputs video data as parallel three-bit words. The data enters the interface via the same connectors and cables as the transfer acknowledge signals described above. The three sets of 3-bit words are re-transmitted by the video repeater and transferred to the MULTIBUS P2 bus. VIDØ(Ø)-VID2(Ø) (unit Ø data) are transported, via MULTIBUS P2, to the 5Ø/6Ø Hz TV Timing and Colorizer board. The remaining signals (units 1 and 2) are transported, via P2, to the 12-bit Dual Channel Colorizer.

DETAILED CIRCUIT DESCRIPTION

TV TIMING REPEATER

Refer to schematic diagram 645Ø-Ø379, dated 3/17/86. PXLCK, HORZDRV, VERTDRV, and OE are applied to differential line receiver AF37 sections A, B, C, and D respectively. Note that the OE minus and plus drive signals are applied to the AF37-D plus and minus inputs respectively. Thus, OE is inverted at AF37 pin 13 (D output). The four outputs of AF37 are applied to differential line driver AF12. Note that PXLCK is also applied directly to AD23, AH23, and AK23; it is applied indirectly via inverter AF27-A to AD12, AH12, and AK12. These components use PXLCK and PXLCK/, covered in the Video Repeater section.

MULTIBUS CONTROL REPEATER

MWTC/ and INIT/ are applied to octal line driver AB33, pins 17 and 15 respectively. Pin 19 enables the MWTC/ and INIT/ drivers at all times. The driver connected to pin 2 is enabled by pin 1 which is active low during a transfer acknowledge (see Transfer Acknowledge Generator below).

ADDRESS AND DATA BUS REPEATERS

The address bus is buffered and re-transmitted by octal line drivers Z7 and Z2Ø. The data bus is treated identically by Z33.

TRANSFER ACKNOWLEDGE GENERATOR

The unit transfer acknowledge signals XACKØ/, XACK1/, and XACK2/ (units Ø, 1, and 2 respectively) are applied to the differential line receivers AB12-A, -B, and -C respectively. The differential line

receivers convert the differential inputs to TTL outputs. The three outputs are applied to the inputs of AND gate AB23-B. Therefore, the output of the AND gate goes active low if any inputs go active low. The AND gate output drives one of the tri-state controls (pin 1) on tri-state line driver AB33. On this chip, the only driver used is controlled by pin 1 and has input pin 2 and output pin 18. Because the input is grounded, a low on pin 1 causes XACK/ to go low, informing the microprocessor that the requested read or write operation is completed.

VIDEO REPEATER

There is a separate video repeater for each of the three units. Because all three are identical, only unit Ø is discussed. VIDØ(Ø) (LSB), VID1(Ø), and VID2(Ø) are applied to differential line receivers AD1-A, -B, and -C respectively. The three TTL outputs of the line receivers are applied to D-latch AD12, which resynchronizes the video data with the rising edge of PXLCK/. The three output bits of AD12 are then applied to D-latch AD23, which resynchronizes the data with the rising edge of PXLCK. Finally, the outputs of AD23 are applied to the A, B, and C sections of differential line driver AD37. The line driver outputs are transported to the 5Ø/6Ø Hz TV Timing and Colorizer-Brooktree via the P2 bus.

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SECTION 8
DIGITAL JOYSTICK 2
TABLE OF CONTENTS

DIGITAL JOYSTICK 2

(SSEC DRAWING 645Ø-Ø521, DATED 11/19/86)

INTRODUCTION

The dual joystick module allows the user to maneuver a cursor symbol on the workstation monitor. It can also be used as a general I/O device. The joysticks provide analog voltages to the Digital Joystick 2 board. This board digitizes the four analog input voltages from the joystick module, converts the data to standard RS-232 levels, and serially asynchronously transmits this data to the Cursor Generator. From the Cursor Generator, the data is available to the microprocessor.

FUNCTIONAL DESCRIPTION

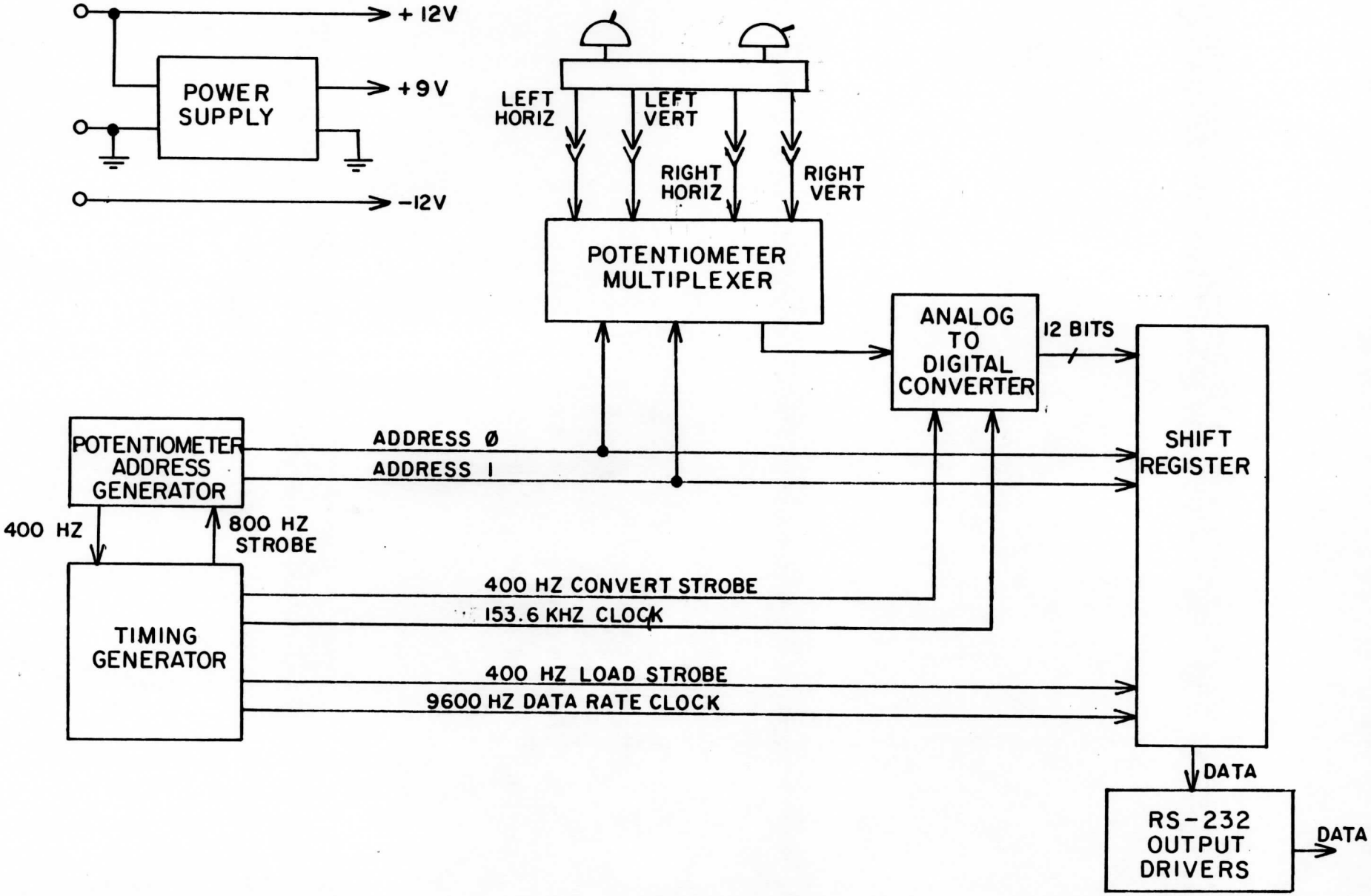
Figure 1 is a functional block diagram of the Digital Joystick 2 board. Movement of each joystick handle is sensed by two potentiometers (hereafter referred to as "pots"). One pot senses only the vertical component of the motion while the other senses only the horizontal. Diagonal motion creates inputs to both. There are two joysticks, so four pots are required to sense the positions of the handles. The outputs of the pots are sent to the pot multiplexer block of Figure 1. The pot multiplexer is an addressable analog switch. That is, each pot can be connected to the output of the multiplexer by applying the proper address.

The Timing Generator in Figure 1 produces three clock frequencies:

- 153.6-Khz output clock
- 4ØØ-hz control clock
- 96ØØ-hz data rate clock

For proper interpretation of the 96ØØ-baud serial output data, a clock signal 16 times the data frequency must be sent (153.6-Khz output clock). The 96ØØ-hz data rate clock is the source for all other timing; it includes an 8ØØ-hz strobe.

The Pot Address Generator uses the 8ØØ-hz strobe to produce a 4ØØ-hz clock. The 4ØØ-hz clock drives a counter that sequentially generates pot addresses for the Pot Multiplexer block.



DIGITAL JOYSTICK 2 FUNCTIONAL BLOCK DIAGRAM

FIG.-1

The Analog-to-Digital Converter converts the selected analog voltage to a 12-bit binary number and sends it to the Shift Register.

The Shift Register performs the following four functions:

1) latches the Analog-to-Digital (A-to-D) output data into the input registers
2) encodes the pot address and byte identification codes
3) formats the data for serial transmission
4) serially clocks the data out to the RS-232 Output Driver at a rate of 9600 bits/sec (baud)

The RS-232 Output driver convert the Data to standard RS-232 logic levels for asynchronous 9600-baud transmission.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the Digital Joystick 2 is shown on SSEC drawing #6450-0521 (dated 11/19/86). The schematic circuit analysis is accomplished by analyzing groups of components, represented by a single block in Figure 1 above.

SCHEMATIC CONVENTIONS

When reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and the letter designator. The symbol ID number alone is used to refer to single function ICs.

BAUD RATE GENERATOR

The Baud Rate Generator is composed of components, U7-A, U7-B, U8 and a 4.91520 MHz crystal. U8 is a 14-stage binary counter capable of producing various subsets of the fundamental crystal frequency of 4.91520 Mhz. By selecting the required outputs of U8, Q5 (pin 5) and Q9 (pin 12) provide the two output frequencies needed; they are 153.6 Khz and 9600 hz, respectively. The 153.6-Khz frequency (pin 5) is used to clock the A to D converter U1.

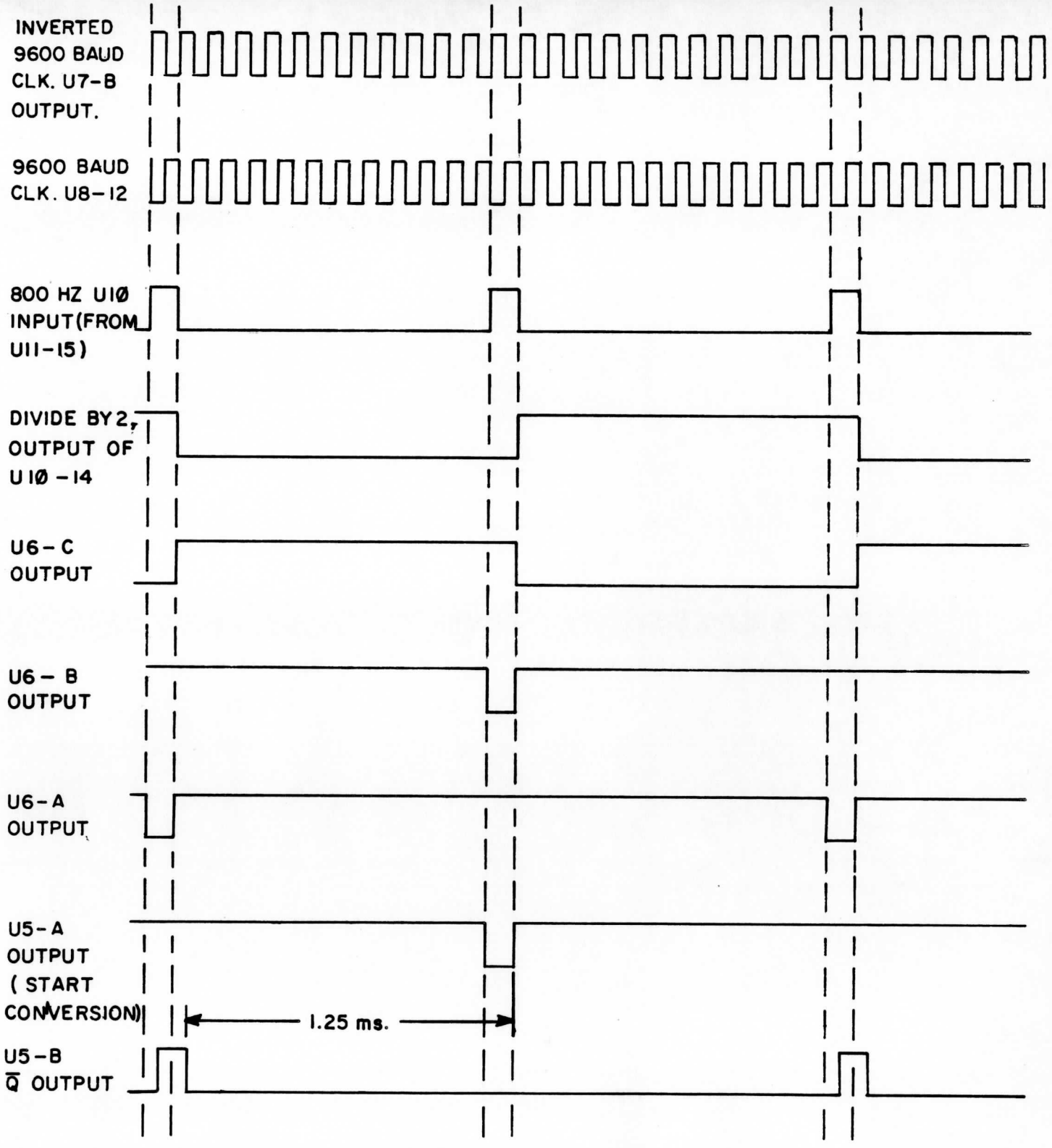
The 9600-hz frequency is inverted by a complimentary pair/inverter U7-B for increased drive and is used by the Pot Address Generator U10 to clock the data from the shift register and drive counter U11. U11 is a four-stage binary counter forced to divide the 9600-hz buffered input

clock by 12. This is accomplished by using the overflow pulse to generate a preset count of 4, thereby generating a 1Ø4-µsec positive pulse in synchronism with each 12th rising edge of the inverted clock (see Timing Diagram 1). This produces an 8ØØ-hz strobe pulse, used by the Pot Address Generator (U1Ø) and logic gates U6-B and U6-A. One output of the Pot Address Generator is a divide-by-two of the input 8ØØ-hz strobe, resulting in 4ØØ hz. The logic state of the divide-by-two counter toggles to its opposite state upon receipt of each 8ØØ-hz strobe pulse (see Timing Diagram 1).

The state of the divide-by-two counter is inverted by NAND inverter U6-C and applied, along with the 8ØØ-hz strobe, to NAND gate U6-B. When the output of the divide-by-two counter is a logic "zero" and the strobe is a logic "one" (see Timing Diagram 1), this results in a logic "zero" input to latch U5-A. The state of the divide-by-two counter and the 8ØØ-hz strobe are also applied to NAND gate U6-A (this time the divide-by-two output is <u>not</u> inverted). This results in a logic "zero" input to latch U5-B. When the output of the divide-by-two counter and the 8ØØ-hz strobe are a logic "one" (see Timing Diagram 1), the output of latch U5-A is applied to A-to-D converter U1. The inverted output from latch U5-B is applied to shift register U2, U3, and U4. These waveforms are shown in Timing Diagram 1. Note that the two output waveforms (U5-A and U5-B) are displaced from each other by 1.25 msec. The output of latch U5-A generates conversion strobes for A-to-D converter U1, while the output of latch U5-B generates load and shift strobes for the shift register. This allows the A-to-D converter to convert the analog data to digital data, and make the digital data available to the shift register while the shift register is outputting the previous data.

POT ADDRESS GENERATOR

The Pot Address generator is U1Ø, a divide-by-sixteen binary counter used as a divide-by-eight binary counter. As the counter counts the 8ØØ-hz input, it goes through a full cycle 1ØØ times per second. The pot address is taken from the QB and QC outputs (pins 13 and 12, respectively). Table 1 below shows how QB and QC change as a function of the 8ØØ-hz input. QB and QC select which Multiplexer input pot is applied to the



TIMING DIAGRAM 1

DIGITAL JOYSTICK 2 BOARD

(6450-0400)

A-to-D converter and supply pot address information to the shift register. During a counter cycle, each pot is selected and converted to digital data at a rate of 1ØØ times/sec.

Table 1

Pot Address State Table

QC	QB	QA	Pot	A to D	Shift Reg
Ø	Ø	Ø	right	convert	load
Ø	Ø	1	vert	load	shift
Ø	1	Ø	right	convert	load
Ø	1	1	horiz	load	shift
1	Ø	Ø	left	convert	load
1	Ø	1	vert	load	shift
1	1	Ø	left	convert	load
1	1	1	horiz	load	shift

POT MULTIPLEXER

The Pot Multiplexer is U9, an AD75Ø3 circuit. This circuit, an eight-input analog multiplexer, is configured as a four-input device by grounding the high four inputs and the MSB address line. The Joystick module voltage outputs (-3v to +3v) are applied via J2 (pins 1, 2, 3, and 4) to U9 (pins 13, 11, 1Ø, and 9, respectively).

Addressing inputs from the Pot Address Generator are applied to U9 pins 16 (LSD) and 1 (MSD). The selected output is applied to the input of the A-to-D converter U1. Note that each input to the multiplexer is filtered for noise reduction by a simple despiking capacitor (C1, C2, C3, C4).

ANALOG-TO-DIGITAL CONVERTER (A-TO-D)

The Analog-to-Digital Converter (A-to-D) comprises U1 and associated discrete components (all capacitors are used for decoupling and noise reduction). U1 is a 12-bit, successive-approximation, A-to-D converter. The circuit requires the application of a clock and internal voltage reference for proper operation. The circuit requires a negative pulse at the start conversion pin (13) to initiate or arm the conversion cycle. The conversion does not begin until the falling edge of the convert pulse. The start conversion input (pin 13 - active low), when taken low, causes

the register to reset synchronously on the next 153.6KHz clock low-to-high transition. The register remains reset until the start conversion input is taken high (approx. 104 µsec). When start conversion goes high, the conversion process begins on the next low-to-high transition of the clock pulse. This process continues until the LSB (Q_0) is found. A complete conversion requires only 1ØØ µsec. Thus, all digital outputs are at their correct state 1ØØ µsec after the falling edge of the convert pulse. During the 1Ø4-µsec positive portion of the convert pulse, the converter is armed. During the first 1ØØ µsec of the 2396-µsec rest period, conversion takes place and data is presented to the shift register.

SHIFT REGISTER

The Shift Register comprises U2, U3, and U4. Each of these three ICs is an eight-bit, parallel-input, shift register. When the P/S pin (pin 9) is high, parallel data is loaded into the registers. When pin 9 is low, data is shifted serially out of the registers (LSB bit first) by the 96ØØ-hz inverted clock. Note that the output from U3 shifts into the input of U4 and the output from U4 shifts into the input of U2.

Twelve data bits from the A-to-D converter, two bits of pot address encoding, and two bits of character identifier must be formatted for serial asynchronous RS-232 transmission (16 data bits total).

The data bits are loaded into the three 8-bit shift registers (U3, U4, and U2) along with the start, stop, and parity bits required by RS-232 receiving hardware on the Cursor/Joyboard and Graphics Tablet board. The start, stop, parity, and character identifier bits are hard-wired by grounding or strapping the appropriate shift register inputs to +5 volts. One start bit and two stop bits are standard RS-232 convention; however, the parity bits are used only as a filler and are ignored on the receiving end (always transmitted as a high). The pot address information is applied to U4 pins 6 and 7. Table 2 below summarizes the conditions of U3, U4, and U2 after a register load has been performed.

The data is shifted out of the shift registers, one bit at a time, by the 96ØØ-hz data rate clock. Note that four sets of loads and shifts are required to transmit the positions of all four pots.

Table 2

Shift Register Data Format

U3								U4								U2								
PØ	P1	P2	P3	P4	P5	P6	P7	PØ	P1	P2	P3	P4	P5	P6	P7	PØ	P1	P2	P3	P4	P5	P6	P7	
1	1	1	D	D	D	D	D	D	D	1	Ø	1	1	1	D	D	D	D	D	D	D	Ø	Ø	*value
SP	SP	P	D	D	D	D	D	AD	AD	ID	ST	SP	SP	P	D	D	D	D	D	D	D	ID	ST	**function
2nd character								1st character																

* 1 = high, Ø = low, D = variable
**ID = identification, Ø = 1st character, 1 = 2nd character
ST = start
SP = stop
D = data
AD = address
P = parity

RS-232 OUTPUT DRIVERS

U12-A is an RS-232 line driver. The line drivers convert the logic levels from U2 pin 3 to RS-232 levels (via CMOS inverter U7-C and current source inverter U14). A high input causes an output of approximately -1Ø volts and a low input causes an output of approximately +1Ø volts output.

POWER SUPPLIES

The power supply requirements for this board are provided from the cursor generator board via the J2-J3 connectors of the digital joystick board. The voltages provided are +12V, -12V, and ground reference levels. A 78LØ9 +9 volt regulator U13 is used to convert the +12V to +9V required in the RT and LT vertical joystick potentiometers and the +V reference to the A-to-D converter.

4/PCAT/08

SECTION 9
PAL (NTSC) TV SYNC BOARD
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PAL/NTSC TV SYNC BOARD
(SSEC DRAWING 6450-0492, MODIFICATION C, DATED 6-27-86)

INTRODUCTION

The PAL/NTSC TV Sync board has two purposes; it provides the TV Sync signal necessary for PAL/NTSC encoders, TV cameras, recorders, and other TV equipment, and it provides pixel clock and sync reset signals to synchronize the 5Ø- or 6Ø-Hz TV Timing and Colorizer Board circuits. The following are operating modes:

- internally-generated sync and color sub-carrier signals
- strapped control of PAL or NTSC mode of operation
- externally-generated color sub-carrier signal

The sub-carrier and other sync and clock signals used by the PAL/NTSC TV Sync Board are approximately equal to those specified by the NTSC and PAL standards. Some slight differences result from these approximations; however, color television system synchronization circuits generally are designed to ignore such slight variations with system operation occurring as normal. The functional and detailed description of this board's operation will be discussed with reference to the NTSC mode of operation. All signal frequences will be given for NTSC mode with PAL mode values following in parenthesis; ex: 3.5795 Mhz (4.4336 Mhz).

FUNCTIONAL DESCRIPTION

Refer to Figure 1, the function block diagram of the PAL/NTSC TV Sync board. All signals generated by this unit are either a multiple or submultiple of either a 3.579545-Mhz or 4.433619-Mhz reference frequency. The frequency depends on the mode of operation, either PAL or NTSC. This reference frequency is generated internally by a high-quality, temperature-compensated crystal oscillator (TXCO).

The reference frequency is divided by five (nine) to produce a 715.9-Khz (492.6-Khz) reference for a phase-locked loop. The phase-locked loop produces the 12.886-Mhz (12.8Ø8-Mhz) pixel clock by multiplying the

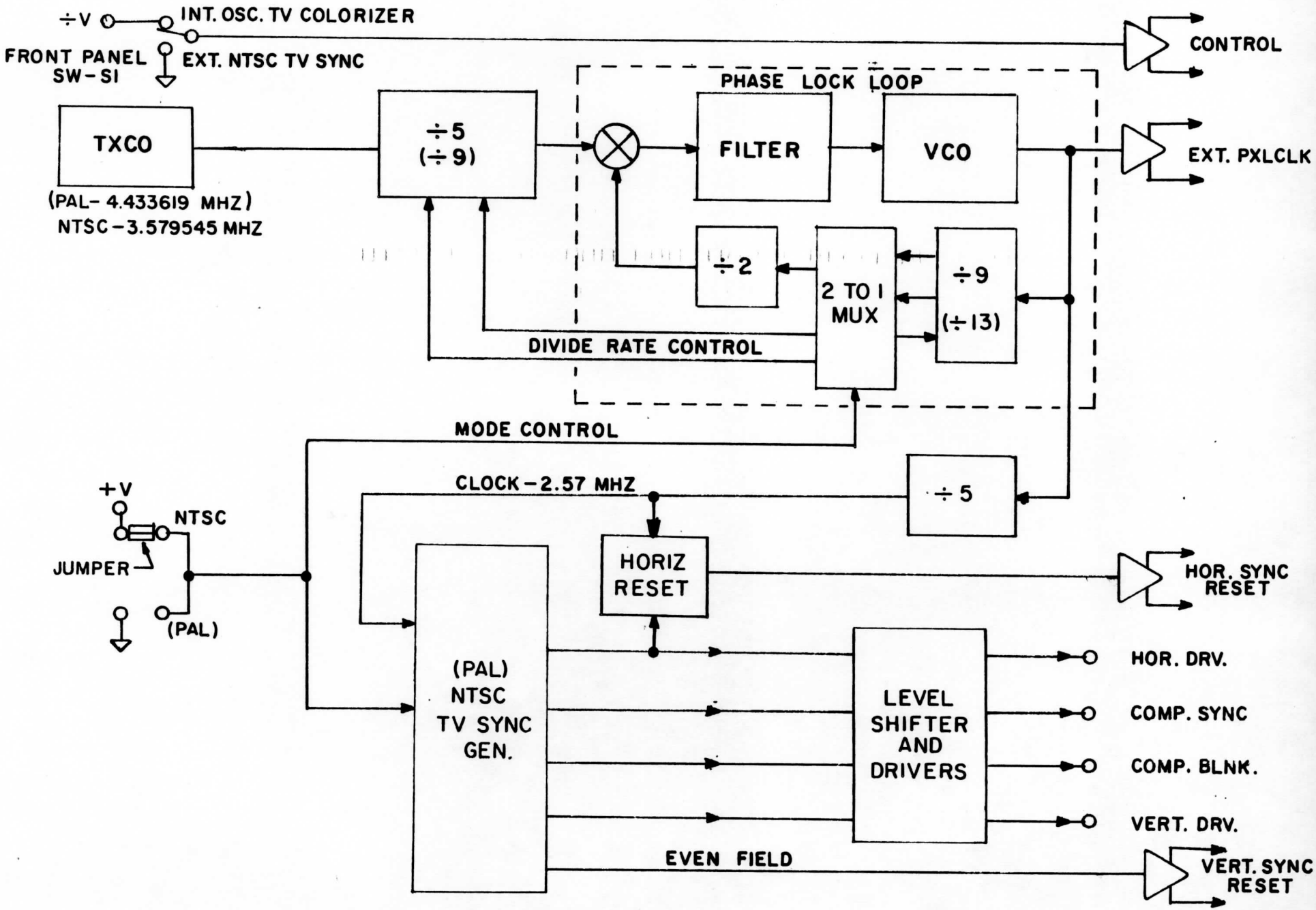


FIGURE - 1

PAL/NTSC TV SYNC UNIT FUNCTIONAL BLOCK DIAGRAM

(6450-0492)

reference frequency by 18 (26). Also produced are 2.583-Mhz (2.5625-Mhz) clocks for use by the NTSC TV Sync Generator block, by dividing the pixel clock frequency by five. The following five blocks constitute the phase-locked loop:

- Phase Comparator (digital)
- Filter
- Voltage-Controlled Oscillator (VCO)
- Divide-by-nine (13) block
- Divide-by-two block

The Phase Comparator compares the 715.9-Khz (492.6-Khz) reference signal to pixel clock divided by 18 (26) 715.9-Khz (492.6-Khz). If there is a difference in frequency or phase, the Phase Comparator produces a DC error voltage. The Filter smoothes the noisy DC error output from the Phase Comparator. The Voltage-Controlled Oscillator (VCO), a DC-controllable oscillator, has a natural frequency of about 12 Mhz. The DC error input to the VCO forces it to operate at exactly 12.88636 Mhz for NTSC (12.8Ø8 Mhz for PAL). The Divide-by-nine (thirteen) and Divide-by-two blocks, together, form a divide-by-18 (26) block. If the VCO drifts off frequency, the output from the divide-by-18 (26) block is no longer 715.9 Khz (492.6 Khz). The Phase Comparator output shifts in the appropriate direction (up or down) to pull the VCO back on frequency. The output is applied to a line driver for output to the McIDAS workstation (TV Timing and Colorizer board).

The 2.583-Mhz (2.5625-Mhz) output from the Divide-by-five block is a clock input to the NTSC TV Sync Generator block. This block is a single IC chip, containing the necessary dividers and logic to produce all of the standard TV sync signals from the single clock input.

The NTSC (PAL) TV Sync Generator block outputs the following signals:

- Composite Sync
- Composite Blanking
- Vertical and Horizontal sync resets
- Vertical Drive
- Horizontal Drive

These signals are applied to the Level Shifters and Drivers block which directly drives the rear-panel-mounted BNC output connectors. Composite Sync, Composite Blanking, and the Internal Color Subcarrier Output signals

drive an NTSC Encoder Unit that combines these signals with the Red, Blue, and Green video drive signals to produce the NTSC monitor drive signal.

The Reset Generator block provides a generator lock ("gen lock") synchronizing pulse to the TV Timing and Colorizer board. This signal's purpose is explained in detail in the TV Timing and Colorizer description. Essentially, however, the TV Timing and Colorizer board has a sync generator chip identical to the NTSC (PAL) TV Sync Generator chip. When using the NTSC (PAL) Sync Generator as the system master timing generator, you must replace the TV Timing and Colorizer board's internally-generated pixel clock (PXLCK) with the pixel clock output from the PAL/NTSC TV Sync Board. You must also synchronize the vertical and horizontal drive signals. The drive signal synchronization is accomplished by locking the TV Timing and Colorizer generator chip to the PAL/NTSC TV Sync Board generator. To do this, you must generate a sync pulse to occur at the rate and time necessary to synchronize the TV Timing Unit. This pulse must occur at approximately the sixth horizontal scan after the beginning of the even field vertical drive pulse.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the PAL/NTSC TV Sync Board is shown on SSEC drawing #645Ø-Ø492 (Modification C dated 6/27/86). The schematic circuit analysis is accomplished by analyzing groups of components, represented by a single block in Figure 1 above.

SCHEMATIC CONVENTIONS

When reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and the section letter designator. The symbol ID number alone is used to refer to single section ICs.

MODE CONTROL MULTIPLEXER

Refer to sheet 1 of the schematic diagrams. The PAL/NTSC TV Sync Board is designed to operate in one of two modes: PAL -- a European TV standard and NTSC -- the US TV Standard. The circuit board jumper strap option is used to select the mode of operation, either PAL or NTSC.

The mode strap has a dual function, control of quad two line to one Multiplexer (MUX) AG36 (74LS157) and mode control of TV sync generator

BC22 (Ferranti ZNA134). The MUX sets the division rate of various multi-state counters used throughout the board. The mode strap places a logic level (zero for PAL, or one for NTSC) at the input of inverter/driver AE39-A (74LSØ4). The inverted output drives the select line of MUX AG36 as well as the 5Ø Hz or 6Ø Hz mode select input to the TV Sync Generator chip BC22. The MUX has four sets of inputs of which three are tied to grounds or pull-ups. The 1A, 2B, and 3B inputs are tied high, while the 1B, 2A, and 3A inputs are tied low. The 4A and 4B inputs are connected to the most significant bit's output of variable division rate counter AE28 (74LS169). When the strap is connected for PAL mode, a logic zero is inverted by AE39-A and a high level is placed on the select input of AG36. A logic one selects the B inputs to be passed to the Y outputs of the MUX. Conversely, in NTSC mode a low logic level is presented to the select input passing the A inputs to the Y outputs.

The MUX output lines route logic levels or clocking signals to various counters throughout the board. These signals control the preset inputs that determine the counter's division rates. The action of the variable rate counters is discussed in detail later. The clocking data passed through section four of the MUX is passed to a divide-by-two counter; the counter conditions the symmetry and phase of the variable rate clock. This signal is then passed to the VCO input of phase comparator AC12 (MC4044).

TXCO OSCILLATOR

Refer to Sheet 2 of the schematic diagrams. The color sub-carrier (CSC) signal is generated by a temperature-compensated, chassis-mounted, crystal-oscillator (TXCO) module. The 3.579545-Mhz (4.433619-Mhz) reference signal is approximately 2.Ø V peak-to-peak (p-p) in amplitude, and is RC-coupled to voltage amplifier BG4Ø (LM318); BG4Ø provides a 4.Ø V p-p output signal. The output of BG4Ø is applied to the input of current amplifiers BG3 and BG12. The output impedance of BG3 and BG12 (LHØØØ2), in series with a 68-ohm registor, is approximately six ohms.

Together, these two resistances form a 75-ohm output impedance that drives the 75-ohm "INT CSC OUT" and CSC encoder lines at approximately 2.Ø V p-p when terminated into 75 ohms.

DIVIDE-BY-FIVE/NINE

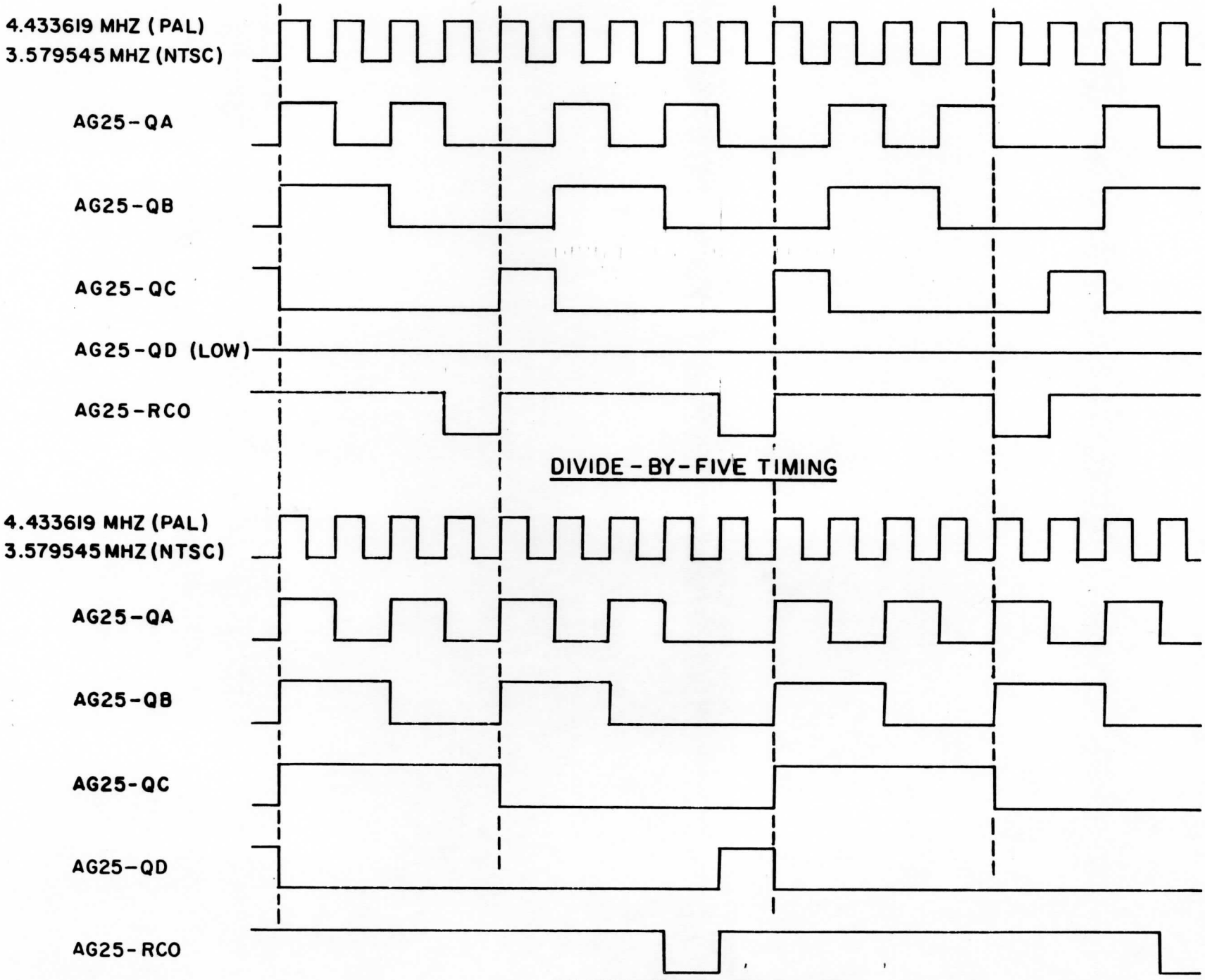
The PAL/NTSC modes have separate CSC signal frequencies, therefore separate frequency division rates must be used to develop the PIXEL CLOCK and synchronizing frequencies generated by the board.

The output of current amplifier BG3 is applied to line receiver AG16 (26LS33), which converts the CSC signal from a sine wave to a square wave. The potentiometer (AJ1Ø) controls the symmetry of the square wave output. The line receiver output is used as a clock by AG25 (74LS169), a 4-bit binary counter that can be switched between divide-by-five and divide-by-nine circuits.

AG25 is wired as a down counter; the counters preset inputs are either hardwired or controlled by MUX AG36 (74LS157). The MUX functions as the board's PAL/NTSC mode controller. In PAL mode, AG36 places a low level on the C data preset to counter AG25 and a high level on the D data preset. In the NTSC mode, the C and D data preset states are the converse of the above. AG25 is preset to ØØØ1B (eight) in PAL mode and preset to ØØ1ØB (four) in NTSC mode. The counter's ripple carry output (RCO) is wired back to the load input. Refer to Timing Diagram 1. Because the counter features a synchronous load, either four or eight clock cycles count the device down to ØØØØB and produce a ripple carry (underflow). The counter does not actually preload again until the fifth or ninth clock pulse arrives. Therefore, depending on mode, the counter divides by five or nine. Pin 12 of AG25, the QC output, drives the phase-locked loop phase comparator reference input. It is not important that the QC output is nonsymmetrical, because the phase comparator is sensitive only to the signal's negative-going edges.

PHASE COMPARATOR

The Phase Comparator is AC12, a Motorola MC4Ø44B circuit. This circuit consists of three parts: a digital phase comparator, a charge pump, and a darlington amplifier. The reference 715.9-Khz (492.6-Khz) signal is applied to the "RC" (pin 1) input of the Phase Detector while the VCO signal is applied to pin 3 (y_1). There are two outputs from the comparator, a pump-up output and a pump-down output. The comparator section is designed so that both outputs are high when the input phases are exactly equal. If the VCO input lags in phase, active low pulses



TIMING DIAGRAM-1 PAL/NTSC TV TIMING

appear at the pump-up output (pin 13). The width of these pulses increase with an increase in phase difference until a maximum of 5Ø% duty cycle is reached (18Ø° phase difference). If the VCO output leads in phase, the pump-down output (pin 2) performs exactly as the pump-up output during a phase lag. The pump-up and pump-down outputs are coupled to the charge pump inputs by connecting pin 13 to pin 4 (pump-up input of the charge pump) and connecting pin 2 to pin 11 (pump-down input of the charge pump).

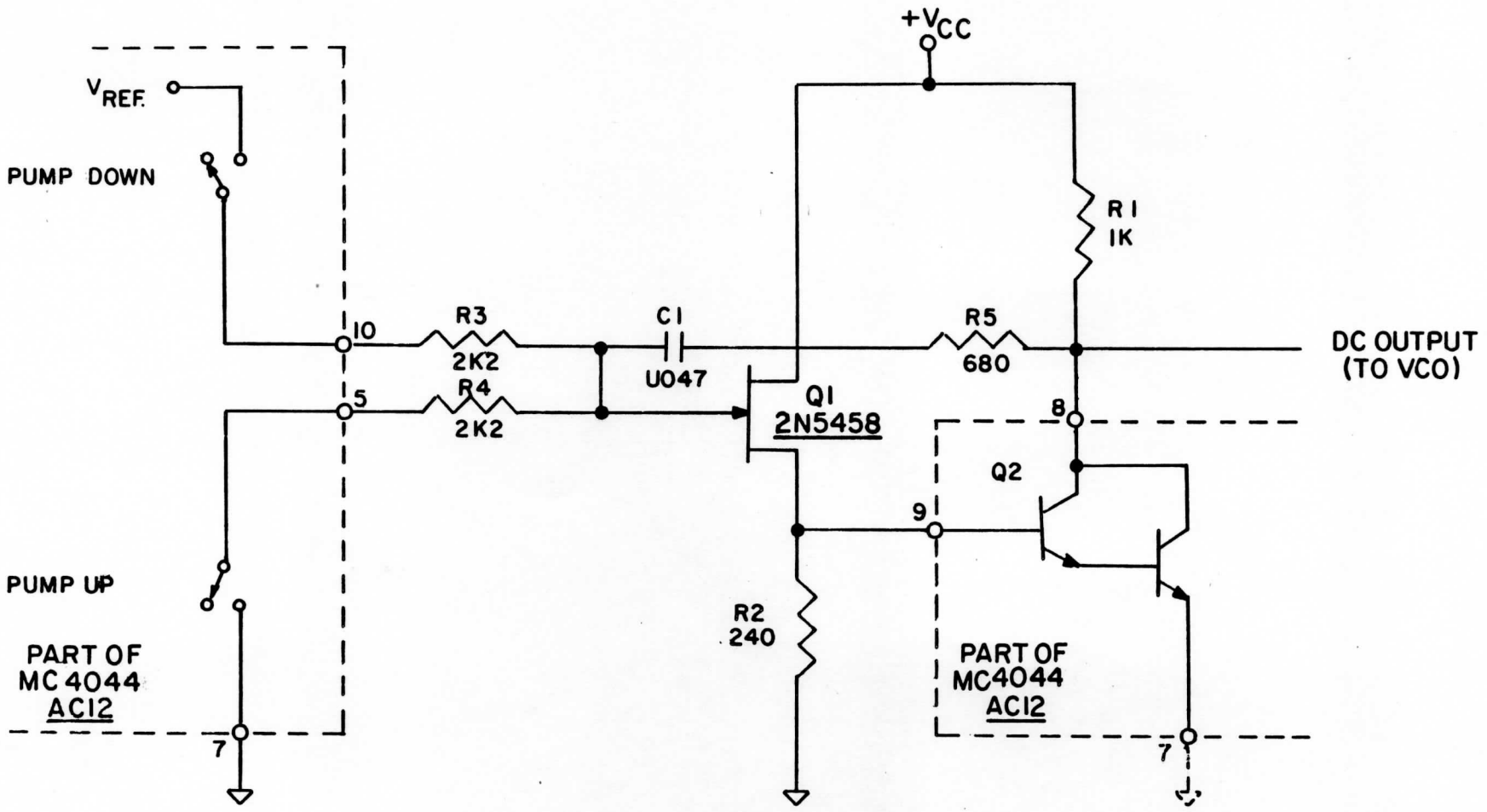
The charge pump consists of two electronic switches. A logic high at the charge pump inputs opens the switches. The pump-up switch connects ground and resistor AC22 (2.2-K ohm connected to pin 5), while the pump-down switch connects an internal voltage source and resistor AC23 (2.2-K ohm connected to pin 1Ø). These resistors are part of the Filter block discussed in the next paragraph.

FILTER

Figure 2 was redrawn from SSEC drawing 645Ø-Ø492 and the MC4Ø44B schematic diagram. The circuitry in Figure 2 functions as a Miller integrator or low-pass active filter. The value of C_1 is effectively multiplied by the very high beta of Q_2. If the pump-up switch is closed (VCO has lagging phase), a charge path for C_1 is completed from ground through R_4, C_1, R_5, R_1, and VCC. The charge current for C1 flows through R_4, making the junction of R_4C_1 positive (with respect to ground). This positive voltage is amplified by Q_1, a junction Field Effect Transistor (FET), operating as a source follower. The positive-going output of Q_1 is applied to a darlington, common-emitter amplifier Q2, resulting in a decrease in collector voltage. The collector output of Q2 is coupled back to the gate of Q_1, via R_5 and C_1, as a negative feedback, cancelling nearly all the original input. This results in a very low charge current for C_1 and a very long time constant. When the pump-down switch is closed, the capacitor attempts to discharge through Q_2 to ground, causing the collector of Q_2 to decrease in voltage. In summary, a lagging VCO phase results in an increasing voltage at Q_2's collector. Conversely, a leading VCO phase results in a decreasing voltage at Q_2's collector.

VCO

The VCO is AE19 (74S124), a dual, TTL, voltage-controlled oscillator. The oscillator's base frequency is established by the variable capacitor



PHASE COMPARATOR FILTER SCHEMATIC

FIGURE -2

(6450-0492)

soldered between pins 4 and 5. Pin 3 is the range control for the VCO and is connected to a decoupled +5 volt supply, yielding maximum range. The DC error voltage output from the filter is applied to pin 2 as the control voltage. The output from pin 7 is a symmetrical 12.88636-Mhz (12.80823-Mhz) square wave and is applied to differential line driver AE3-B (26LS31). AE3-B provides the differential NTSC pixel clock drive for the TV Timing and Colorizer board. The pixel clock is also applied to 4-bit synchronous up/down counter AE28 (74LS169), and 4-bit binary counter BA3 (74LS163) (located on page 2 of the schematic diagrams).

DIVIDE-BY-NINE/THIRTEEN

The 4-bit synchronous up/down binary counter AE28, is wired as a divide-by-nine or thirteen circuit. The division rate of the device is controlled by the PAL/NTSC mode strap and MUX AG36. The input data preset C line of AE28 is set by the 3Y output of AG36. In NTSC mode, 3Y outputs a logic zero. Conversely, in PAL mode, 3Y outputs a logic one to the data C preset of counter AE28. The A and B data presets are hardwired to a pull-up. Therefore, the counter preset condition for NTSC mode is 1ØØØB (eight), and for PAL mode is 11ØØB (twelve).

The counter operates similarly to the other multiple-divide device (AG25) discussed earlier. The clocking input to AE28 is the PIXEL CLOCK output of the VCO at a frequency of 12.886 Mhz (NTSC) or 12.808 Mhz (PAL), depending on the TXCO used to generate the CSC signal.

Because the counter divides by either of the two rates, the output's most significant bit must be decoded for each specific division rate. The QC and QD outputs of AE28 are applied to the mode controller AG36, pin 14 and pin 13, respectively. Again, the PAL/NTSC mode switch setting determines which of these inputs is multiplexed through to the 4Y output (AG36 pin 12). The 4Y output is the PIXEL CLOCK signal, divided by nine for NTSC operation or thirteen for PAL operation.

DIVIDE-BY-TWO

The divided PIXEL CLOCK signal from AG36 pin 12 (4Y) is applied to the clocking input of D-type flip-flop AC3Ø (74LS74). Both the preset and clear lines are tied to a pull-up. The Q/ output of AC3Ø is fed back to the D input. AC3Ø performs a divide-by-two operation on the already

divided PIXEL CLOCK signal. The PIXEL CLOCK signal is divided in two blocks to simplify circuit design and reduce signal phase jitter through the phase-locked loop. The Q output is a symmetrical square wave that is either the PIXEL CLOCK divided by 18 (NTSC mode) or by 26 (PAL mode). The output of this block is applied to the VCO input of the phase comparator (AC12 pin 3).

NTSC TV SYNC GENERATOR

The NTSC TV Sync Generator is chip BC22 (Ferranti ZNA134). This chip provides all of the basic sync functions for either color or monochrome 525 line/60-hz or 625 line/50-hz interlaced camera and video recorder applications.

The chip divides the clock input by 164 to produce the horizontal drive frequency of 15,750 (15,625 hz). The vertical drive frequency is generated by dividing the horizontal frequency by 262.5, resulting in a vertical drive frequency of 59.94 hz. All remaining output signals from this chip are composites of these two frequencies. For further information on this device, refer to a Ferranti Semiconductor MOS/CCD data book.

DIVIDE-BY-FIVE

Refer to sheet 2 of the schematic diagrams. The divide-by-five circuit is made up of 4-bit binary counter BA3 (74LS163) and BA12-A (74LS00). The clocking input to BA3 is the PIXEL CLOCK generated by the VCO (AE19). The counter is preloaded with a count of two by NAND gate BA12-A. BA12-A is qualified by a counter output of 0110B (six), because the QB and QC counter outputs are used. It takes four counts to qualify the output of BA12-A, but the counter (74LS163) has a synchronous load feature so it does not preload until the next clock pulse input. The output frequency, taken off the QC output of the counter, is 2.5625 Mhz (PAL) or 2.583 Mhz (NTSC). The output frequency is applied to the TV Sync generator BC22-pin 8. The divide-by-two (QA) output of the counter is used to pass a PIXEL CLOCK/2 signal to synchronize the horizontal reset generator circuit.

LEVEL SHIFTERS AND DRIVERS

Except for the EVEN FLD (pin 14) output of the PAL/NTSC TV Sync Generator chip, all outputs are inverted by sections of hex inverter BC14

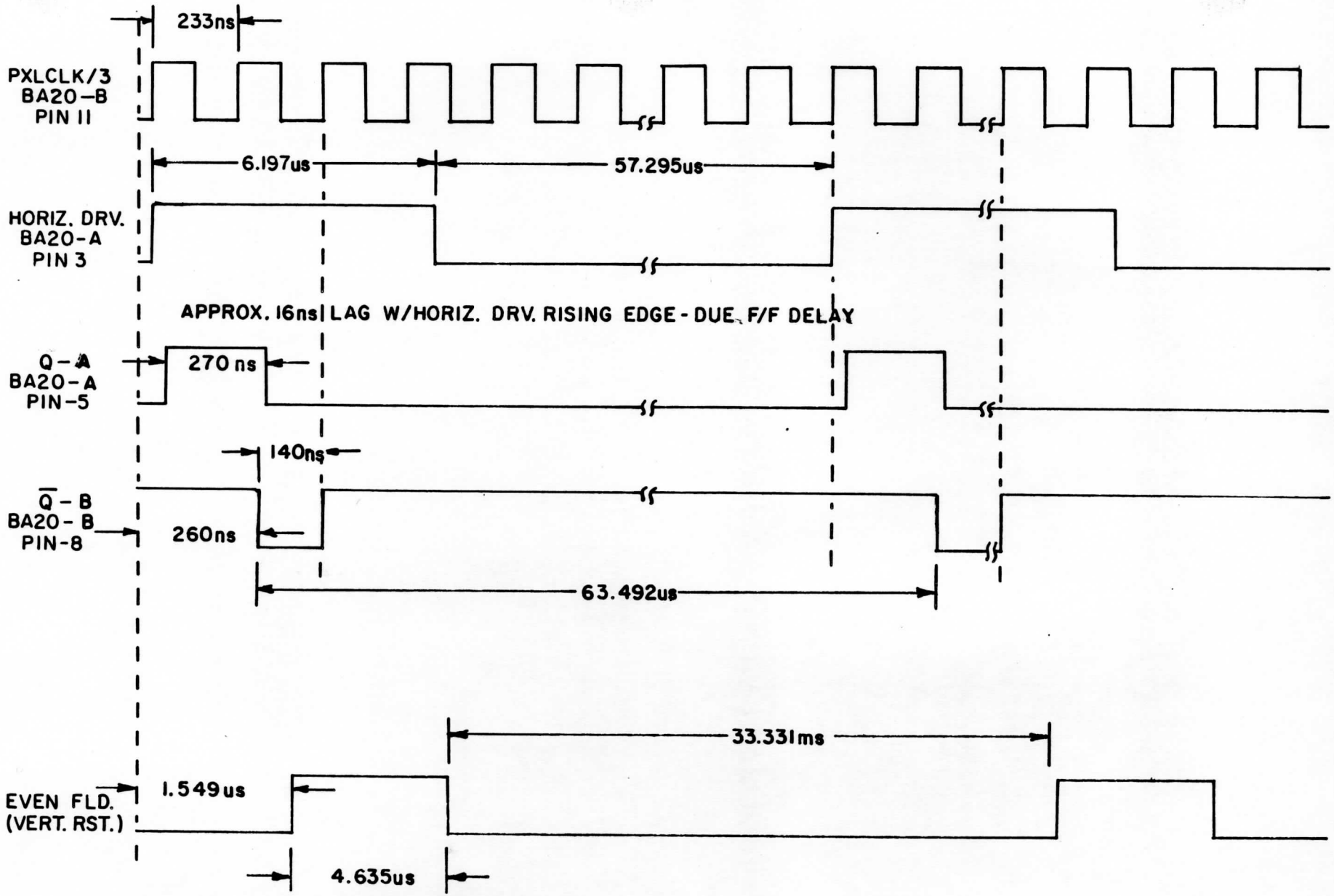
(74LS04) and applied to dual, 2-input, NAND-gate, TTL-to-MOS voltage shifters (BC4 and BE4). Each output of the sync generator chip drives both inputs of a single NAND gate. Composite Sync output and Horizontal Drive are shifted by BC4, Composite Blanking and Vertical Drive are shifted by BE4 (both DHØØ34). Because the NAND gates invert the signals that were already inverted by the hex inverter, the outputs of the NAND gates are in phase with the outputs of the Sync generator chip. A logic "one" at the output of the shifters is approximately Ø.Ø volts and a logic "zero" is approximately -7.5 volts.

RESET GENERATOR

The horizontal reset generator circuit is composed of dual D-type flip-flop BA2Ø (A and B). BA2Ø-B (74LS74) is wired to an asynchronous clear condition with its preset and clear inputs tied to a pull-up. The flip-flop receives its data from the Q output of BA2Ø-A. The clocking input to BA2Ø-B is a submultiple of the PIXEL CLOCK frequency provided by the QA output of divide-by-five counter BA3. The Q/ output of BA2Ø-B is fed back as the asynchronous clear and data inputs to the second half of the reset generator, BA2Ø-A. The clocking signal to BA2Ø-A is the inverted Horizontal Drive pulse provided by the TV sync generator chip BC22.

Refer to Timing Diagram 2. The static condition of the circuit is as follows: the data input to BA2Ø-A is a logic high level due to the Q/ output of BA2Ø-B being cleared by the PIXEL CLOCK. The Q output of BA2Ø-A is a logic zero also sensed on the D input of BA2Ø-B. Because the PIXEL CLOCK occurs at a rate about 41Ø times the horizontal drive clock, the B sections of the two flip-flops initiate the development of the reset pulse.

On the positive-going leading edge of the PIXEL CLOCK flip-flop, BA2Ø-B is toggled, setting up the circuit action. No action occurs until the first horizontal drive pulse arrives at the clocking input of BA2Ø-A. On the positive leading edge of the pulse, the Q output of BA2Ø-A toggles from low to high, placing a high at the D input of BA2Ø-B. At the rising edge of the next PIXEL CLOCK this positive to negative going edge causes a reset (clear) condition on BA2O-pin 1 and immediately clears the Q output, BA2O-pin 5. The pulse output of pin 5 was initiated by the horizontal



NOTE: ALL TIMING VALUES SHOWN ARE FOR NTSC MODE.

TIMING DIAGRAM -2 RESET TIMING GENERATION
(6450-0492)

drive pulse and terminated by the clear to BA20-pin 1, this results in a positive-going pulse of approximately 27Ø ns at a repetition rate of 15.75 khz (the horizontal drive pulse rate). On the next PIXEL CLOCK the two flip-flops (BA2Ø-A and -B) are set to the static condition described previously, awaiting the next horizontal drive pulse needed to generate another horizontal reset signal.

The vertical reset pulse is the EVEN FIELD output from the TV Camera Sync generator chip BC22. The EVEN FIELD output pulse is an active high pulse of 4.63 µsec occurring at a 3Ø-hz rate. This pulse signals the beginning of a new picture (the odd and even frames).

Refer to sheet 1 of the schematic diagrams. The horizontal and vertical reset sync pulses, along with the PIXEL CLOCK and PXLCK control signal, are exported to the TV Timing and Colorizer board via the J1 connector and differential line drivers AE3-A through D (26LS31).

4/PCAT/09

SECTION 10
PAL/NTSC ENCODER BOARD
TABLE OF CONTENTS

PAL/NTSC ENCODER BOARD
(SSEC DRAWING 645Ø-Ø494, MODIFICATION B, DATED 2/13/87)

INTRODUCTION

The PAL/NTSC Encoder board is used to generate a TV composite color video signal. The encoder's input signals are the red, blue, and green (RGB) color drive signals from the 5Ø/6Ø-hz TV Timing and Colorizer board; the sync input, color subcarrier, and power come from the PAL/NTSC TV Sync Board. The video output is a fully implemented, top quality, composite signal with performance levels virtually equal to high-cost, studio equipment.

FUNCTIONAL DESCRIPTION

Refer to Figure 1, the functional block diagram of the PAL/NTSC Encoder. The PAL/NTSC encoder board shares the chassis with the PAL/NTSC TV Sync Board. The inputs to the encoder board are via the BNC connectors on the back panel (R, G, B) or are directly from the TV sync board (sync, power, and color subcarrier). The encoder printed circuit board is quite simple in design; it consists primarily of several high-speed op-amps for signal conditioning and the PAL/NTSC encoder chip manufactured by Motorola Semiconductor Products, Inc.

The PAL/NTSC Encoder Board receives its power from the TV Sync Board ±12V DC supply. The five signal inputs to the encoder are the RGB color drive signals, the Color Sub Carrier (CSC), and the composite sync signal (SYNC). The board's single output is the 75-ohm Composite Video drive signal, which can be used to drive an NTSC device.

The RGB video inputs are amplified and shifted to specific DC levels required by the PAL/NTSC encoder. The composite sync signal is also shifted to a specific DC voltage before it is applied to the encoder chip. A strapped Mode Control input to the encoder is used to choose between PAL and NTSC operation.

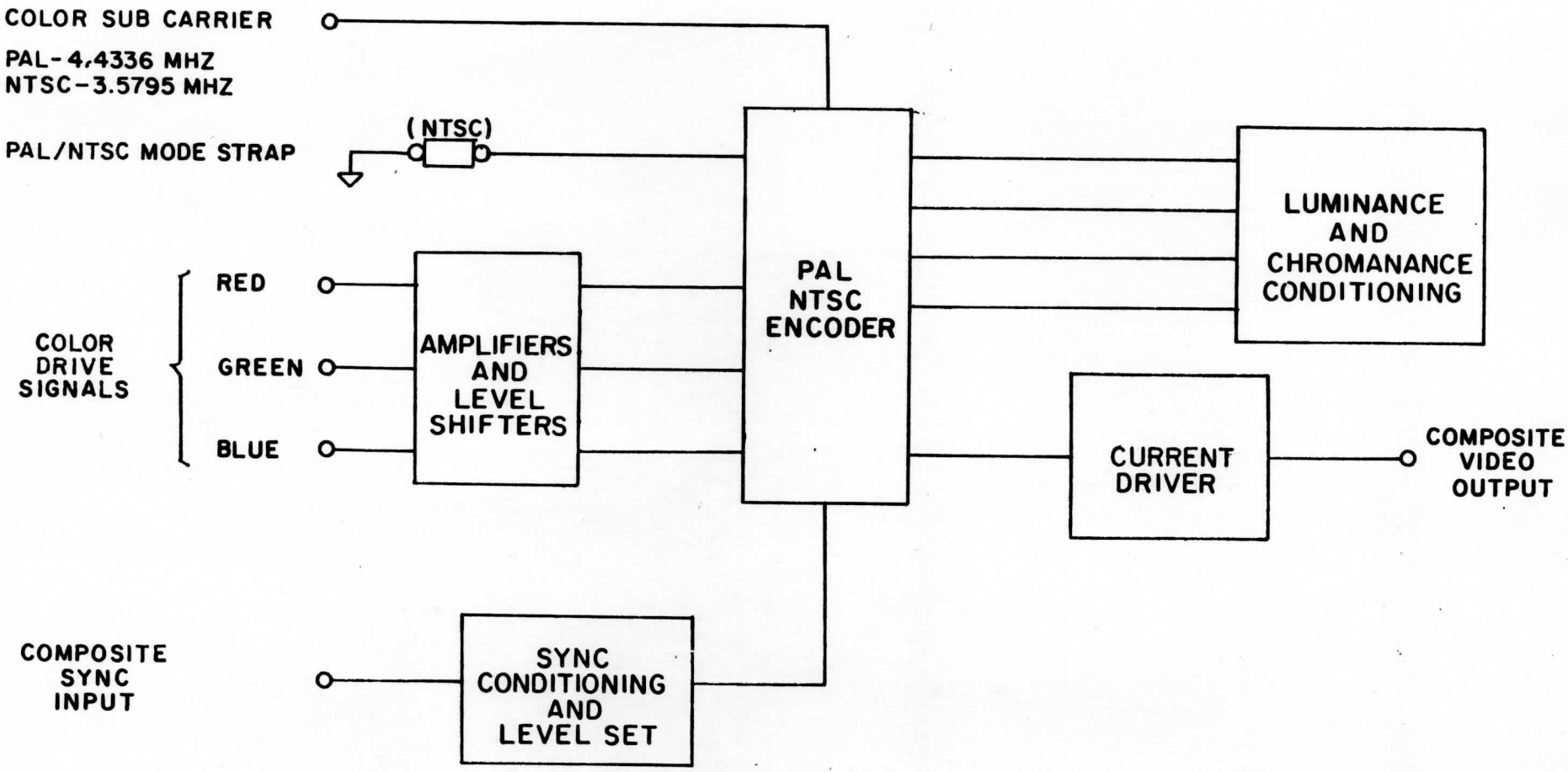


FIGURE - 1

PAL/NTSC ENCODER BOARD FUNCTIONAL BLOCK DIAGRAM

(6450-0494)

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of the PAL/NTSC Encoder Board is shown on SSEC drawing #645Ø-Ø494 (Modification B, dated 2/13/87). The schematic circuit analysis is accomplished by analyzing groups of components, represented by a single block in Figure 1 above.

SCHEMATIC CONVENTIONS

When reference is made to a schematic circuit symbol of a multiple device, the symbol ID is used, followed by a hyphen and the section letter designator. The symbol ID number alone is used to refer to single section ICs.

Color Drive Amplifiers

The red, green, and blue color drive signals are applied to individual high-speed Operational Amplifiers (OP-AMP), IC1, -2, and -3 (LM318's), via a coupling capacitor and DC level set circuitry. Through careful selection of components, the OP-AMP circuits used in this section provide a slight gain and set a specific DC bias level on their outputs. This fulfills input considerations required by the encoder chip.

The red video signal is coupled through C2, a 15 µf capacitor, which helps to prevent signal tilt during the 5Ø- or 6Ø-hz vertical period. Resistors R3 and R4 set up a DC bias level to the input of IC1, an LM 318, high-speed, OP-AMP circuit. The OP-AMP is configured as an non-inverting circuit with a gain of approximately 1.43. The gain figure is required to boost the Ø.7V drive signal to a 1.ØV level that is required by the encoder chip. Resistors R9 and R1Ø associated with IC1 determine the circuit gain and, along with R3 and R4, set up the static DC bias levels of approximately 3V required by the encoder IC4 (Motorola MC1377) for proper input signal coupling. The green and blue video drive signals are amplified by IC2 and IC3 respectively. All three OP-AMPs have identical circuit components and operate as described above for the red video signal.

Sync Conditioning and Level Set Circuitry

The composite sync signal (SYNC) from the PAL/NTSC Sync Board is applied to the Encoder board through J1-pin 1. The SYNC signal is capacitively coupled through C14 and is conditioned to the specific DC level

required by the encoder chip. The DC level is realized by coupling an encoder-developed 8.2V, DC-reference voltage level to the composite sync input line via 47K-ohm resistor R15. The SYNC input line of the encoder has a characteristic impedance of 1ØK ohms. The input impedance applied in series with R15 and the 8.2V DC reference level, develops the DC bias level required by IC4. The SYNC signal is biased to a static level which fulfills the application requirements of the encoder chip.

The 8.2V DC reference voltage level developed in the encoder chip is also used as a reference for the latching ramp (burst flag) generator circuitry that is internal to the encoder chip. The burst generation is provided by a sync-triggered ramp on pin 1 of IC4, and two internal level sensors. The chrominance envelopes, (R-Y) and (B-Y), can be set through potentiometers R19 and R17 respectively. These potentiometers are used to null residual color subcarrier signals which occur due to imperfections in gain, matrixing, and modulator balance. The black residual color subcarrier imbalance (from the modulators) can be nulled by sourcing or sinking small currents into clamp Pins 11 and 12 of IC 4. The nominal voltage on these pins is about 4.ØV DC, so the 8.2V reference at IC4 pin 16 provides a pull-up source.

The Encoder IC contains an on-board color reference oscillator. This oscillator drives the (B-Y) modulator and a voltage controlled phase shifter which produces an oscillator phase of 9Ø° ±7° at the (R-Y) modulator. Components R21, R22, and C23 make up a circuit for adjusting the modulator phase angle. Supplying a pull-up to IC4 pin 19 will increase the (R-Y) to (B-Y) phase angle by about 25°/uA. The nominal voltage on Pin 19 is about 6.3 VDC, so the +12V supply (VCC) is a good control reference.

Luminance and Chrominance Conditioning Circuitry

The recommended operating condition of the encoder chip requires a chrominance bandwidth of approximately ±Ø.5 Mhz. This bandwidth is realized through the use of a bandpass circuit connected between pins 10 and 13 of encoder chip IC4. The bandpass circuitry (made up of T1, R23 and R24, and C24 through C27) gives the desired bandwidth. When this bandwidth reduction circuitry is used, the chroma is delayed by approximately 35Ø ns. This 35Ø-ns delay results in a visible displacement of the color and the black-and-white information on the final display. Placement

of a delay line in the luminance signal path (L1) realigns the two components, chroma and luminance.

RGB Color to PAL/NTSC Encoder

The RGB color to PAL/NTSC encoder MC1377 (IC4) can encode NTSC and PAL to studio standards. All of the support circuits described in previous subsections adjust the condition of the inputs to the encoder. PAL or NTSC mode selection is accomplished by strapping IC4 pin 2Ø. A ground reference on pin 2Ø selects the NTSC mode while letting pin 2Ø float, or tying it to a pull-up selects PAL encoding.

The oscillator input (pin 17) receives the Color Sub Carrier (CSC) signal from the PAL/NTSC TV Sync Board. The CSC signal frequency is 4.4336 Mhz for PAL and 3.579 Mhz for NTSC encoding. The divider R1 and R2 reduce the input Color Subcarrier signal to the voltage amplitude as required by the MC1377 color encoder IC. R1 and R2 also set the oscillator input impedance to approximately 75 ohms.

The red, green, and blue color inputs are amplified to a required input level of 1.ØV and DC-coupled by the OP-AMP drivers, IC1 through IC3. The color signal inputs to pins 3, 4, and 5 should be at a 1V level because the encoder IC generates a predetermined Ø.6V sync and Ø.6V burst signal at the output. It needs the 1.ØV input signals to produce the corresponding full luminance and chrominance amplitudes.

As described in the Sync Conditioning section, the SYNC input requires a bias pull-up from the sync source. During the period between sync pulses, the voltage must be above 1.7V and below the 8.2V internal regulator. During sync, the voltage (negative going) must extend below +Ø.9V and should not exceed -Ø.5V.

The video output is AC coupled to the high-impedance input of an LHØØØ2 current driver IC5. IC5 gives additional drive current and provides a method of developing two composite video outputs (only one output is present on rear panel BNC connector). The output impedance of IC5 is about 6 ohms; by adding a 68-ohm resistor in series, the industry standard impedance of 75 ohms is realized. The composite video signal output of IC5 is the standard 1.ØV level. Further application documentation on the MC1377 color encoder IC may be obtained through Motorola Semiconductor Products, Inc. Refer to Application Note AN932 or the Motorola Linear and Interface IC handbook, series D - 1983.

APPENDIX A

The listing below is a typical list of reference manuals and may not match your particular installation. This is due to custom installations and system component interchangeability.

A. iSBC 8Ø/24A™ SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL by Intel Corporation

B. BULK SEMI MEMORY SYSTEM MODEL DR129/229/s by DATARAM Corporation

C. BS-1Ø1/1Ø2 by DATARAM Corporation

D. CONRAC 7211 (preliminary) by Conrac Division, Conrac Corporation

I. CONRAC 6242 (preliminary) by Conrac Division, Conrac Corporation (RGB/NTSC)

J. OKIDATA PERSONAL PRINTER USER'S MANUAL by OKIDATA (MICROLINE 293)

K. MIDDS HOST TO TERMINAL - TERMINAL TO HOST SYSTEM PROTOCOL DESCRIPTION dated 26 June 1985 by SSEC (REV. LEVEL 1)

L. IBM GUIDE TO OPERATIONS PERSONAL COMPUTER AT by IBM. Order #15Ø2241

M. IBM HARDWARE MAINTENANCE AND SERVICE PERSONAL COMPUTER AT. Volumes 1 and 2 by IBM. Order #15Ø2242

N. IBM TECHNICAL REFERENCE PERSONAL COMPUTER AT by IBM. Order #628ØØ7Ø

O. IBM TECHNICAL REFERENCE OPTIONS AND ADAPTERS Volumes 1 and 2 by IBM. Order #6322509

P. ADVANTAGE! MEMORY EXPANSION AND I/O BOARD for the IBM Personal Computer AT by AST Research Inc. Manual #ØØØ179-ØØ1C

Q. MULTIBUS ADAPTER MULTIBUS-IBM PC/AT CONNECTION by BiT3 Corporation.

R. ProNET MODEL P13ØØ IBM PC LOCAL NETWORK SYSTEM INSTALLATION AND PROGRAMMING GUIDE P13ØØV Addendum by Proteon Inc.

APPENDIX B

SCHEMATIC DIAGRAMS (Separate)

List of Diagrams and Drawings

Appendix C

Supplemental Information for PAL/NTSC TV circuit sections

Similarities and differences between the NTSC and PAL color television systems:

The first practical color broadcasting system was developed in the United States after a variety of methods had been proposed. The evolution of the system was guided by the recommendations of the National Television System Committee; consequently it has been termed the NTSC system. Varient systems have since been developed, incorporating many of the basic features of NTSC. These systems are PAL (Phase Alternating Line) and SECAM (Sequential Color with Memory).

The NTSC system is used in the US, Canada, Mexico, Japan, and a few other countries. The PAL variant, which started in West Germany, is used in Great Britain, most Western European countries, Australia, Brazil, and South Africa. SECAM, developed and used by the French, has been taken up by the USSR and some Eastern European countries. SECAM will not be discussed further; it is not applicable to McIDAS workstation operation.

One particular difficulty in television transmission and reception arises because signals that differ in frequency or amplitude take varying amounts of time to pass through a stage, network, or channel; this results in "phase distortion", with undesirable effects on the chrominance sub-carrier.

The phase relationship between the sub-carrier transmitted during picture time and the burst transmitted within "back porch" periods determines the hue. If any spurious change of this relationship occurs, wrong hues are displayed on the receiver. Phase change resulting from changes in amplitude, either of the luminance signal or the sub-carrier itself, is termed differential phase distortion.

There are a number of ways in which differential phase distortion may be produced in transmission circuits and with complex transmission chains (e.g., video tape recorders, line systems, transmitters, receiver i.f. stages); there is some difficulty keeping the overall distortion within acceptable limits.

The PAL color television system was developed to reduce the effects of differential phase errors which may be suffered by the chrominance sub-carrier in transmission and reception. With PAL, color difference signals (R-Y) and (B-Y) of equal bandwidth are used (as opposed to the I and Q chrominance signals of NTSC). These modulate a sub-carrier in amplitude and phase in a way similar to NTSC, except that the (R-Y) contribution to the resultant is reversed in polarity on sucessive lines. Differential phase errors may thus be corrected over a period of two lines rather than from field to field.

NTSC

Line Standard	Fields per sec.	Line freq(hz)	Sub-carrier freq(Mhz)	Sub-carrier in terms of line freq
525	59.94	15,734.26	3.579545	455/2

The PAL system more closely follows the 625-line standard of the NTSC system. The basic sub-carrier frequency adopted by PAL is the NTSC value plus a quarter of the line frequency. By adding another half cycle per field (i.e., by adding 25 hz) to the sub-carrier frequency, dot pattern interlacing is achieved reducing the screen dot pattern wavering caused by variations in the chrominance signal. The final precise sub-carrier frequency for the PAL 625-line system becomes: (567/2 + 1/4)x 15625 + 25(hz)=4.43361875 Mhz

The table below shows the relevant characteristics of the 625-line PAL color television system.

PAL

Line Standard	Fields per sec.	Line freq(hz)	Sub-carrier freq(Mhz)	Sub-carrier in terms of line freq
625	50	15,625	4.43361875	567.5/2

The NTSC system provides good compatibility, good vertical and horizontal resolution, is rugged in the presence of noise in various degrees and forms, and is reasonably simple to transmit and receive.

The main drawbacks of the NTSC system are its susceptibility to differential phase distortion and its bandwidth requirement to avoid crosstalk between the color difference signals (with resultant hue distortion).

The main feature of the PAL system is its good protection against differential phase distortion. Transmitting and receiving equipment tends to be more complicated. The advantages associated with video tape recording outweigh the disadvantages, and transmission over long links is not as difficult as with NTSC.

The main advantage of PAL over NTSC is reduced hue distortion, but this advantage is exchanged for the slightly reduced compatibility and lower vertical chrominance resolution. The latter failing is inherent in delay line receivers.