McIDAS

Man computer Interactive Data Access System

Ingestors Manual

March 1989

Space Science and Engineering Center
University of Wisconsin - Madison
1225 West Dayton Street
Madison, WI 53706
Telephone 608-262-2455
TWX 608-263-6738

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University of Wisconsin - Madison
1225 West Dayton Street
Madison, WI 53706
Telephone 608-262-2452
TWX: 910-286-8276

METEOSAT PDUS Ingestor

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METEOSAT PDUS Ingestor

METEOSAT is the European meteorological satellite system. Appendix A describes the METEOSAT system and a typical Primary Data User Station (PDUS). A PDUS uses the processed and retransmitted high resolution digital METEOSAT data.

The METEOSAT Ingestor card (hereafter referred to as "ingestor") is a Multisourcerer application card. It functions as an intelligent interface between a Dornier Frame Synchronizer and the internal Multibus* of the Multisourcerer.

The raw satellite data is processed, formatted into "records", and retransmitted to the METEOSAT satellite. The satellite broadcasts the data serially on an S-band microwave channel to METEOSAT users. The PDUS receiving and demodulating system recovers the serial data bits. This data is passed to the Dornier Frame Synchronizer (frame sync). The frame sync forms the serial data bits into 16-bit parallel words. Each 16-bit word represents two bytes of data. The ingestor collects the words and reconstructs them into data records. It does this by separating the 16-bit words into bytes and storing them in one of two input buffers.

When the entire data record has been assembled, the input buffers are swapped, making an empty input buffer available for the next incoming record. While the next record is being assembled, the previous record is transferred to the host.

The following documentation assumes that you are familiar with Appendix A and 8085 microprocessor applications.

This document is divided into three areas of discussion:

- Basic Functional Description
- Detailed Functional Description
- Detailed Circuit Description

*MULTIBUS is a registered trademark of INTEL Corporation.

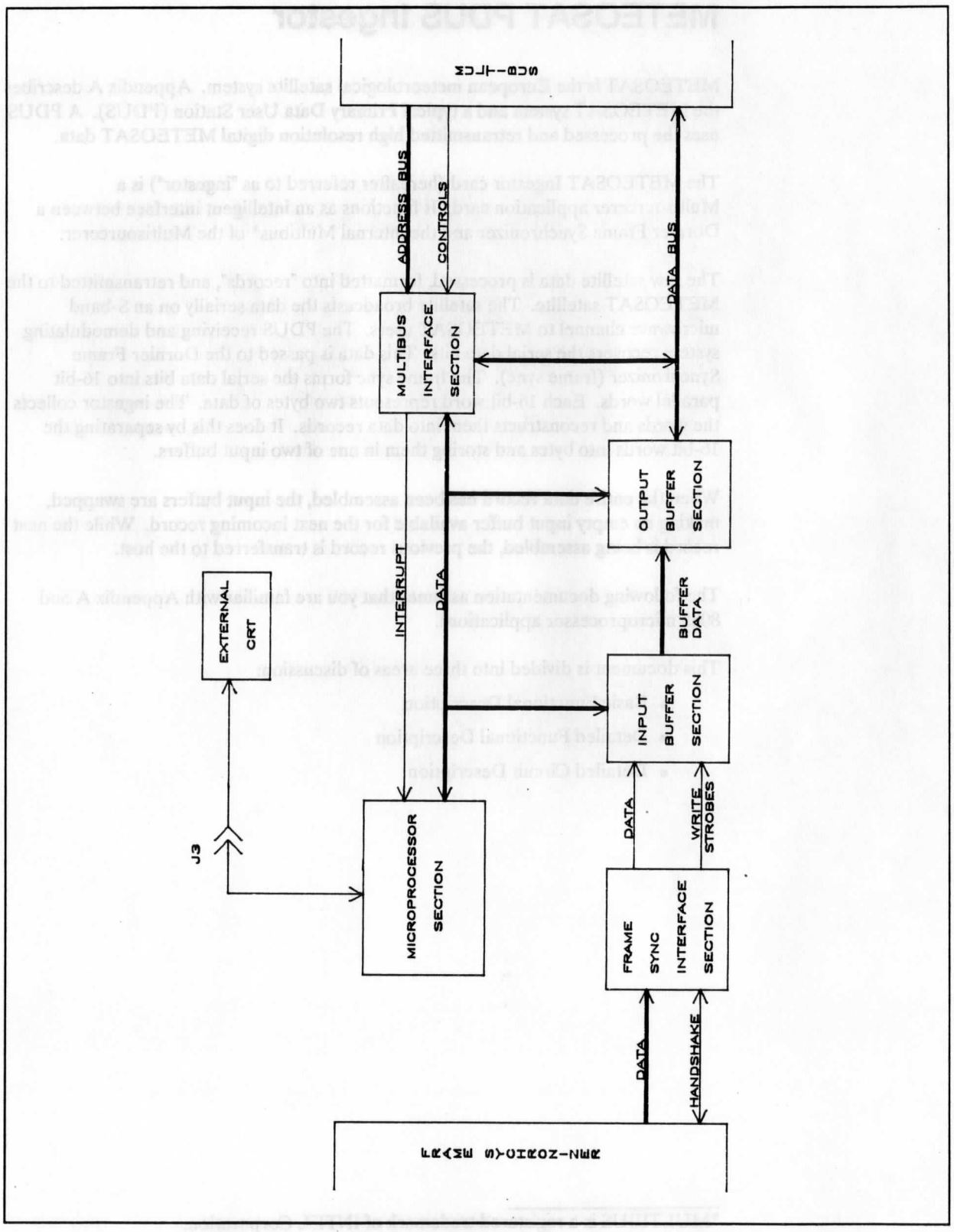


Figure 1. Simplified Block Diagram of the METEOSAT PDUS Ingestor

Basic Functional Description

Figure 1 on the adjacent page is the Simplified Functional Block Diagram of the PDUS METEOSAT Ingestor. The ingestor is divided into the following five functional parts:

- Frame Synchronizer Interface Section
- Input Buffer Section
- Output Buffer Section
- Microprocessor Section
- Multibus Interface Section

Frame Synchronizer Interface Section

The Dornier Frame Synchronizer converts the serial data stream input to a parallel output. METEOSAT data is eight bits per word. The frame sync sends two words (16 bits) at a time to the ingestor via a 16-bit parallel bus. Handshake signals control the data transmission process.

The Frame Sync Interface Section separates the 16-bit input words into two 8-bit words, and sends these words to the Input Buffer Section. The Frame Synchronizer Interface Section also develops an input load strobe for each word it transfers to the Input Buffer Section. Two input load strobes are generated for each 16-bit input word.

Input Buffer Section

The Input Buffer Section consists of two buffers. Each buffer can function as either an on-line buffer or an off-line buffer. The on-line buffer receives satellite input data while the off-line buffer passes its previously stored data to the Output Buffer Section. When reception of the current incoming record is complete, the buffers swap functions. That is, the on-line buffer becomes the off-line buffer and vice versa.

Output Buffer Section

The Output Buffer Section is nearly identical to the Input Buffer Section. It has two buffers that function as either on-line or off-line buffers. The off-line buffer receives data from the off-line input buffer while the on-line buffer transfers data to the Multibus. When both output buffers complete their respective transfer, the buffers swap functions.

Microprocessor Section

The Microprocessor Section is a conventional 8085 design. It functions as the board controller. The following are primary functions performed by this section:

- input buffer switching
- output buffer switching
- diagnostic testing of other ingestor sections
- data transfer control
- asynchronous communications with an external CRT
- Multibus interface control

Multibus Interface Section

The Multibus Interface Section makes the ingestor appear (from the Multibus' perspective) as a group of I/O ports. The Multibus writes commands and controls into two of these ports. The ingestor reads the commands and controls to determine what data is requested. The ingestor informs the Multibus of its progress in acquiring the requested data via a status port. The Multibus periodically reads ingestor status to determine when the ingestor has the requested data ready. When the Multibus is ready to receive the requested data, it sends the ingestor a command instructing it to send the data.

Detailed Functional Description

The Detailed Functional Block Diagram of the PDUS METEOSAT Ingestor is shown in Figure 2 on the page 7. This figure is an expansion of Figure 1, and introduces the main control blocks. Note that the schematic sheet numbers are listed in each functional block. This should make the transition from the Functional Descriptions to the schematic diagrams easier.

This detailed functional description includes:

- Frame Sync Interface Section
- Input Buffer Section
- Output Buffer Section
- Microprocessor Section

Frame Sync Interface Section

Before discussing the Frame Sync Interface Section, a few Dornier Frame Synchronizer characteristics should be reviewed. The Dornier Frame Synchronizer assembles the serial data output of a bit synchronizer into double-byte words (16 bits total). It sends these words to the ingestor via a 16-bit parallel bus. When the 16-bit word is valid and stable on the parallel bus, the frame sync sets the Data Ready flag (DRF). DRF remains active until the ingestor responds to the flag by activating the Acknowledge (ACK) signal.

Byte Selector

The 16-bit frame sync words must be disassembled into two 8-bit words because all ingestor buffers and buses are eight bits wide. The Byte Selector, under control of the Frame Sync Interface Controller, performs this function.

Interface Controller

DRF goes true after the data on the 16-bit input bus is valid. While the data is valid, the Frame Sync Interface Controller performs two Buffer Memory transfers. First, it transfers the least significant byte of the 16-bit word, then it transfers the most significant byte. The Frame Sync Interface Controller generates the Buffer Memory transfer strobes (Load Clock in Figure 2), and manipulates the SEL (select) input to the Byte Selector during the transfer.

The Frame Sync Interface Controller manages the ingestor's side of the handshake scheme between the ingestor and the frame sync. Essentially, this consists of returning an ACK (Acknowledge) after receiving a DRF flag. The ingestor holds ACK until DRF goes false.

ID Clock Pulse Inhibitor Refer to Appendix A, if necessary. The Dornier Frame Sync strips off the three sync words located at the beginning of each frame. It sends the remaining 361 bytes of each frame to the ingestor. The first byte of each 361-byte frame is the ID word. The ID word is not used, and must also be stripped off before storing the frames in the Input Buffer.

The ID Clock Pulse Inhibitor receives input Load Clock pulses from the Frame Sync Interface Controller. It inhibits the first clock pulse in each 361-byte frame. The Input Buffer Address Generator uses the output of the ID Clock Pulse Inhibitor as memory write strobes for the Buffer Memory. Since the ID words' clock pulses are inhibited, the ID words are not stored in the Buffer Memory.

The ID Clock Pulse Inhibitor is initialized every eight frames (A-Format) or every four frames (B-Format) by EOR (End of Record). The frame sync generates the EOR signal, marking the end of the current subframe and the beginning of the next subframe. EOR also generates a restart interrupt for the microprocessor. The function of this interrupt is discussed further in the Microprocessor Section.

Input Buffer Section

The Input Buffer Section stores input data from the Frame Sync Interface Section. It transfers data to the Output Buffer when enabled by the Microprocessor Section.

Input Buffers A and B Each Input Buffer is a 4K by 8-bit static RAM. Each buffer can function as either the on-line or off-line buffer. These functions are toggled by EOR. That is, at the end of each record the on-line buffer becomes the off-line buffer, and the off-line buffer becomes the on-line buffer. Input data is stored in the on-line buffer while the off-line buffer's data is transferred to the Output Buffer Section.

Data Director The Input Buffer Data Director receives input data from the Frame Sync Interface Section and the Microprocessor Section. The Input Data Bus (see Figure 2) transports the lower byte, then the upper byte, from the Frame Sync Interface to the Input Buffer Data Flow Director. The Input Buffer Data Director sends either the Selected Data or microprocessor data to the on-line buffer (A or B). The microprocessor writes data to the Input Buffer Section during diagnostic testing.

The Input Buffer Data Director passes data from the off-line input buffer to the Microprocessor Section or the Output Buffer Section. It passes data to the microprocessor during diagnostic testing and data ingesting.

Controller The Input Buffer Controller performs the following control functions:

- enables the data source in the Input Buffer Data Director to the online buffer
- generates write strobes for the on-line and off-line buffers
- gates the off-line buffer data to the selected destination

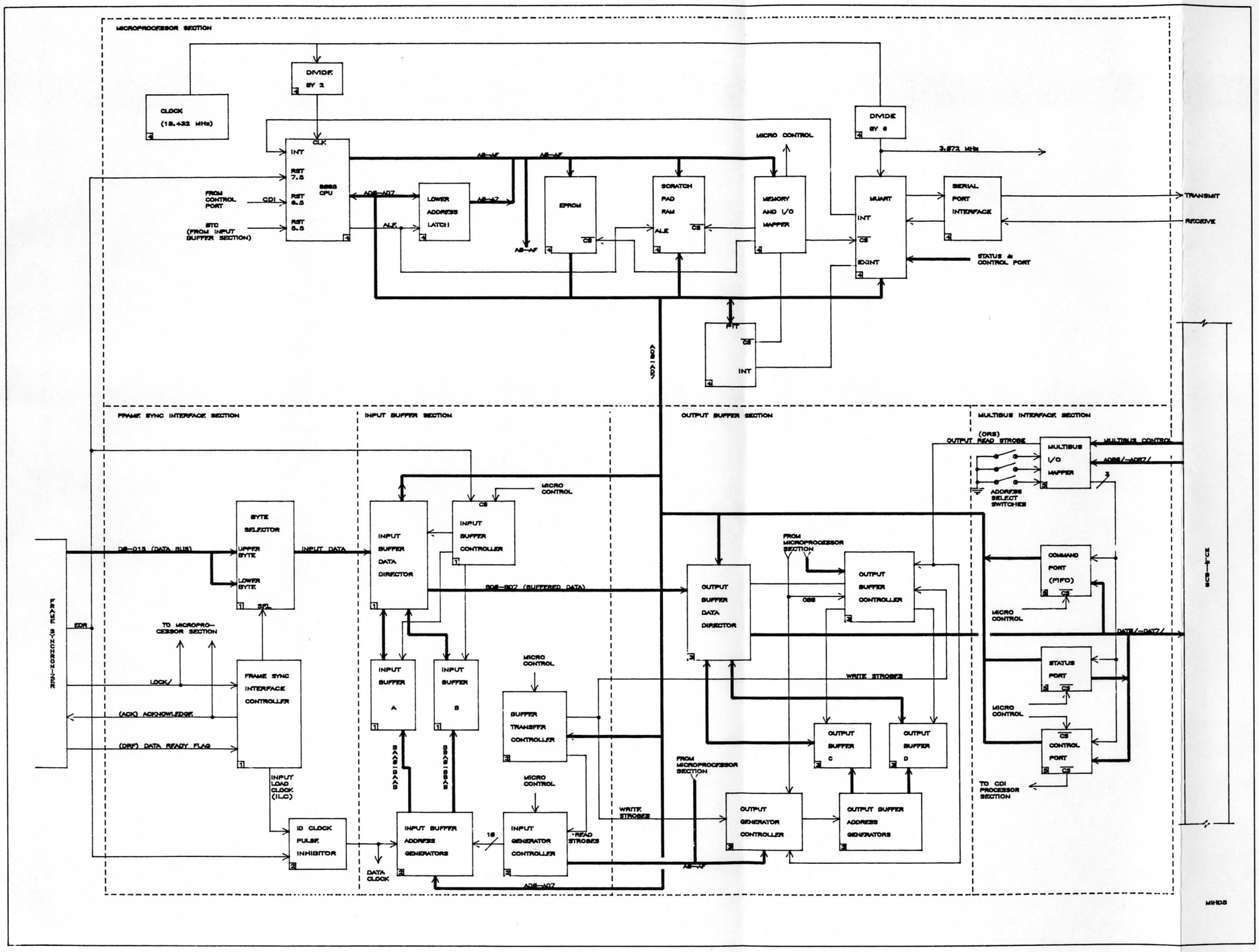


Figure 2. Detailed Functional Block Diagram of the METEOSAT PDUS Ingestor

Address Generators

The Input Buffer Address Generators block consists of two 12-bit programmable up/down binary counters. One counter drives the address inputs of Input Buffer A. The other drives the inputs of Input Buffer B. Each counter has the following control inputs from the Input Generator Controller:

- clear
- count up clock
- countdown clock
- lower byte load
- upper nibble load

The on-line Input Buffer Address Generator is always cleared (reset to 000H) prior to the arrival of the first byte of a new record. The on-line generator is always in the count up mode. However, the off-line Input Buffer Address Generator is usually preset (loaded) with the address of the last stored byte, and the generator is operated in the countdown mode.

The METEOSAT satellite physically scans from east to west and south to north. Since most image monitors scan from left to right and top to bottom, images would appear upside down and backwards if the data was used in the same chronological order as generated. The mainframe reverses the south to north effect; the ingestor reverses the east to west effect. The east to west effect is corrected by storing data in the on-line input buffer in ascending address order, and outputting this data in descending address order.

Generator Controller

The Input Generator Controller produces the five control signals listed above for each counter. This block receives control and data inputs from the Microprocessor and Frame Sync Interface Sections. The Microprocessor Section controls the up/down mode of the off-line buffer's address generator. Microprocessor read/write controls produce appropriate up/down clock pulses for the address generators during microprocessor read/write cycles. Load Clock pulses from the Frame Sync Interface produce clock up pulses for the on-line Input Buffer Address Generator. Finally, counter offsets, required when reading the off-line buffer backwards, are transported to the Input Generator Controller by the microprocessor's AD bus.

Transfer Controller

The Buffer Transfer Controller controls the record transfers from the off-line Input Buffer to the off-line Output Buffer. The heart of this block is a programmable 16-bit counter. Prior to the start of a transfer, the microprocessor loads the counter with the number of bytes to be transferred. Then, the microprocessor enables the block via a control signal from its MUART, allowing the transfer to commence. The block has three outputs, an off-line Input Buffer read strobe, an off-line Output Buffer write strobe, and a Buffer Transfer Complete (BTC) interrupt for the microprocessor. The read and write strobes are generated at a 3.072 MHz rate until the counter decrements to zero. When the counter reaches zero, the transfer ceases and BTC goes active, interrupting the microprocessor. The interrupt informs the microprocessor that the transfer is complete, allowing the microprocessor to remove the transfer enable signal.

Output Buffer Section

The Output Buffer Section is functionally and physically very similar to the Input Buffer Section.

Output Buffers C and D

Output Buffers C and D are physically identical to Input Buffers A and B. The off-line output buffer receives input data from the off-line input buffer (via the Output Buffer Data Director). The on-line/off-line functions are toggled by OBS (Output Buffer Switch). OBS is a control signal output of the MUART and is controlled by the microprocessor.

Data Director

The Output Buffer Data Director receives data from the Input Buffer and Microprocessor Sections. The Output Buffer Data Director sends data to the off-line buffer. During diagnostic testing, the microprocessor can write data to either the on-line or off-line buffer.

The Output Buffer Data Director gates data from the on-line output buffer to either the Multibus or the Microprocessor Section (diagnostic testing only).

Controller

The Output Buffer Controller performs the following control functions:

- gates the selected data to the off-line buffer
- generates write strobes for the off-line buffer
- gates on-line buffer data to the selected destination

Address Generators

The Output Buffer Address Generators generate addresses for Output Buffers C and D. Each buffer has its own generator. These generators always begin at address 000H and can only be incremented. Thus, they are physically and functionally simpler than their Input Buffer Section counterparts. Each generator has the following control inputs:

- clear
- clock (up)

The respective generator is always reset to zero prior to the start of a transfer. The counters are incremented after each byte transfer.

Generator Controller

The Output Generator Controller produces the clear and clock input for each address generator. OBS determines the off-line and on-line buffers. ORS (Output Read Strobe) causes the Output Generator Controller to generate a clock pulse for the on-line generator after each Multibus I/O read cycle. Write strobes from the Input Buffer Section cause the Output Generator Controller to generate clock pulses for the off-line generator after each byte transfer.

Microprocessor Section

The Microprocessor Section is conventional in design. The design is based on the Intel 8085 microprocessor.

Microprocessor

The hardware aspect of the 8085 microprocessor is well documented in Intel's *Microprocessor and Peripheral Handbook*. The *Intel 8080/8085 Assembly Language Programming* manual provides a good programming reference for the 8085. The additional 8085 hardware documentation provided here is limited to that which is necessary to discuss remaining Microprocessor Section components.

The 8085 has three restart interrupt inputs. They include RST5.5, RST6.5 and RST7.5. All three are used in the METEOSAT application. The restart interrupts allow hardware to force the 8085 into an interrupt service routine. Upon completion of the service routine, the 8085 returns to the point in the program from which it was interrupted. BTC drives the RST5.5 interrupt, and interrupts the 8085 upon completion of an off-line input buffer to off-line output buffer transfer. The RST6.5 interrupt is driven by the Control Port. The Control Port automatically generates an interrupt (CDI) when the Multibus writes to it. RST7.5 allows the End of Record (EOR) signal, initiated by the frame sync, to interrupt the 8085 at the end of a record.

Lower Address Latch

The 8085 multiplexes data with the lower eight bits of the address and outputs this information on its AD bus (AD0-AD7). The 8085 outputs a demultiplexing control signal called ALE (Address Latch Enable). ALE is high when the multiplexed address/data bus carries valid address information. The Lower Address Latch is driven by the AD bus; it is latched by ALE. Thus, the output of the latch is the lower eight address bits. The upper eight address bits are output directly from the address port on the 8085. This port joins the output of the Lower Address Latch to form the 16-bit address bus (A0-AFH). This bus drives the EPROM, Scratch Pad RAM, and the Memory and I/O Mapper. Each of these devices is discussed separately below.

EPROM

The 8K by 8-bit EPROM (Erasable Programmable Read-Only Memory) stores the ingestor's firmware. The 13 LSBs of the A bus (A0-AC) drive the address inputs. The EPROM's output connects to the microprocessor's AD bus.

RAM

The RAM (Random Access Memory) provides temporary storage for the following system variables:

- microprocessor's stack
- data record label
- CRT message buffers
- program pointers and flags

The RAM has a multiplexed address/data port, and is connected directly to the AD bus. The ALE output of the microprocessor demultiplexes the addresses and data. The RAM's two MSB address inputs are driven by A8 and A9 of the A bus.

Memory & I/O Mapper The Memory and I/O Mapper produce chip enable signals for each device addressable by the microprocessor. This block produces chip enables for the following:

- EPROM
- RAM
- Programmable Interval Timer (PIT)
- Control Port
- Status Port
- Input Buffer Controller
- Command Port
- MUART

PIT The PIT (Programmable Interval Timer) has three independent 16-bit programmable counter/timers. One counter/timer functions as an event counter, counting the number of bytes transferred from the off-line input buffer to the off-line output buffer. It is part of the Buffer Transfer Controller (refer to the Input Buffer Section). The remaining two counters are cascaded to produce a 32-bit counter. The output of the first counter drives the input of the second counter.

The cascaded counter generates an interrupt if the frame sync takes more than 90 seconds to acquire a signal after receiving an IDLE command. The IDLE Command instructs the ingestor to wait for the RST 7.5 EOR interrupt.

MUART The MUART (Multifunction Universal Asynchronous Receiver Transmitter) combines several microprocessor functions into a single LSI chip. This chip provides:

- five 8-bit programmable timer/counters
- a programmable serial asynchronous communications interface
- an on board baud rate generator
- two 8-bit programmable parallel I/O ports
- an eight level priority interrupt controller

The timer/counters are numbered 1-5. Timer/counter 1 is not used. Timer/counters 2 and 4 are cascaded, yielding a 16-bit timer. They are used as the SYNC command timeout counter. The ingestor informs the host when it begins receiving header records. The host may issue a SYNC command which tells the ingestor to wait for the first data record. Up to 84 2912-byte header records may be received before the data records begin (see Appendix A). The firmware shuts off the SYNC timeout counter when a data record is received.

Timer/counter 3 functions as the WAIT command timeout counter. The WAIT command tells the ingestor to wait for the next data record. The host issues WAIT commands when the current data record is not required by the host.

Timer/counter 5 functions as a retriggerable counter. It is reset (retriggered) by ACK, the ingestor's response to the frame sync's input data. Thus, if the frame sync stops sending data, no ACKs are generated, and timer 5 times out, causing an interrupt.

The programmable serial asynchronous communications interface provides an interface to a CRT. It can monitor host commands and display record labels and ingestor status. It is not required for ingestor operation.

The on board baud rate generator generates a baud rate clock for the programmable serial asynchronous communications interface. It can generate 13 standard baud rates, ranging from 50 baud to 19.2K baud. Currently, it is programmed for 19.2K baud.

The MUART has two 8-bit programmable I/O ports. Only Port 1 is currently used. Each I/O pin on Port 1 can be individually defined as an input or output pin. The pins that are defined as output pins are used as control inputs to other sections of the ingestor; the pins that are defined as inputs provide status inputs from other sections of the ingestor.

The eight level priority interrupt controller assigns priorities to the following interrupt sources:

- port 1 (highest priority)
- external interrupt (EXINT)
- timer 3
- asynchronous receiver buffer full
- asynchronous transmitter buffer empty
- timer 2 and 4 (cascaded)
- timer 5 (lowest priority)

The eight level priority interrupt controller prevents interrupt source contention during simultaneous interrupts. INT, the output of this section, drives the INT input on the microprocessor. The microprocessor executes an interrupt service routine for the device causing the interrupt.

Clock

The Clock generates an 18.432 MHz square wave. This signal frequency is divided by two to produce a 9.216 MHz clock input for the microprocessor. The Clock output drives a divide-by-six circuit to produce a 3.072 MHz clock for the MUART and Input Buffer Controller.

Multibus Interface

The Multibus Interface section makes the ingestor appear (from the Multibus' perspective) as a group of I/O ports. A switch-programmable I/O address decoder responds only to Multibus I/O activity intended for this ingestor. It generates enable signals for the three I/O ports addressable by the Multibus. Each I/O port has a unique address within the block of I/O addresses selected by the address decoder. The three I/O ports are:

- Control and Status Port
- Command and Data Out Port
- Soft Reset Port

The Control and Status port is actually two I/O ports that share the same I/O Port address. The Control Port responds to Multibus write cycles and the Status Port responds to Multibus read cycles. The Multibus writes to the Control Port which is read by the microprocessor. The Control Port hardware automatically interrupts the microprocessor when the Multibus writes to it. The Multibus can tell the microprocessor to either abort the last command or read a new command that is just written to the Command Port. The microprocessor writes to the Status Port. This port is read by the Multibus, and allows the GPCI to monitor progress of the previous command.

The Command and Data Out Port is actually two I/O ports that share the same I/O port address. The Command Port responds to Multibus write cycles and the Status Port responds to Multibus read cycles.

The Multibus writes to the Command Port which is read by the microprocessor. The Command Port can store commands up to 16 bytes in length. However, writing to the Command port has no effect on the microprocessor. That is, it does not generate an interrupt. The microprocessor must be informed of the new command by writing an appropriate control word to the Control Port (see the preceding paragraph) after writing the command.

The Data Out Port passes image data to the GPCI. First, the ingestor transfers an image data record from its Input Buffer to its Output Buffer, making the data available to the GPCI. Then, the ingestor sets the Data Present flag in the Status Port. The GPCI polls the Status Port periodically, and upon detection of the Data Present flag, performs a DMA transfer from the Data Out Port to the GPCI.

The Soft Reset Port allows the GPCI to reset the METEOSAT PDUS Ingestor. The GPCI issues a soft reset when it receives unexpected results for commands issued to the ingestor.

Detailed Circuit Description

The schematic diagrams of the METEOSAT PDUS Ingestor are shown on SSEC drawing #6450-0537 (Revision H, dated 1/7/88).

Circuit Labels

The METEOSAT Ingestor is built on a Multibus wire-wrap form factor board. Pin locations on the board are described by the column designator (alpha) and the row number. Each IC schematic circuit symbol has a three or four character label that describes the column and row where pin 1 of that IC is located. The Detailed Circuit Description that follows refers to the ICs by this location label. For example, a 74LS640 IC whose 1 pin is located in Column T and row 23 is referred to as T23. When reference is made to a schematic circuit symbol of a multiple section device, the symbol ID is used, followed by a hyphen and the letter designator. The symbol ID alone refers to single section ICs.

Logic Conventions

Logic signal names are indicated by all uppercase letters and numbers (i.e., OBS). A logic signal name that ends with a trailing slash represents an active low signal (i.e., INIT/).

There are several conventions that can describe the state of a logic signal. Some of these conventions are true or false, high or low, one or zero, and active or inactive. In the remaining METEOSAT discussion, all logic states are described with "high" and "low." This convention best describes the physical condition of a logic signal and is better suited for troubleshooting.

Frame Sync Interface Section

The Frame Sync Interface is shown on sheet 1 of the schematics. It includes:

- Byte Selector
- Frame Sync Interface Controller
- ID Clock Pulse Inhibitor

Byte Selector

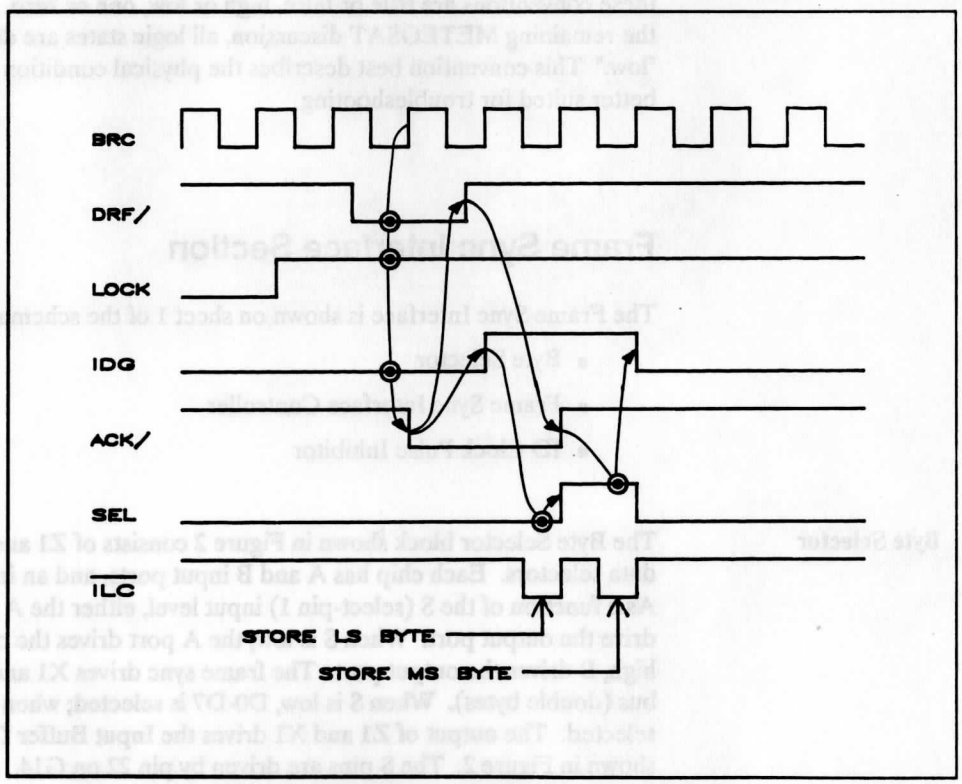
The Byte Selector block shown in Figure 2 consists of Z1 and X1. Z1 and X1 are 4-bit data selectors. Each chip has A and B input ports, and an inverting output port (Y/). As a function of the S (select-pin 1) input level, either the A or B port is selected to drive the output port. When S is low, the A port drives the output port; when S is high, B drives the output port. The frame sync drives X1 and Z1 with its 16-bit data bus (double bytes). When S is low, D0-D7 is selected; when S is high, D8-D15 is selected. The output of Z1 and X1 drives the Input Buffer Data Director block shown in Figure 2. The S pins are driven by pin 22 on G14. A portion of G14 functions as the Frame Sync Interface Controller.

Interface Controller

The Frame Sync Interface Controller involves a portion of G14, a Programmable Array Logic (PAL,*). The controller interacts with the frame sync during data ingesting. It also generates the select signal that drives the S pins on the Byte Selector. Finally, the Frame Sync Interface Controller generates ILC (Input Load Clock).

Refer to Timing Diagram 1 below. Upon recognition of a record's sync pattern, the frame sync sets LOCK/ low. LOCK/ remains low during the entire record. LOCK/ is inverted by J15-C and applied to G14. Inverted LOCK/ functions as an enable input to the ACK/ logic. When the data on D0-D15 is valid, the frame sync drops DRF/ (Data Ready Flag). After DRF/ goes low, the next rising edge of BRC (Baud Rate Clock - 3.072 MHz) causes DAK (Data Acknowledge) to go high. An inverter in AD31 produces ACK/ by inverting DAK.

ACK/ is a handshake input to the Frame Sync. When ACK/ goes low, the frame sync raises DRF/ after some propagation delay. After DRF/ rises, the next rising edge of BRC sets DAK low (ACK/ goes high). IDG (Input Data Gate) follows ACK by one BRC clock period. ILC/ (Input Load Clock) is produced by NANDing BRC with IDG. Thus, ILC/ goes low twice for each input word. The Input Buffer description shows how the falling edges of ILC/ clocks data into the Input Buffer. The first rising edge of BRC, after IDG goes high, causes SEL to go high. SEL automatically returns low on the next rising edge of BRC Thus, X1 and Z1 transfer D0-D7 to the Input Buffer Section during the first ILC pulse, and transfer D8-D15 on the last ILC pulse.



Timing Diagram 1. Frame Sync Interface Controller Timing

*PAL is a registered trademark of Monolithic Memories Incorporated.

ID Clock Pulse Inhibitor The ID Clock Pulse Inhibitor is shown on sheet 2 of the schematics. The ID Clock Pulse Inhibitor consists of AF1, AF17, part of AD31, AF9-A and AF9-B. AF1-A, AF1-B and AF17-B compose a 9-bit counter. AD31 and AF9-A function as a 6-input AND gate. The AND gate provides the feedback necessary to limit the maximum count to 360. AF17-A resets the counter at the end of the 361 pulse or at the end of a record.

An End of Record (EOR) pulse clears AF17-A. This places a high level at the J-input of AF17-A, and a high at the CLR (Clear) input pins of AF1 (pins 2 and 12). The high input on pins 2 and 12 clears both sections of AF1, causing all Q outputs to go low. Thus, the output of AF9-A is low, placing a low at the K input of AF17-A. The low Q (pin 3) output of AF17-A clears AF17-B and disqualifies AF9-B. Note that ILC (described in the previous section) is the other input to AF9-B. Thus, as long as AF17-A is reset, AF9-B blocks the passage of ILC/ pulses to Z32.

The falling edge of the first ILC pulse that arrives after AF17-A is reset toggles AF17-A (sets AF17-A). The counters do not count this pulse since the overriding CLR input was still high when the falling edge occurred. As soon as AF17-A sets, pin 4 of AF9-B goes high, allowing AF9-B to pass subsequent ILC/ pulses. AF17-A is unaffected by subsequent clock inputs as long as AF9-A supplies a low input to the K input of AF17-A. Thus, as soon as AF17-A sets, the output of AF9-B follows its pin 5 input (ILC/). To summarize, the first ILC pulse removed the CLR inputs from the counters and qualified AF9-B.

Now, the counter increments on the falling edge of each ILC/ pulse. On the falling edge of the 129th pulse the QD output of AF1-B goes high. On the falling edge of the 257th input pulse, the QB output of AF1-B goes low, clocking AF17-B (AF17-B goes set). The Q output of AF17-B drives one input of AD31. AD31 is a PAL programmed as a five input AND gate. The output of AD31 (pin 15) goes high when the remaining four inputs are simultaneously high. This occurs after the falling edge of the 359th pulse, and drives pin 2 of AF9-A high. The falling edge of the 360th pulse drives the QA output of AF1-A high, producing a high output from AF9-A. Now, AF17-A will reset on the next falling edge of ILC (361st pulse). The 361st ILC pulse resets AF17-A, causing the counters to reset in coincidence with the last data pulse of the frame. Thus, on each counter cycle, the first ILC pulse is blocked, and the next 360/ pulses pass through AF9-B.

X32 PIN#	PAL Term	Data Transfer *Source	Data Transfer *Dest.	Active State	Buffer Status On-Line	Buffer Status Off-Line	Buffer Mode Read	Buffer Mode Write	I/O Port	Diag. Test
21	MADE	BS	A	low	yes	no	no	yes	--	no
		A	OB	low	no	yes	yes	no	--	no
20	MADS	BS	A	low	yes	no	no	yes	--	no
		A	OB	high	no	yes	yes	no	--	no
19	MBDE	BS	B	low	yes	no	no	yes	--	no
		B	OB	low	no	yes	yes	no	--	no
18	MBDS	BS	B	low	yes	no	no	yes	--	no
		B	OB	high	no	yes	yes	no	--	no
23	WSA	BS	A	low	yes	no	no	yes	--	no
		MP	A	low	no	yes	no	yes	D0,D1	no
		MP	A	low	--	--	no	yes	D2,D4	yes
15	WSB	BS	B	low	yes	no	no	yes	--	no
		MP	B	low	no	yes	no	yes	D0,D1	no
		MP	B	low	--	--	no	yes	D3,D5	yes
17	PDDS	MP	A,B	low	no	yes	no	yes	D0,D1	no
		MP	A,B	low	--	--	no	yes	D2-D5	yes
		A,B	MP	high	no	yes	yes	no	D0,D1	no
		A,B	MP	high	--	--	yes	no	D2-D5	yes
22	PDAE	A	MP	low	no	yes	yes	no	D0,D1	no
		MP	A	low	no	yes	no	yes	D0,D1	no
		A	MP	low	--	--	yes	no	D2,D4	yes
		MP	A	low	--	--	no	yes	D2,D4	yes
16	PDBE	B	MP	low	no	yes	yes	no	D0,D1	no
		MP	B	low	no	yes	no	yes	D0,D1	no
		B	MP	low	--	--	yes	no	D3,D5	yes
		MP	B	low	--	--	no	yes	D3,D5	yes

* A = Buffer A
B = Buffer B
BS = Byte Selector
MP = Microprocessor
OB = Output Buffer

Table 1. Input Buffer Controller Signal Characteristics

Input Buffer Section

The Input Buffer Section is shown on sheet 1 of the schematics. It includes:

- Input Buffers A and B
- Input Buffer Data Flow Director
- Input Buffer Conroller
- Input Buffer Address Generators
- Input Generator Controller
- Buffer Transfer Controller

Input Buffers A and B

The input buffers consist of four high speed static RAMs. The RAMs are organized as 4K by 4-bits. Two RAMs are cascaded to produce each 4K by 8-bit buffer. Z10 and Z21 compose Buffer A; X10 and X21 compose Buffer B. The address inputs of Buffer A (BAA0-BAAB) are driven by the Buffer A Address Generator; the address inputs of Buffer B (BBA0-BBAB) are driven by the Buffer B Address Generator. These generators are described below. The write enable for each buffer is driven by the Input Buffer Controller.

Data Flow Director

The Input Buffer Data Flow Director consists of four 4-bit bidirectional bus drivers located at AB1, AB10, V1, and V10, and two octal transceivers located at T12 and T1. AB1 and AB10 link Buffer A to the Byte Selector and the BD bus; T12 links Buffer A to the microprocessor's AD bus. Likewise, V1 and V10 link Buffer B to the Byte Selector and the BD bus; T1 links Buffer B to the microprocessor's AD bus. All chip selects and data direction controls for this section are driven by the Input Buffer Controller. These signals are described below. Unlike the octal transceivers, the bidirectional bus drivers have separate input and output ports. This isolates the Input Data bus from the BD bus. For this reason, input data can be channeled into one input buffer while the other input buffer is transporting data to an output buffer.

Input Buffer Controller

The Input Buffer Controller consists of PAL P22V10 located at X32. X32 generates the chip enable and direction control signals for AB1, AB10, V1, V10, T1 and T12. X32 also generates the write enable signals for Input Buffers A and B. X32 is completely described by its equations found in the Supplemental Data Section. Each signal is functionally described in Table 1 on the adjacent page. These signals contain one or more of the following input terms:

- ILC - Input Load Control
- IBS - Input Buffer Switch
- IBC - Input Buffer Control (Microprocessor I/O ports D0/H-DFH)

ILC is the input load strobes that originate in the Frame Sync Interface Section. IBS determines the on-line and off-line buffers. When IBS is low, Buffer A is on-line, and Buffer B is off-line; when IBS is high, Buffer A is off-line, and Buffer B is on-line. IBC is a microprocessor memory-mapped I/O control signal that goes low for I/O port address D0H-DFH. Thus, IBC goes low when the microprocessor reads data from or writes data to Buffers A or B.

Z32 PIN#	PAL Term	Data Transfer *Source	*Dest	Buffer Status	Buffer Mode	I/O Port	Diag. Test	Comments
21	BACR	---	---	----------	----------	---	no	FOR clears GEN A
		---	---	----------	----------	D6	no	Micro off-line clear
		---	---	----------	----------	D7	yes	Micro A GEN clear
23	BACD	A	OB	Off-line	Read	---	no	GEN A clock down
		A	MP	Off-line	Read	D0	no	(BUD is high)
		MP	A	Off-line	Write	D0	no	
		A	MP	----------	Read	D4	yes	
		MP	A	----------	Write	D4	yes	
22	BACU	BS	A	On-line	Write	---	no	GEN A clock up
		A	OB	Off-line	Read	---	no	(BUD is low)
		A	MP	Off-line	Read	D1	no	
		MP	A	Off-line	Write	D1	no	
		A	MP	----------	Read	D2	yes	
		MP	A	----------	Write	D2	yes	
20	BALL	---	---	Off-line	----------	D9	no	GEN A lower load
		---	---	----------	----------	DB	yes	
19	BAUL	---	---	Off-line	----------	DA	no	buffer GEN A upper
		---	---	----------	----------	DC	yes	load
16	BBCR	---	---	----------	----------	---	no	EOR clears GEN B
		---	---	----------	----------	D8	yes	Micro off-line clear
		---	---	----------	----------	D8	yes	Micro B GEN clear
14	BBCD	B	OB	Off-line	Read	---	no	GEN B clock down
		B	MP	Off-line	Read	D0	no	(BUD is high)
		MP	B	Off-line	Write	D0	no	
		B	MP	----------	Read	D5	yes	
		MP	B	----------	Write	D3	yes	
15	BBCU	BS	B	On-line	Write	---	no	GEN B clock up
		B	OB	Off-line	Read	---	no	(BUD is low)
		B	MP	Off-line	Read	D1	no	
		MP	B	Off-line	Write	D1	no	
		B	MP	----------	Read	D3	yes	
		MP	B	----------	Write	D3	yes	
17	BBLL	---	---	Off-line	----------	D9	no	GEN B lower load
		---	---	----------	----------	DD	yes	
18	BBUL	---	---	Off-line	----------	DA	no	buffer GEN B
		---	---	----------	----------	DE	yes	upper load

* A = Buffer; B = Buffer B; BS = Byte Selector; MP = Microprocessor; OB = Output Buffer

Table 2. Input Generator Control Signal Characteristics

Address Generators

Refer to Sheet 2 of the schematics. The two Input Buffer Address Generators consist of AB19, AB28, AB37, V19, V28 and V37. AB19, AB28 and AB37 are cascaded to produce the 12-bit Input Buffer A Address Generator. V19, V28 and V37 serve as the Input Buffer B Address Generator. These counters can be preset via the microprocessor's AD bus. The 8-bit AD bus connects to the eight LSB preset inputs of both generators. The four LSBs of the AD bus also connect to the four MSB preset inputs of both counters.

A particular generator is preset by writing the eight LSBs to the AD bus and strobing the generator's load pin (pin 11) low. Then, the four MSBs are preset by writing them to the four LSBs of the AD bus and strobing pin 11 of AB37 or V37 (generator A or B respectively) low. Each generator has a common clear, clock up and clock down control in addition to the lower and upper load controls. Thus, each generator has five external control inputs. These controls are outputs of the Input Generator Controller.

Generator Controller

The Input Generator Controller consists of PAL 22V10, located at Z32 and shown on sheet 2 of the schematics. Z32 is documented by the PAL equations located in the Supplemental Data Section. The documentation contained here is a functional description of those equations. Table 2 on the adjacent page describes each output of Z32.

BUD, a MUART output signal, controls the incrementing/decrementing of the off-line generator. EOR (End of Record) is an output of X32, and is shown on sheet 4 of the schematics. X32 generates EOR by ANDing the EOF output of the frame sync with ILG (Input Load Gate). ILG, an output of the MUART, is set high at the beginning of the first data frame.

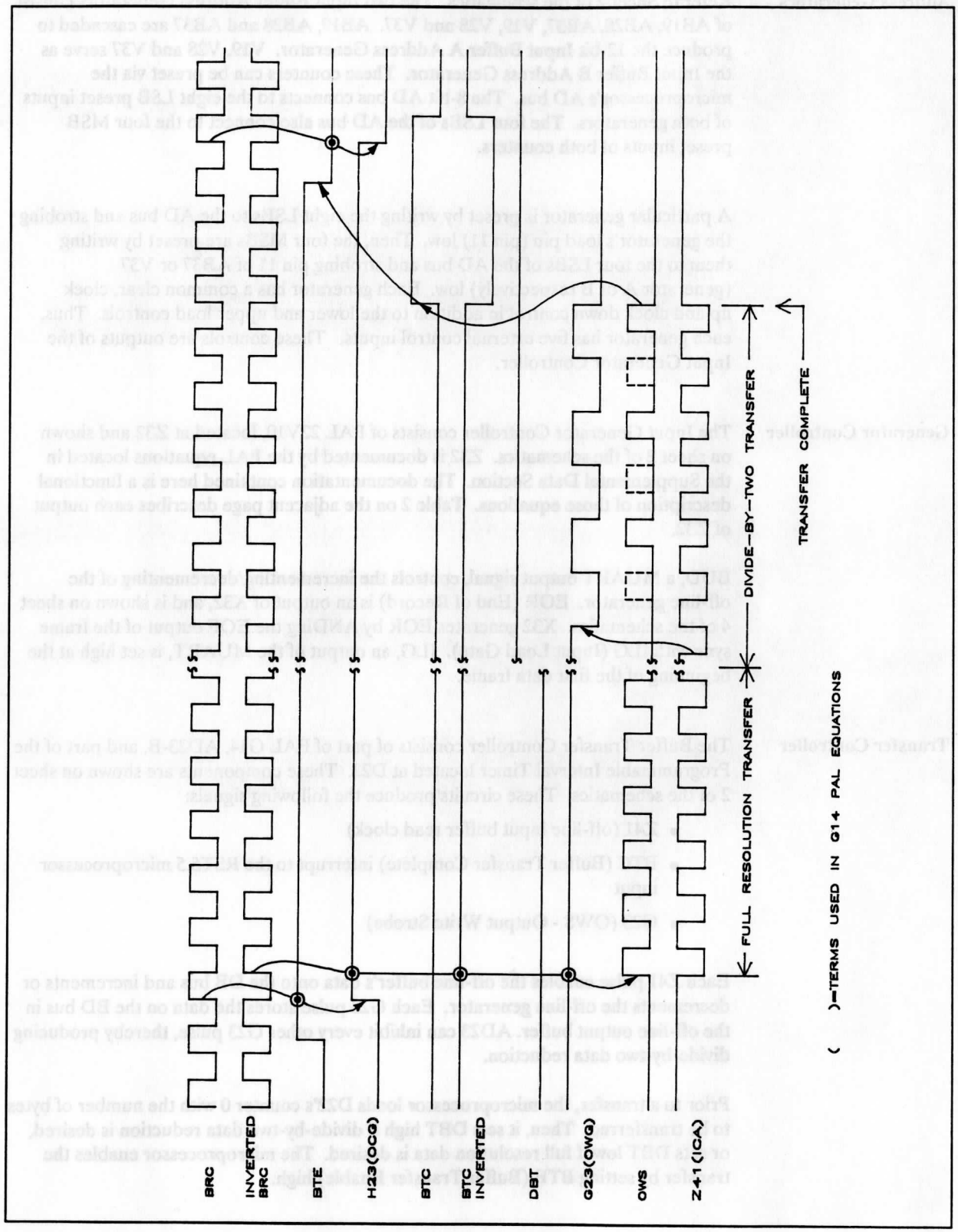
Transfer Controller

The Buffer Transfer Controller consists of part of PAL G14, AD23-B, and part of the Programmable Interval Timer located at D22. These components are shown on sheet 2 of the schematics. These circuits produce the following signals:

- Z41 (off-line input buffer read clock)
- BTC (Buffer Transfer Complete) interrupt to the RST5.5 microprocessor input
- G23 (OWS - Output Write Strobe)

Each Z41 pulse enables the off-line buffer's data onto the DB bus and increments or decrements the off-line generator. Each G23 pulse stores the data on the BD bus in the off-line output buffer. AD23 can inhibit every other G23 pulse, thereby producing divide-by-two data reduction.

Prior to a transfer, the microprocessor loads D22's counter 0 with the number of bytes to be transferred. Then, it sets DBT high if divide-by-two data reduction is desired, or sets DBT low if full resolution data is desired. The microprocessor enables the transfer by setting BTE (Buffer Transfer Enable) high.



Timing Diagram 2. Input to Output Buffer Transfer Controls

Refer to Timing Diagram 2 on the adjacent page. Inverted BRC (Baud Rate Clock) is ANDed with G23 (G14's pin 1 input signal) in the generation of OWS. Thus, G14's pin 10 acts as an OWS pulse gate. If pin 10 is high, OWS pulses are generated; if pin 10 is low, OWS pulses are inhibited. When enabled by H23, a Z41 pulse is generated with each BRC clock pulse regardless of G14's pin 10 level. Z41 increments or decrements the off-line buffer's generator after each data byte transfer. The rising edge of Z41 triggers D-latch AD23-B. If DBT is high, each rising edge of Z41 causes AD23-B to change state, allowing every other OWS pulse to be generated. If DBT is low, AD23-B remains reset, allowing each OWS pulse to be generated.

H23 functions as a "count enable" input to counter zero in D22. When H23 is high, the counter decrements with each OWS pulse. When the counter reaches zero, it raises BTC, interrupting the microprocessor, and inhibiting OWS and Z41 pulses. Upon interrupt, the microprocessor drops BTE, causing H23 to go low on the next rising edge of BRC, completing the transfer cycle.

Tables 1 and 2 show that ports D0H-DEH are used by the microprocessor for input buffer and address generator control. Table 3 below summarizes the I/O port information shown in Tables 1 and 2.

I/O Port	Read/Write	Buffer Function	Generator Function
D0H	Write	Off-line	Decrement
D1H	Write	Off-line	Increment
D2H	Read/Write	Test A	Increment
D3H	Read/Write	Test B	Increment
D4H	Read/Write	Test A	Decrement
D5H	Read/Write	Test B	Decrement
D6H	--	Off-line	Clear
D7H	--	Test A	Clear
D8H	--	Test B	Clear
D9H	--	Off-line	Lower Load
DAH	--	Off-line	Upper Load
DBH	--	Test A	Lower Load
DCH	--	Test A	Upper Load
DDH	--	Test B	Lower Load
DEH	--	Test B	Upper Load
DFH	--	--	(not used)

Table 3. I/O Ports D0H-DFH Summary

N32 PIN#	PAL Term	Data Transfer *Source	Data Transfer *DEST	Active State	Buffer Status On-Line	Buffer Status Off-Line	Buffer Mode Read	Buffer Mode Write	I/O Port	DIAG Test
20	MCDS	IB	C	low	no	yes	no	yes	--	no
		C	MB	high	yes	no	yes	no	--	no
21	MCDE	IB	C	low	no	yes	no	yes	--	no
		C	MB	low	yes	no	yes	no	--	no
18	MDDS	IB	D	low	no	yes	no	yes	--	no
		D	MB	high	yes	no	yes	no	--	no
19	MDDE	IB	D	low	no	yes	no	yes	--	no
		D	MB	low	yes	no	yes	no	--	no
23	WSC	IB	C	low	no	yes	no	yes	--	no
		MP	C	low	no	yes	no	yes	E1	no
		MP	C	low	--	--	no	yes	E2	yes
15	WSD	IB	D	low	no	yes	no	yes	--	no
		MP	D	low	no	yes	no	yes	E1	no
		MP	D	low	--	--	no	yes	E3	yes
17	PDDS	MP	C/D	low	no	yes	no	yes	E1	no
				low	--	--	no	yes	E2	yes
				low	--	--	no	yes	E3	yes
22	PDCE	C	MP	low	no	yes	yes	no	E1	no
		MP	C	low	no	yes	no	yes	E1	yes
		C	MP	low	--	--	yes	no	E2	yes
		MP	C	low	--	--	no	yes	E2	yes
16	PDDE	D	MP	low	no	yes	yes	no	E1	no
		MP	D	low	no	yes	no	yes	E1	no
		D	MP	low	--	--	yes	no	E3	yes
		MP	D	low	--	--	no	yes	E3	yes

* IB = Input Buffer (off-line)
C = Buffer C
D = Buffer D
MB = Multibus
MP = Microprocessor

Table 4. Output Buffer Controller Signal Characteristics

Table 4 on the adjacent page describes the function of each output signal. This table is derived from N32's PAL equations located in the Supplemental Data Section.

Output Buffer Section

The Output Buffer Section is shown on sheet 3 of the schematics. Much of the hardware in this section is identical to corresponding hardware in the Input Buffer Section. Where applicable, documentation of some subsections of the Output Buffer Section will consist of a reference to a corresponding section in the Input Buffer Section.

C and D

Output Buffers C and D consist of N10 and N21 (Buffer C), and R10 and R21 (Buffer D). Refer to Input Buffers A and B.

Data Flow Director

N21, R1, J37, L37, T23 and T34 form the Output Buffer Data Flow Director. Refer to the Input Buffer Data Flow Director.

Controller

The Output Buffer Controller consists of PAL P22V10A located at N32. N32 produces chip enables and direction control signals for N1, R1, J37, L37, T23 and T34. It also generates the write enable pulses for the output buffers.

Address Generator

The Address Generator for Buffer C consists of L1 and L10; the address generator for Buffer D consists of L19 and L28. Since the generators are identical, only L1 and L10 will be described.

L1 and L10 are 8-bit counters. These chips have internal storage registers with tri-state parallel outputs. The counters increment on the rising edge of the pin 11 input signal. Counter contents transfer to the storage register on the rising edge of the pin 13 signal. These chips have a direct clear input.

L1 and L10 are cascaded to yield a 16-bit generator (only 12 bits are used). L1 drives the eight LSB address inputs of Buffer C while L10 drives the four MSBs. The counter clock (pin 11) and the register clock (pin 13) are driven by the same signal source. Pin 11 is driven directly by R32 pin 22. R32's pin 22 drives inverter J15-B in addition to pin 11 of each generator chip. J15-B drives the register clock input of each generator chip. Thus, the generator increments on the rising edge of the counter clock, and transfers its count to its storage register on the falling edge of the counter clock.

R32 PIN#	PAL Term	Data Transfer *Source	Data Transfer *DEST	Buffer Status On-Line	Buffer Status Off-Line	Buffer Mode Read	Buffer Mode Write	I/O Port	Diag Test	Comments
22	MCCC	C	MP	no	yes	yes	no	E1	no	Counter C
		MP	C	no	yes	no	yes	E1	no	Clock
		C	MP	--	--	yes	no	E2	yes	
		MP	C	--	--	no	yes	E2	yes	
		C	MB	yes	no	yes	no	--	no	
		IB	C	no	yes	no	yes	--	no	
		--	--	no	yes	--	--	E4	no	
		MP	C	--	--	no	yes	E5	yes	
23	MCCR	--	--	--	--	--	--	E4	no	Counter
		--	--	--	--	--	--	E5	yes	C Reset
20	MDCC	D	MP	no	yes	yes	no	E1	no	Counter D
		MP	D	no	yes	no	yes	E1	no	Clock
		D	MP	--	--	yes	no	E3	yes	
		MP	D	--	--	no	yes	E3	yes	
		D	MP	yes	no	yes	no	--	no	
		IB	D	no	yes	no	yes	--	no	
		MP	D	no	yes	no	yes	E4	no	
		MP	D	--	--	no	yes	E6	yes	
21	MDCR	--	--	--	--	--	--	E4	no	Counter D
		--	--	--	--	--	--	E6	yes	Reset

* MP = Microprocessor
IB = Input buffer (off-line)
MB = Multibus
C = Buffer C
D = Buffer D

Table 5. Output Generator Controller Signal Characteristics

Controller

The Output Generator Controller consists of a PAL22V10A, located at R32. R32 produces the clear strobes and clock signals for both Output Buffer Address Generators.

The signal OBS (Output Buffer Switch) is an input to R32. The microprocessor, via the MUART, controls OBS. OBS determines the online/ offline buffer counter and address generator status. The chart below defines OBS.

OBS Level	On-line	Off-line
High	Buffer C Gen	Buffer D Gen
Low	Buffer D Gen	Buffer C Gen

Table 5 on the adjacent page describes the four output signals of R32. This table is generated from the PAL equations for R32 located in the Supplemental Data Section.

Tables 4 and 5 show that the microprocessor uses ports E0-E6 for output buffer and address generator control. Table 6 below summarizes the I/O port information shown in Tables 4 and 5.

I/O Port	Read/Write	Function
E1	Write	MP writes to off-line buffer and increments off-line address generator
	Read	MP reads off-line buffer and increments off-line address generator
E2	Write	MP writes to Buffer C and increments Buffer C Address Generator
	Read	MP reads Buffer C and increments Buffer C Address Generator
E3	Write	MP writes to Buffer D and increments Buffer D Address Generator
	Read	MP reads Buffer D and increments Buffer D Address Generator
E4	--	Reset off-line buffer's Address Generator
E5	--	Reset Buffer C Address Generator
E6	--	Reset Buffer D Address Generator

Table 6. I/O Ports E1 - E6 Summary

MICROPROCESSOR SECTION

The Microprocessor Section is shown on sheet 4 of the schematics. It includes:

- Microprocessor
- Lower Address Latch
- Memory and I/O Mapper
- RAM
- EPROM
- Programmable Interval Timer
- MUART
- Clock

Microprocessor

The microprocessor is an Intel 8085 8-bit microprocessor located at A1. Microprocessor theory is not described in this document, as you should already be knowledgeable in microprocessor based systems. If you need additional microprocessor theory, refer to the Microprocessor Section of the Detailed Functional Description. Microprocessor description is limited to interaction with peripheral components.

Lower Address Latch

The Lower Address Latch consists of a transparent D-type latch located at E35. E35's enable pin (pin 11) is driven by the 8085's ALE (Address Latch Enable) signal. The 8085's AD (Address/Data) bus drives the eight D-inputs of E35; ALE drives the latch pin (pin 11). ALE goes high when the AD bus carries the eight LSBs of an address. When ALE goes high, E35 passes its input data to its output port (A0-A7). When ALE returns low, E35 latches the input data. ALE returns low before the data on the AD bus changes.

Memory & I/O Mapper

The Memory and I/O Mapper consist of parts of R32 and N32. The remainders of R32 and N32 serve as the Output Generator Controller and the Output Buffer Controller. Both chips are driven by the four MSBs of the 8085's address bus. RD and WR restrict some outputs to read only or write only addresses. Table 7 on the next page summarizes the outputs of R32 and N32. Note on sheet 4 of the schematics that the 8085's A15 pin (pin 28) serves as a chip enable for A22. This assigns the first 32K bytes of memory space to A22, the EPROM.

Address	MEM/IO	Function
0000H-7FFFH	MEM Read	Firmware EPROM
8000H-8FFFH	MEM Read/write	RAM
9000-9FFFH	(not used)	
A0H-AFH	I/O Read	Control Register
B0H-BFH	I/O Read/write	Programmable Interval Timer Control
C0H-CFH	I/O Read/write	MUART Control
D0H-DFH	I/O Read/write	Input Buffer Control
E0-EFH	I/O Read/write	Output Buffer Control
F0H-FFH	I/O Read	Command Port Read
F0H-FFH	I/O Write	Status Port Write

Table 7. Memory and I/O Map

RAM

The 1K byte RAM (Random Access Memory) is located at C36. The 8085's AD bus connects directly to C36. C36 contains an internal demultiplexer controlled by the 8085's ALE pin. The demultiplexer separates the eight LSBs of the address from the data. The two address MSBs (A8 and A9) are driven directly by the 8085's A8 and A9 address pins (pins 21 and 22 respectively). C36's chip select pin (pin 14) is driven by an output from the Memory and I/O Mapper. This signal goes low for addresses 8000H-8FFFH.

EPROM

The EPROM (Eraseable Programmable Read Only Memory) consists of A22. A22 contains the ingestor's firmware, and is organized as 8K by eight bits. The tri-state output of A22 is enabled when the 885's A15 output signal (pin 28) is low. Thus, A22 is enabled for memory addresses -7FFFH. The Lower Address Latch drives the eight LSB address inputs of A22; the 885's A8-A12 (pins 21-26) signals drive the five MSB address inputs.

PIT

The PIT (Programmable Interval Timer) consists of D22, which contains three 16-bit programmable timer/counters. Each timer/counter has an input, an output and a gate. Timer/counters 1 and 2 are cascaded to provide a 32-bit counter. Timer/counter 1 is clocked by BRC, the 3.072 MHz Baud Rate Clock. This timer/counter is programmed to divide BRC by 30,720, yielding an output of 100 Hz at pin 15. The output of timer/counter 1 drives the clock input of timer/counter 2.

Timer/counter 2 is programmed to divide its input by 900, producing a 90 second timer. The output of timer/counter 2 interrupts the 8085 via the MUART's external interrupt input pin (pin 16). The 90 second timer is used during signal acquisition. If the frame sync acquires lockon within 90 seconds of expected lockon, the 8085 shuts off timer/counter 2, preventing the interrupt.

Timer/counter 1 is always enabled because its gate is pulled high. Timer/counter 2 is enabled via the ILG control signal output from pin 38 on the MUART. Thus, after the timer/counters are programmed, timer/counter 2 does not begin to count down until it is enabled by ILG.

Timer/counter zero is part of the Buffer Transfer Controller. It is described in that section.

D22 is programmed by the 8085 via the AD bus. Timer status and count value can also be read via the AD bus. A0 and A1 (pins 19 and 20 respectively) select the counter to be programmed or read. D22's chip select (pin 17) is driven by an output of the Memory and I/O Mapper. It goes low when the 8085 writes to or reads from I/O ports B0H-B3H.

MUART

The MUART (Multifunction Universal Asynchronous Receiver-Transmitter) is located at D1 on sheet 4 of the schematics. Refer to the Detailed Functional Description and the *Intel Microprocessor and Peripheral Handbook* for programming and additional functional information on the MUART.

D1's chip select pin (pin 13) is driven by an output of the Memory and I/O Mapper. It goes low for port addresses C0H-CFH. The chip select pin enables the tri-state bidirectional data port (pins 1-8) which connects directly to the 8085's AD bus. The data port provides access to 32 internal command/control/status registers in D1. The AD bus is multiplexed. D1 demultiplexes the address and data with the aid of the 8085's ALE signal. When ALE goes low, the four LSBs of the AD bus are latched into D1's internal address register. These four bits (the four LSBs of the I/O address) select one of 16 register pairs. The active RD or WR signal selects the read or write register within the register pair while the AD bus acts as a data sink or source.

Port 2 of D1 is not used. By writing a byte of data to register 4 (C4H), each bit in Port 1 can be configured as an input or an output pin. (If a bit is high, the corresponding Port 1 pin is an output pin.) However, Port 1 is unique in that each pin has a special function that can be enabled via other registers. Only when the special function is disabled does the respective pin act as a general I/O pin, as specified by register 4.

The special function is enabled for Port 1 pins 5 and 7 (P15 and P17 respectively). P15 retriggers timer 5 in D1, forcing it to start a new time out. P15 is driven by DAK (Data Acknowledge), the ingestor's acknowledge of the frame sync's input data. If the frame sync stops sending data, DAK fails to retrigger the counter. When counter 5 times out, it interrupts the microprocessor, informing the microprocessor of a loss of signal. P17 interrupts the 8085 when LOCK/ goes high, indicating that the frame sync lost lock.

P10-P14 and P16 are general purpose I/O pins. They are configured as output pins and are described in Table 8 below.

Port	Control Signal	Comments
P10	DBT	Controls the Divide-By-Two data sampling feature in the Buffer Transfer Controller.
P11	ILG	ILG (Input Lead Gate) is set high while receiving a record.
P12	OBS	OBS (Output Buffer Switch) selects the on-line output buffer. If OBS is high, Buffer C is on-line, Buffer D is off-line.
P13	BUD	BUD (Buffer Up/Down) selects incrementing or decrementing of the input buffer's off-line address generator. If BUD is high, the off-line generator decrements with each byte transfer to the off-line output buffer.
P14	LBC	LBC (Lower Bit Control) controls the passing of the two LSBs when transferring data from the input buffer to the output buffer. If BUD is high, the two LSBs are passed. If BUD is low, only the six MSBs are passed (the two LSBs are held high).
P16	DPF	DPF (Data Present Flag) is a Status Register input.

Table 8. MUART Port I/O Assignments

The Asynchronous Receiver-Transmitter data pins are pins 19 and 23.

D1 receives and sends serial asynchronous data on pins 19 (RXD) and 23 (TXD) respectively. These signals are TTL levels. They are converted to RS232 levels by AD6. AD6 generates 12 volts from the +5 volt Vcc input, eliminating the need for a separate ±12 volt supply.

Clock

All clock signals on the ingestor are submultiples of 18.432 MHz. AD15 is a crystal controlled 18.432 MHz oscillator. It generates a square wave clock input to A37. A37, a quad D-type flip-flop, is configured as two frequency dividers. A37 section 4 divides the 18.432 MHz by two, producing a 9.216 MHz biphase clock input to the 8085. The remaining three sections of A37 are configured as a divide-by-six circuit. This circuit is driven by the 18.432 MHz output of AD15. BRC (Baud Rate Clock), the output of the divide-by-six circuit, is a 3.072 MHz square wave. It clocks the MUART, the PIT, and the Frame Sync Interface Controller (G14).

Multibus Interface

The Multibus Interface is shown on sheet 5 of the schematic. Refer to Figure 2 and the Detailed Functional Description as necessary.

The Multibus Interface includes:

- Multibus I/O Mapper
- Command Port
- Status Port
- Control Port

Multibus I/O Mapper

The Multibus I/O Mapper consists of PAL 22V10A located at G1. Refer to the PAL equations for G1 in the Supplemental Data Section.

G1 generates control signals that are Multibus I/O mapped. This is accomplished in two stages. In the first stage, G1 determines if I/O addresses on the Multibus are intended for this ingestor. An internal signal called CAD (refer to G1's PAL equations) goes low for the I/O address intended for this ingestor. CAD is an input to the second stage of control signal generation. Here, CAD acts as an enable signal in a decoder that decodes the two LSBs of the I/O address along with IORC and IOWC, to produce five I/O mapped controls.

ADR2/-ADR7/ and AS1-AS3 are inputs to the CAD generator. CAD goes low if all of the following conditions are simultaneously met:

- ADR7/ is low
- ADR6/ is high
- ADR5/ does not match AS3
- ADR4/ does not match AS2
- ADR3/ does not match AS1
- ADR2/ is high

Switches AS1-AS3 cause their respective input to G1 to go low if the switch is closed. If the above list of conditions is to be satisfied, the respective Multibus address input must be high (false) for a closed switch and low (true) for an open switch. The following chart defines the assigned Multibus address for the ingestor. Multibus Address inputs are shown noninverted.

A D R 7	A D R 6	A S 3	A S 2	A S 1	A D R 2	*A D R 1	*A D R	ADDRESS
1	0	0	0	0	0	X	X	80H-83H
1	0	0	0	1	0	X	X	88H-8BH
1	0	0	1	0	0	X	X	90H-94H
1	0	0	1	1	0	X	X	98H-9BH
1	0	1	0	0	0	X	X	A0H-A4H
1	0	1	0	1	0	X	X	A8H-ABH
1	0	1	1	0	0	X	X	B0H-B4H
1	0	1	1	1	0	X	X	B8H-BBH

* X = Don't care

Note that CAD responds to four consecutive I/O addresses because the two LSBs of the Multibus address bus are not monitored by CAD. If the lowest address of an I/O block is referred to as the "base address", then each address within that block can be referred to by its offset (i.e., I/O port 81H is base (80H) plus 1). Now, the five I/O control outputs of G1 can be defined. These signals, with their offsets and functions are shown in Table 9 below and explained in the sections in which they are used.

Signal	Output Pin	Offset	Function
ORS	20	00	Output Buffer Read Strobe
MPW	21	00	Command Port Write Strobe
MSR	22	01	METEOSAT Status Port Read Strobe
CDI	17	01	Control Port Write and Interrupt
CRI	16	02	Control Reset Interrupt

Table 9. I/O Interface Control Signals

Command Port

The Command Port consists of two cascaded 4-bit by 16 word FIFOs (First In - First Out memory). They are located at G27 and G36. The two FIFOs function as an 8-bit by 16 word FIFO, with G27 storing the least significant nibbles and G36 storing the most significant nibbles. The Command Port stores Multibus transported commands. These commands are limited to a maximum length of 16 bytes each.

Each FIFO functions as a 16-nibble RAM with separate read and write address generators. The address generators are four bit binary up counters. These counters increment after each data nibble is stored or read. Once a counter reaches a full count (1111B), it rolls over to zero on the next increment. Data may be stored until the storage address generator catches up to the read address generator (FIFO is full).

Likewise, data may be read until the read address generator catches up to the write address generator (FIFO is empty). Once the FIFO is full, it will not accept additional data. An empty FIFO does not respond to additional read cycles.

Each FIFO has separate write and read strobe pins. When pin 3 goes low, the data on D0-D3 (pins 4-7) is loaded into the next cell in the FIFO (providing the FIFO isn't already full). When pin 15 goes low, the contents of the data cell, pointed to by the read address generator, is written to the AD bus.

The load pin (pin 3) goes low when the GPCI writes to the ingestor's base address. The unload pin (pin 15) goes low when the microprocessor reads port FFH. Before reading port FFH, the microprocessor tests PRI to be sure that it is high. PRI is high unless the FIFO is empty. When the microprocessor is informed that a new command is present in the Command Port, it executes port FFH read instructions until PRI goes low, indicating the Command Port is empty.

Status Port

The Status Port consists of J15 and part of a PAL located at AD31. The microprocessor writes status data to the status port; the Multibus periodically reads the Status Port.

When the Multibus reads the base address plus one, MSR (pin 22 of G1) goes low, enabling AD31 and J15. The outputs of AD31 and J15 connect to the Multibus data bus. The following chart defines the status bits.

Multibus Bit	Definition
DAT7/	undefined - always high
DAT6/	undefined - always high
DAT5/	undefined - always high
DAT4/	undefined - always high
DAT3/	undefined - always high
DAT2/	Data Present Flag (DPF)
DAT1/	Exception
DAT0	Busy

AD31 sets DAT4/-DAT7/ high when it is enabled. AD31 also contains the combinatorial logic that generates the Busy and Exception status bits. AD31 passes these Status signals to J15. J15 drives the lower four bits of the Multibus data bus. The three active status bits (DPF, Busy and Exception) are described below.

DPF (Data Present Flag) is an output from the MUART. The 8085 asserts this bit when the on-line output buffer holds a record of Multibus requested data. The Multibus periodically polls ingestor status. Upon detection of the DPF bit, the GPCI performs a DMA transfer from the ingestor's on-line output buffer to the IBM channel.

The Busy Flag is set automatically by the Multibus I/O Mapper when the Multibus writes to the Control Port (base address plus one). The Busy Flag is also set by a Multibus Initialization and a Multibus Reset command. This flag remains set until the ingestor completes execution of the present command. At the completion of a command, the 8085 clears Busy and sets the DPF if the command was executed successfully or sets Exception Flag if the command execution was unsuccessful.

Control Port

The Control Port consists of an octal D-type tri-state latch located at J26. J26's data inputs connect to the Multibus' data bus (DAT0-DAT7/); its outputs connect to the 8085's AD bus (AD0-AD7).

The Multibus latches data into J26 by writing to the ingestor's base address plus one. This asserts CDI, latching J26. It also interrupts the microprocessor by causing an RST6.5 Restart. Within the RST6.5 Restart interrupt routine, the 8085 reads port A0H, causing CRS/ to be asserted. When CRS is asserted, J26 drives the AD bus, presenting the control data to the 8085. The control output bits of J26 are defined as follows.

Bit	Definition
AD0	Command Ready (new command)
AD1	Clear (present command)
AD2-AD7	Undefined

Supplemental Data

This Supplemental Data section contains:

- an explanation of the PAL equation listings
- the symbols and abbreviations used in the equations
- seven PAL equations
- Schematic drawings 1 through 5 (6450-0537)
- Assembly drawing 1 (6450-0538)

PAL Equation Listings

The listings for the logic equations used in the Programmable Array Logic Devices are explained below.

Title

Each device has a printout that begins with the title page. On this page the device is called out by its location and device name.

Declarations

Declarations lists the logic conventions and format for the signal names. The signal names are in uppercase letters and numbers.

The first group of signal names refers to the power and ground rails. The respective pin numbers that make these connections are given in the line below the signal names.

The second group of signal names refers to the input signals received by the device. The respective pin numbers assigned to receive these inputs are given in the line below the signal names.

The third group of signal names refers to the outputs from the PAL. The respective pin numbers assigned to each output are given in the line below the signal names.

Equations

The logic equations used to generate each signal are shown in their highest order form.

Symbols and Abbreviations

The following is an example of a PAL equation.

```
!SNV :  =   !SM0 & !SM1 & (Address > = ^h1E)
        #   SM0 $ (Address = = ^hFF)
```

Below is an explanation of the symbols and abbreviations used in the equation.

Symbol/Abbreviation	Explanation
!	The one's complement of, e.g. !SNV = (SNV)
:	A register latched signal. Valid on rising edge of register clock.
&	Logical AND
#	Logical OR
$	Exclusive OR
Address > = ^h1E	Combined terms simplify to a value greater than or equal to 1E Hexadecimal.
Address = = ^hFF	Combined terms are equal to FF Hexadecimal.

P22V10 Located at G1

Title

Multibus Address Decoder
EWS SSEC Madison, WI 8/24/87

Identification

Device location G1
Device type P22V10

Module

MPIMAD
flag r0

Declarations

```
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
            pin 12, 24

ADR7, ADR6, ADR5, ADR4, ADR3, ADR2, ADR1, ADR0, IORC, IOWC, AS3
            pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

AS2, AS1, CRS, CRI, MCW, RACK, CAD, ORS, MPW, MSR, WACK
            pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23
```

Equations

```
enable WACK = !CAD & !IOWC

WACK =   CAD

!MSR  =  !CAD & !IORC & !ADR0 & ADR1

MCW   =  !CAD & !IOWC & !ADR0 & ADR1          "SET
       # MCW & CRS                             "HOLD / RESET

ORS   =  !CAD & !IORC & ADR0 & ADR1

MPW   =  !CAD & !IOWC & ADR0 & ADR1

!CRI  =  !CAD & !IOWC & ADR0 & !ADR1

CAD   =  ADR7
       # !ADR6
       # !ADR5 & !AS3
       # ADR5 & AS3
       # !ADR4 & !AS2
       # ADR4 & AS2
       # !ADR3 & !AS1
       # ADR3 & AS1
       # !ADR2
```

```
enable RACK = !CAD & !IORC

RACK  =    CAD
```

P22V10 Located at G14

Title

Load Controller
EWS SSEC Madison, WI 1/5/88

Identification

Device location G14
Device type P22V10

Module

MPILC
flag r0

Declarations

TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 12, 24

CLK, ILG, DRF, LOCK, DI1, DI0, LBC, BTE, BTC, OWG, OR1
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

OR2, PRI, OCG, OWS, ICA, BD0, BD1, ILC, ACK, SEL, IDG
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations

```
!ACK  :=  !DRF & LOCK & !IDG

SEL   :=  IDG & !SEL

IDG   :=  !ACK
      #   IDG & !SEL

ILC   =   !CLK & IDG & ILG

!BD1  =   !DI1 & LBC

!BD0  =   !DI0 & LBC

!ICA  =   !CLK & OCG & !BTC

OWS   =   !CLK & OCG & OWG & !BTC

OCG   :=  BTE

PRI   =   OR1 & OR2
```

P22V10 Located at N32

Title

Output Buffer Decoder
EWS SSEC Madison, WI 4/8/87

Identification

Device location N32
Device type P22V10

Module

MPIOBD
flag r1

Declarations

```
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C

GND, VCC
        pin 12, 24

OBS, ORS, OWS, A2, A1, A0, WR, A12, A13, A14, A15
        pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

RD, MPR, WSD, PDDE, PDDS, MDDS, MDDE, MCDS, MCDE, PDCE, WSC
        pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = A15, A14, A13, A12, X, A2, A1, A0
```

Equations

```
!WSC   =   !OBS & OWS
         # !OBS & !WR & (Address = = ^hE1)
         # !WR & (Address = = ^hE2)

!PDCE  =   !OBS & !RD & (Address = = ^hE1)
         # !OBS & !WR & (Address = = ^hE1)
         # !RD & (Address = = ^hE2)
         # !WR & (Address = = ^hE2)

!MCDE  =   OBS & ORS
         # !OBS & OWS

!MCDS  =   !OBS & OWS

!MDDE  =   !OBS & ORS
         # OBS & OWS

!MDDS  =   OBS & OWS

!PDDS  =   !WR & ((Address > = ^hE1) & (Address < = ^hE3))
```

```
!PDDE  =   OBS & !RD & (Address = = ^hE1)
         #  OBS & !WR & (Address = = ^hE1)
         #  !RD & (Address = = ^hE3)
         #  !WR & (Address = = ^hE3)

!WSD   =   OBS & OWS
         #  OBS & !WR & (Address = = ^hE1)
         #  !WR & (Address = = ^hE3)

!MPR   =   !RD & A15 & A14 & A13 & A12
```

P22V10 Located at R32

Title

Output Counter/Port Decoder
EWS SSEC Madison, WI 4/8/86

Identification

Device location R32
Device type P22V10

Module

MPIOCPD
flag r1

Declarations

```
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C

GND, VCC
        pin 12, 24

OBS, ORS, OWS, A2, A1, A0, WR, A12, A13, A14, A15
        pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

RD, RAM, CRS, PCS, MCS, IBC, SWR, MDCC, MDCR, MCCC, MCCR
        pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = A15, A14, A13, A12, X, A2, A1, A0
```

Equations

```
MCCC =   !OBS & !RD & (Address = = ^hE1)
       # !OBS & !WR & (Address = = ^hE1)
       # !RD & (Address = = ^hE2)
       # !WR & (Address = = ^hE2)
       # OBS & ORS
       # !OBS & OWS
       # !OBS & !WR & (Address = = ^hE4)        " CLEAR TERMS
       # !WR & (Address = = ^hE5

!MCCR =  !OBS & !WR & (Address = = ^hE4)
       # !WR & (Address = = ^hE5)

MDCC =   OBS & !RD & (Address = = ^hE1)
       # OBS & !WR & (Address = = ^hE1)
       # !RD & (Address = = ^hE3)
       # !WR & (Address = = ^hE3)
       # !OBS & ORS
       # OBS & OWS
       # OBS & !WR & (Address = = ^hE4)        " CLEAR TERMS
       # !WR & (Address = = ^hE6)
```

```
!MDCR =   OBS & !WR & (Address = = ^hE4)
        #  !WR & (Address = = ^hE6)

SWR   =   !WR & A15 & A14 & A13 & A12

IBC   =   A15 & A14 & !A13 & A12

!MCS  =   A15 & A14 & !A13 & !A12

!PCS  =   A15 & !A14 & A13 & A12

!CRS  =   !RD & A15 & !A14 & A13 & !A12

!RAM  =   A15 & !A14 & !A13 & !A12
```

P22V10 Located at X32

Title

Input Buffer Control
EWS SSEC Madison, WI 12/30/87

Identification

Device location X32
Device type P22V10

Module

MPIIBC
flag r1

Declarations

```
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
        pin 12, 24

WR, RD, A0, A1, A2, A3, IBC, IBS, ILC, EOF, ILG
        pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

EOR, WSB, PDBE, PDDS, MBDS, MBDE, MADS, MADE, PDAE, WSA
        pin 14, 15, 16, 17, 18, 19, 20, 21, 22, 23


Address =   A3, A2, A1, A0
Read    =   !RD & IBC
Write   =   !WR & IBC
```

Equations

```
!WSA  =   !IBS & !ILC
        # IBS & Write & ((Address = = ^h0) # (Address = = ^h1))
        # Write & ((Address = = ^h2) # (Address = = ^h4))

!MADS =   !IBS & !ILC

!MADE =   !IBS & !ILC
        # IBS

!PDAE =   IBS & Read & ((Address = = ^h0) # (Address = = ^h1))
        # IBS & Write & ((Address = = ^h0) # (Address = = ^h1))
        # Read & ((Address = = ^h2) # (Address = = ^h4))
        # Write & ((Address = = ^h2) # (Address = = ^h4))

!PDDS =   Write & ((Address > = ^h0) & (Address < = ^h5))
```

```
PDBE   =   !IBS & Read & ((Address = = ^h0) # (Address = = ^h1))
         # !IBS & Write & ((Address = = ^h0) # (Address = = ^h1))
         # Read & ((Address = = ^h3) # (Address = = ^h5))
         # Write & ((Address = = ^h3) # (Address = = ^h5))

!MBDE =   IBS & !ILC
         # !IBS

!MBDS =   IBS & !ILC

!WSB   =   IBS & !ILC
         # !IBS & Write & ((Address = = ^h0) # (Address = = ^h1))
         # Write & ((Address = = ^h3) # (Address = = ^h5))

!EOR   =   !EOF & ILG
```

P22V10 Located at Z32

Title

Input Counter Control
EWS SSEC Madison, WI 12/30/87

Identification

Device location Z32
Device type P22V10

Module

MPIICC
flag r1

Declarations

```
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
        pin 12, 24

RD, WR, A0, A1, A2, A3, IBC, ICC, BUD, ICA, EOR
        pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

IBS, BBCD, BBCU, BBCR, BBLL, BBUL, BAUL, BALL, BACR, BACU, BACD
        pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23


Address =   A3, A2, A1, A0
Read    =   !RD&IBC
Write   =   !WR&IBC
```

Equations

```
BACR  =   !EOR
        #  IBS & Write & (Address = = ^h6)
        #  Write & (Address = = ^h7)

!BACD =   IBS & !ICA & BUD
        #  IBS & Read & (Address = = ^h0)
        #  IBS & Write & (Address = = ^h0)
        #  Read & (Address = = ^h4)
        #  Write & (Address = = ^h4)

!BACU =   !IBS & ICC
        #  IBS & !ICA & !BUD
        #  IBS & Read & (Address = = ^h1)
        #  IBS & Write & (Address = = ^h1)
        #  Read & (Address = = ^h2)
        #  Write & (Address = = ^h2)
```

```
!BAUL =   IBS & Write & (Address = = ^hA)
        #  Write & (Address = = ^hC)

!BALL =   IBS & Write & (Address = = ^h9)
        #  Write & (Address = = ^hB)

!BBLL =   !IBS & Write & (Address = = ^h9)
        #  Write & (Address = = ^hD)

!BBUL =   !IBS & Write & (Address = = ^hA)
        #  Write & (Address = = ^hE)

!BBCU =   IBS & ICC
        #  !IBS & !ICA & !BUD
        #  !IBS & Read & (Address = = ^h1)
        #  !IBS & Write & (Address = = ^h1)
        #  Read & (Address = = ^h3)
        #  Write & (Address = = ^h3)

!BBCD =   !IBS & !ICA & BUD
        #  !IBS & Read & (Address = = ^h0)
        # !IBS & Write & (Address = = ^h0)
        #  Read & (Address = = ^h5)
        #  Write & (Address = = ^h5)

BBCR =    !EOR
        #  !IBS & Write & (Address = = ^h6)
        #  Write & (Address = = ^h8)
```

P22V10 Located at AD31

Title

Busy Flag Logic
EWS SSEC Madison, WI 12/30/87

Identification

Device location AD31
Device type P22V10

Module

MPIBFL
flag r0

Declarations

```
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND,VCC
        pin 12, 24

INIT, AD0, AD1, MSR, CRI, CDI, SWS, DAK, WC0, WC1, WC2
        pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

WC3, WC4, FIG, ACK, EXCP, BSY, DAT4, DAT5, DAT6, DAT7, RST
        pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23
```

Equations

```
!RST = !INIT

enable DAT7 = !MSR

!DAT7 = FALSE

enable DAT6 = !MSR

!DAT6 = FALSE

enable DAT5 = !MSR

!DAT5 = FALSE

enable DAT4 = !MSR

!DAT4 = FALSE

!EXCP =   SWS & !AD1                          "LOAD
        # !SWS & !EXCP                        "HOLD

!BSY  =   !BSY & !CDI & CRI & INIT            "SET / HOLD
        # SWS & !AD0                          "RESET
```

```
ACK   =   DAK                                    "LINE BUFFER

FIG   =   WC0 & WC1 & WC2 & WC3 & WC4
```

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

GND J2-2
GND J2-4
GND J2-6

D7 J2-17
D15 J2-1
D6 J2-19
D14 J2-3
D5 J2-21
D13 J2-5
D4 J2-23
D12 J2-7

74 LS 158 Z1

D3 J2-25
D11 J2-9
D2 J2-27
D10 J2-11
D1 J2-29
D9 J2-13
D4 J2-31
D8 J2-15

74 LS 158 X1

GND J2-8
GND J2-10
GND J2-12
GND J2-14
GND J2-16
GND J2-20
GND J2-24

AF9

SHT. 2 ILC
+5V
SHT. 4 BKC
SHT. 4 ILG
DRF/ J2-22
ACK/ J2-26
SHT. 4 DAK
LOCK/ J2-34
SHT. 4 LOCK/
J15 74LS240
J20
K21
K1
K2
K4
1K

P22V10 G14

BAA0
BAA1
BAA2
BAA3
BAA4
BAA5
BAA6
BAA7
BAA8
BAA9
BAAA
BAAB
SHT. 2

1420 -55 Z10
1420 -55 Z21

GND J2-24
GND J2-28
GND J2-32
GND J2-33
GND J2-35
GND J2-37

SHT. 2 I B3 I B2 I B1 I B0
SHT. 2,3&4 A3 A2 A1 A0
SHT. 2,3&4 RD RW

8216 AB1
8216 AB10
X32 P22V10
8216 V1
8216 V10

BD7
BD6
BD5
BD4
BD3
BD2
SHT. 3
BD1
BD0
LBC SHT. 4

P22V10 G14

1420 -55 X10
1420 -55 X21

BBA0
BBA1
BBA2
BBA3
BBA4
BBA5
BBA6
BBA7
BBA8
BBA9
BBAA
BBAB
SHT. 2

T12 74 LS 640
T1 74 LS 640

AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
μ BUS
SHTS. 2,3,4 &5

INPUT BUFFERS MOD. J

THE UNIVERSITY OF WISCONSIN
SPACE SCIENCE & ENGINEERING CENTER
MADISON, WISCONSIN

TITLE MCIDAS
METEOSTAT PDUS INGESTOR
SCHEMATIC DIAGRAM

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N.A.	D.FORD	3-4-87				4-24-88
NEXT HIGHER ASSEMBLY 10538	PRODUCT ASSURANCE	DATE	PROJECT APPROVAL	DATE		
PROJECT NO 1025	SIZE D	SHEET 1 OF 5	DRAWING NO 6450-0537			

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

SHT. 1 IBS
SHT. 4 EOR
SHT. 1,4 RD
SHT. 1,4 WR
SHTS. 1,3,4 A0 A1 A2 A3
SHT. 1,4 IBC
SHT. 4 BUD
SHT. 4 BTE
SHT. 3 ONS
SHT. 4 BTC
SHT. 4 DBT
SHT. 1 ILC

EOR

AD26 AD24 AD25 AD23 AD28 — 74LS74 A

232 PAL 22V10

AA43 AA33 AA34 AA35 AA36 AA37 AA38 AA39 AA40 AA41 AA42

AB22 AB23 AB31 AB32 AB40 AB41 — 74LS193

AC21 AC20 AC19 AC25 AC26 AC22 AC23 AC24 AC30 AC29 AC28 AC34 AC35 AC31 AC32 AC33 AC39 AC38 AC37 AC43 AC44 AC42

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 — μ BUS SHTS. 1,3,4 & 5

SHT. 1

V21 V20 V24 V25 V23 V22 V29 V28 V34 V35 V32 V31 V41 V40 V37 V38 V39 V35 V42 W43

W21 W24 W23 W22 W30 W33 W32 W31 W39 W38 W37 W43 W44 W42

G14 PAL 22V10 — H21 G21 H22 G22 H23 G23

AE27 AE25 AE26 AE29 AE24 — 74LS74

D22 8254 — D30 D31 D32 GD

AF9 74LS08 AF14 AF13 AF12

AF1 74LS393 AF1 AF2 AF3 AF4 AF5 AF6 — AF1 74LS393 A43 A42 A41 A40 A39

AF17 74LS109 AG23 AG22 AG20 AF21 AF22

AF17 74LS107 AF17 AF19 AF20 AF18 AG18

AD31 P22V10 — AD41 AE42 AD40 AD39 AE41 AE40

AF9 74LS08 AF10 AF11 AF9

EOR

INPUT BUFFER ADDRESS COUNTERS MOD J

THE UNIVERSITY OF WISCONSIN
SPACE SCIENCE & ENGINEERING CENTER
MADISON, WISCONSIN

TITLE MCIDAS
METEOSTAT PDUS INGESTOR
SCHEMATIC DIAGRAM

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N.A.	D. FORD	3-24-87			E. LY	4-86
NEXT HIGHER ASSEMBLY -0538	PRODUCT ASSURANCE	DATE	PROJECT APPROVAL	DATE		
PROJECT NO 1025	SIZE D	SHEET 2 OF 5	DRAWING NO 6450-0537			

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

SHT. 1,2,4&5

4 BUS

ADØ ADØ ADØ ADØ ADØ ADØ ADØ ADØ
Ø 1 2 3 4 5 6 7

L1 74LS590 — L10 74LS590 — L19 74LS590 — L28 74LS590

N10 1420-55 4KX4 — N21 1420-55 4KX4 — R10 1420-55 4KX4 — R21 1420-55 4KX4

AD31 PAL 22V10 — AD32 PAL 22V10

T23 74LS640 — T34 74LS590

N1 8216 — R1 8216 — J37 8216 — L37 8216

N32 22V10A — R32 22V10A

BDØ BD1 BD2 BD3 BD4 BD5 BD6 BD7 (SHT. 1)

DATØ DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7 (SHT. 3 SHT. 5)

OBS (SHT. 4) ORS (SHT. 5) OWS (SHT. 2) A2 A1 AØ (SHT. 1,2&4)

OUTPUT BUFFER - DATA CONTROL MOD J

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MADISON, WISCONSIN

TITLE MCIDAS
METEOSTAT PDUS INGESTOR
SCHEMATIC DIAGRAM

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N.A.	D.FORD	3-24-87				5-24-88
NEXT HIGHER ASSEMBLY -0538	PRODUCT ASSURANCE	DATE	PROJECT APPROVAL	DATE		
PROJECT NO 1025	SIZE D	SHEET 3 OF 5	DRAWING NO 6450-1537			

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

J1 316A102

A1 8085-2AH

A37 74LS379

AD15 XTL. OSC 18.432 MHz

N32 PAL 22V10

R32 PAL 22V10

A37 74LS379

A22 2764-2

E35 74LS373

C36 8185-2

D22 8254

D17 8256

A16 MAX 232

PRS SHT. 5
SWS SHT. 5
TBC SHT. 1 & 2
CRS SHT. 5
BRC SHT. 1
LOCK SHT. 1
DPF SHT. 5
IAK SHT. 1
DBT SHT. 2
ILG SHT. 1
OBS SHT. 3
BUD SHT. 2
LBC SHT. 1
DRD J3-3
DTD J3-5
GND J3-13

BTE SHT. 2
CRI SHT. 5
BTC SHT. 2
CDI SHT. 5
EOR SHT. 2
EOF J2-30
PRI SHT. 5
RST SHT. 5
PL

μ BUS SHT. 1 & 2 & 3

RWDR A3 A2 A1 A0 μ BUS SHT. 1 & 2 SHT. 1, 2 & 3

MICROPROCESSOR SYSTEM MOD J

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MADISON, WISCONSIN

TITLE MCIDAS
METEOSTAT PDUS INGESTOR
SCHEMATIC DIAGRAM

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N.A.	D. Fogg	3-24-87				5-24-88
NEXT HIGHER ASSEMBLY 0535	PRODUCT ASSURANCE	DATE	PROJECT	DATE	APPROVAL	DATE
PROJECT NO 1025	SIZE D	SHEET 4 OF 5			DRAWING NO 6450-0537	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

+5V
K1
J1 316A102
1K
J5
J6
J7
J10
J10 K10 AS3
J11 K11 AS2
J12 K12 AS1

J1
1K
PL K5 K1 +5V

ADR7 P1-52
ADR6 P1-51
ADR5 P1-54
ADR4 P1-53
ADR3 P1-56
ADR2 P1-55
ADR1 P1-58
ADRΦ P1-57
IORC P1-21
IOWC P1-22
XACK P1-23
G1 PAL 22V10A

AD31 PAL 22V10

SHT.4 SWS
DAT 7 P1-68
DAT 6 P1-67
DAT 5 P1-70
DAT 4 P1-69
DAT 3 P1-72
DAT 2 P1-71
DAT 1 P1-74
DAT Φ P1-73

INIT P1-14
AD31 PAL 16L8
SHT.4 RST

J15 74LS240
J16 74LS240
G27 74LS224
G36 74LS224
J26 74LS374

CRI SHT. 4
CDI SHT. 4
ORS SHT. 3
DAT 7
DAT 6
DAT 5
DAT 4
DAT 3
DAT 2
DAT 1
DAT Φ
SHT. 3

SHT.4 PRI
SHT.4 PRS
G14 22V10

AD7
AD6
AD5
AD4
AD3
AD2
AD1
ADΦ
SHTS. 1,2 3&4

SHT.4 CRS

AD31 P22V10

DPF SHT. 4

2 - CARD RESET
1 - CONTROL WRITE / STATUS READ
Φ - COMMAND WRITE / DATA READ

UNIT AS3	AS2	AS1	MULTIBUS ADDRESS Φ	1	2
Φ	Φ	Φ	B4	B1	B2
Φ	Φ	1	68	69	6A
Φ	1	Φ	94	91	92
Φ	1	1	98	99	9A
1	Φ	Φ	A4	A1	A2
1	Φ	1	A8	A9	AA
1	1	Φ	B4	B1	B2
1	1	1	B8	B9	BA

MULTIBUS INTERFACE MOD J

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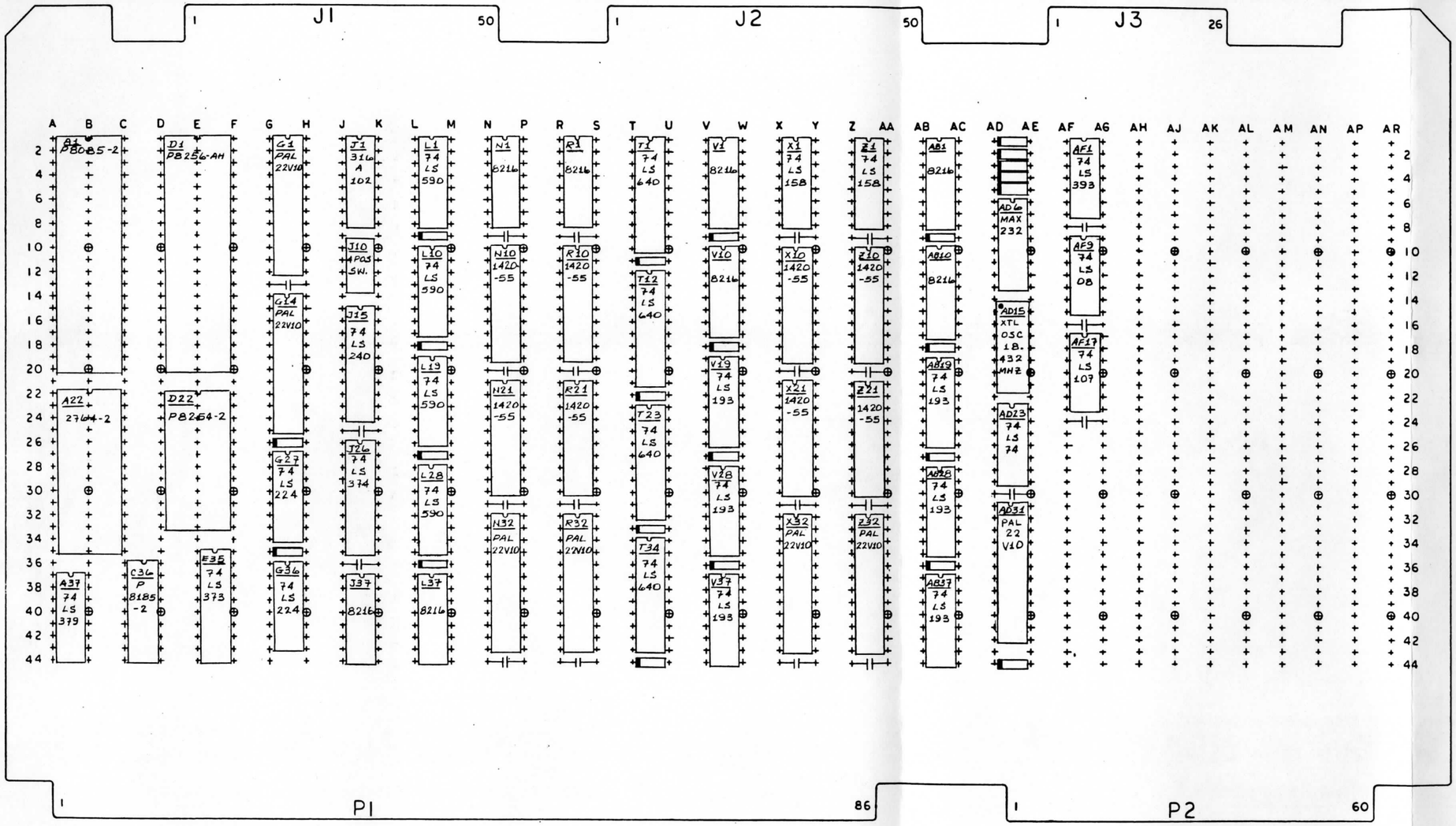
MADISON, WISCONSIN

TITLE MCIDAS
METEOSTAT PDUS INGESTOR
SCHEMATIC DIAGRAM

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N.A.	D.FOKU	3.24.87			8-24-88	
NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE	DATE	PROJECT APPROVAL	DATE		
- 05-25						
PROJECT NO 1025	SIZE D	SHEET 5 OF 5	DRAWING NO 6450-0537			

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



⊕ TENTH ROW DESIGNATION

MOD J

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MADISON, WISCONSIN

TITLE MCIDAS 2
METEOSAT PDUS INGESTOR
ASSEMBLY DRAWING

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
2:1	W.FORD	3-24-87				8-24-88
NEXT HIGHER ASSEMBLY -0537	PRODUCT ASSURANCE	DATE	PROJECT APPROVAL	DATE		
PROJECT NO 1025	SIZE D	SHEET 1 OF 1	DRAWING NO 6450-0538			

Appendix A

METEOSAT PDUS Overview

METEOSAT is a European meteorological satellite system. The satellite is in a geosynchronous orbit over North Africa, and it takes pictures in the following three spectral bands:

- Visible (0.4 - 1.1 μm)
- Infrared (10.5 - 12.5 μm)
- Water Vapor (5.7 - 7.1 μm)

The visible image contains 5000 lines with 5000 pixels per line. An infrared or water vapor image contains 2500 lines having 2500 pixels per line. Visible image resolution is 5 km if only one of the two vis sensors is used, or 2.5 km if both vis sensors are used simultaneously. Infrared and water vapor image resolution is 5 km.

The satellite generates one set of images every half hour. This set consists of:

- 2.5 km resolution visible or
- 5 km resolution infrared or
- 5 km resolution water vapor or
- 5 km resolution visible (one sensor) and infrared or
- 5 km resolution visible (one sensor) infrared and water vapor or
- 5 km resolution infrared and water vapor or
- 2.5 km resolution visible and 5 km infrared

The METEOSAT system is controlled from Darmstadt, W. Germany. The actual transmitted image set is controlled by the ground station at Darmstadt. The raw satellite image data is transmitted to Darmstadt where it is corrected for satellite drift and registration errors caused by the differing fields of view. The corrected data is retransmitted from Darmstadt to the METEOSTAT satellite which retransmits the corrected data to users. In addition to the image data that originates on the METEOSAT, GOES-E data is converted to METEOSAT format by a ground station in Lannion, France. The ground station can retransmit the data to the METEOSAT satellite for retransmission. Thus, in addition to METEOSAT-originated images, the METEOSAT satellite can relay GOES-E images as well.

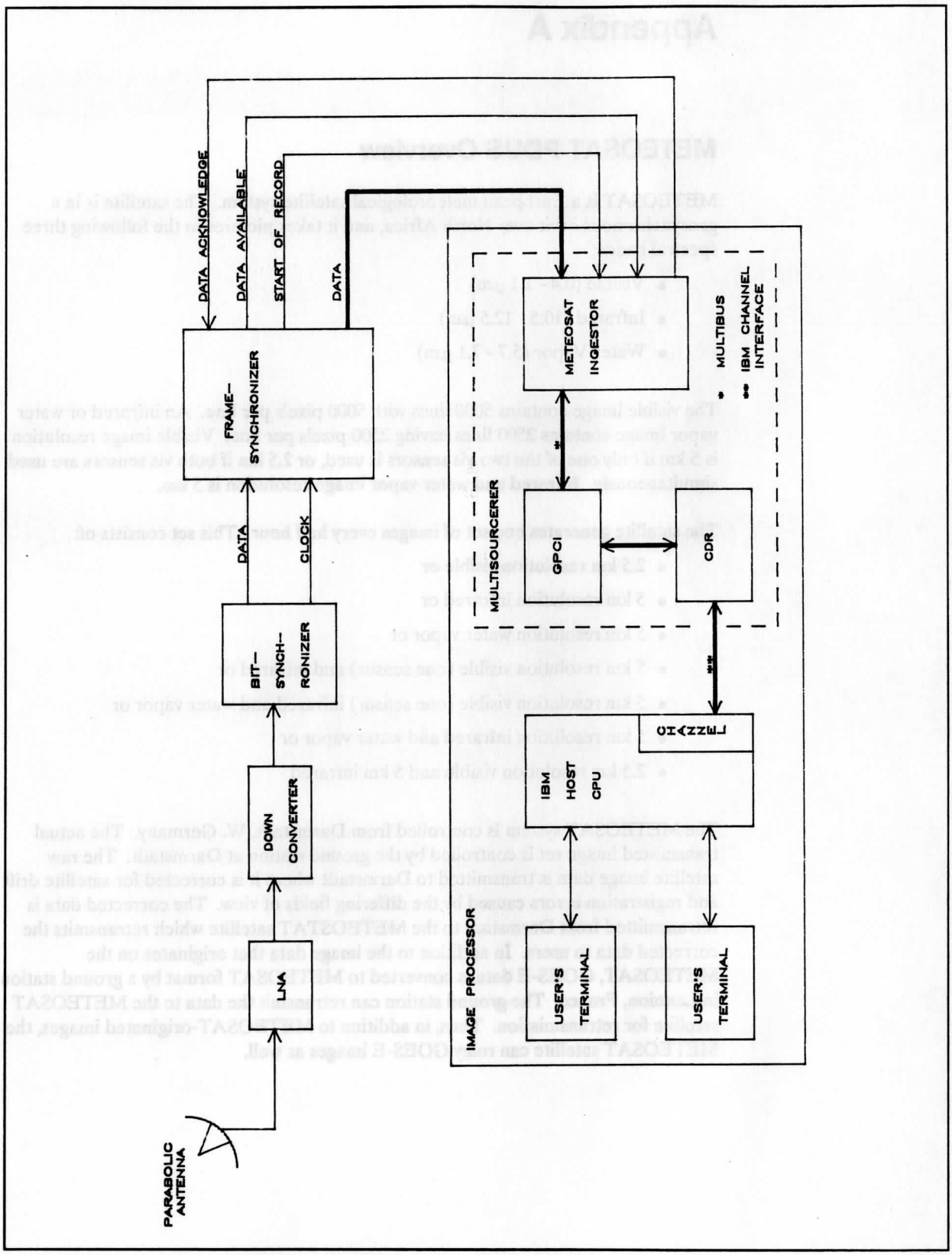


Figure 1. Primary Data User Station Block Diagram

Block Diagram

The METEOSAT retransmits the high resolution processed digital image data via an on-board S-band transceiver. METEOSAT high resolution transmissions can be received by a Primary Data User Station (PDUS). In its simplest form, a PDUS consists of:

- a Parabolic Antenna
- a Low Noise Amplifier (LNA)
- a Down Converter
- a Receiver and Demodulator
- a Bit Synchronizer
- a Frame Synchronizer
- an Image Processor

Figure 1 on the adjacent page is a block diagram of a PDUS. The Parabolic Antenna receives the S-band METEOSAT signal and sends it to the Low Noise Amplifier (LNA). The LNA provides the required amplification to drive the Down Converter. The Down Converter converts the S-band signal to a lower frequency for processing by the Receiver. The Receiver and Demodulator recover the modulation signal, which consists of a composite of data and bit-rate clock.

The Bit Synchronizer separates the Demodulator output into a bit-rate clock and a serial data stream, and sends these signals to the Frame Synchronizer. The Frame Synchronizer recognizes sync patterns, beginnings of images and scan lines, and converts the serial image data to 16-bit parallel data (Dornier type Frame Synchronizer). The Frame Synchronizer passes the data and identifier signals to the Image Processor. The Image Processor consists of the Multisourcerer (containing a PDUS METEOSAT Ingestor, the GPCI, and the CDR boards), the IBM Host, and User's Terminals.

Format	VIS	IR	WV
AV	2500 lines of VIS1 with 5000 pixels per line plus 2500 lines of VIS2 with 5000 pixels per line or 5000 lines VIS1 or VIS2 with 5000 pixels per line	None	None
AI	None	2500 lines with 2500 pixels per line	None
AW	None	None	2500 lines with 2500 pixels per line
AIV	Same as AV	Same as AI	None
AIW	None	Same as AI	None
AIVW	2500 lines VIS1 or VIS2 with 5000 pixels per line	Same as AI	Same as AW
AIVH	2500 lines VIS1 or VIS2 with 2500 pixels per line; Data reduction by taking every second pixel	Same as AI	None
BV	Same as AV except 625 lines and 2500 pixels	None	None
BI	None	625 lines with 1250 pixels per line	None
BW	None	None	625 lines with 1250 pixels per line
BIV	Same as BV	Same as BI	None
BIW	None	Same as BI	Same as BW
BIVW	Same as AIVW except 625 lines and 2500 pixels	Same as BI	Same as BW

Table 1. Modes A and B Data Format Summary

METEOSAT Data Characteristics

The PDUS METEOSAT Ingestor collects and temporarily stores entire scan lines of data. On command from the CPU, the Ingestor transmits all or part of a scan line to the IBM Host via the GPCI and CDR boards. The user interacts with the IBM Host via the User's Terminals.

METEOSAT data is retransmitted in one of the following three formats:

- Mode A - whole earth-disk as seen by METEOSAT
- Mode B - European, North African and Middle-Eastern regions as seen by METEOSAT
- Mode X - North and South American continents as seen by GOES-E

The picture sets listed on the first page of this appendix apply to Modes A and B. That is, the picture set may include data from one, two, three or four sensors. In fact, Mode B is simply a subset of Mode A. It consists of 625 lines containing 1250 pixels per line for infrared and water vapor images, or 1250 lines containing 2500 pixels per line when both vis sensors are used (2.5 km resolution). Mode B is the one-eighth portion of Mode A that covers Europe, North Africa and Middle Eastern regions. The X Format consists of 2500 lines with 2500 pixels in the visible spectrum, and 1250 lines with 1250 pixels in the infrared spectrum. Table 1 on the adjacent page summarizes the A and B formats.

The X Format is not ingested by SSEC's PDUS METEOSAT Ingestor and is not described further.

Data Format

Each Format in Table 1 is made up of message units called "subframes". In turn, each subframe is made up of smaller message units called "frames". There are four types of subframes in a format. They are:

- Heading subframes
- Image data subframes
- Annotation subframes (B Formats only)
- Conclusion subframes

A Format subframes consist of eight frames, while B Format subframes consist of four subframes. All frames contain 364 bytes each. Figure 2 on the next page shows the format construction.

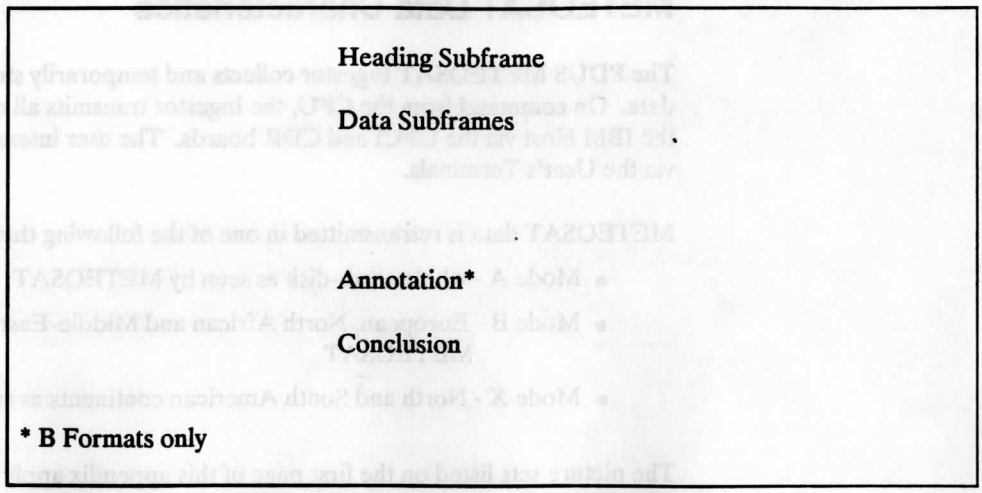


Figure 2. Format Construction

Heading Subframes

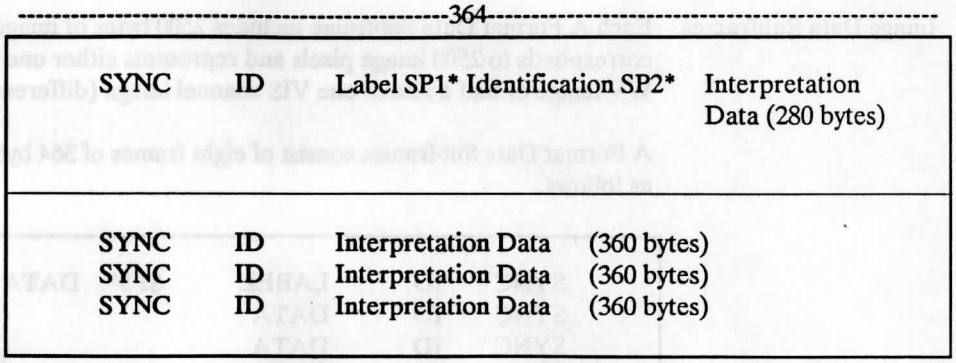
The Heading Subframe consists of eight frames for A Formats, and four frames for B Formats. The Heading Subframe is repeated 42 times for A Formats, and 84 times for B Formats. As stated above, all frames are 364 bytes in length. Refer to the A and B Format header structures below.

----------364----------

SYNC	ID	Label SP1* Identification SP2*	Interpretation Data (280 bytes)
SYNC	ID	Interpretation Data	(360 bytes)
SYNC	ID	Interpretation Data	(360 bytes)
SYNC	ID	Interpretation Data	(360 bytes)
SYNC	ID	SP4*	
SYNC	ID	SP4*	
SYNC	ID	SP4*	
SYNC	ID	SP4*	

A Format Header Structure

*SP1 = 8 spare bytes (all set to zero)
*SP2 = 16 spare bytes (all set to zero)
*SP4 = 360 spare bytes (all set to zero)



B Format Header Structure

*SP1 = 8 spare bytes (all set to zero)
*SP2 = 16 spare bytes (all set to zero)
*SP4 = 360 spare bytes (all set to zero)

Each frame begins with a three-byte synchronization code, followed by a one-byte ID word. The ID word indicates the Frame number within the subframe (i.e., 0-7 for A Formats and 0-3 for B Formats). Thus, there are 360 bytes available in each frame for data. These bytes (2880 total in the A Format or 1440 in the B Format) convey the following information:

- Label - 24 bytes
- Identification - 32 bytes
- Interpretation data - 1360 bytes
- Spares - 1464 bytes for A Formats, 0 bytes for B Formats

The Label indicates:

- number of frames in the subframe
- total number of subframes in the format
- current subframe number
- image line number (0 in the Heading Subframe)
- image number
- sensor identification
- grid information availability flag
- annotation data availability flag
- scan direction

The Identification contains the satellite indicator, the year, day, hour and minute of image acquisition. The Interpretation Data contains information on satellite orbit, geographical correction methods used, calibration coefficients and administrative messages.

Image Data Subframes

Each A Format Data Subframe includes 2500 bytes of image information. This corresponds to 2500 image pixels and represents either one complete line of an IR or WV image or half a line of one VIS channel image (different for AIVH formats).

A Format Data Subframes consist of eight frames of 364 bytes each. The structure is as follows.

SYNC	ID	LABEL	SP5*	DATA (296 BYTES)
SYNC	ID	DATA		(360 bytes)
SYNC	ID	DATA		(360 bytes)
SYNC	ID	DATA		(360 bytes)
SYNC	ID	DATA		(360 bytes)
SYNC	ID	DATA		(360 bytes)
SYNC	ID	DATA		(360 bytes)
SYNC	ID	DATA (44 bytes)		(316 bytes) GRID

A Format Data Subframes Structure

*SP5 = 40 spare bytes (all set to zero)

B Format Data Subframes consist of four frames of 364 bytes each. The structure is as follows.

SYNC	ID	LABEL	SP6*	DATA (328 BYTES)	
SYNC	ID	DATA		(360 bytes)	
SYNC	ID	DATA		(360 bytes)	
SYNC	ID	DATA		(202 bytes)	(158 bytes) GRID

----------364 bytes----------

B Format Data Subframes Structure

*SP6 = 8 spare bytes (all set to zero)

Each B Format Data Subframe includes 1250 bytes of image information. This corresponds to 1250 image pixels and represents one complete B Format line of IR or WV image or half a B Format line of one VIS channel image.

Annotation Subframes

Annotation Subframes are unique to B Formats. 30 Annotation Subframes, corresponding to 30 Image Lines, contain the satellite ID, day, month, year, hour and minute of the image. The design of Annotation Subframes is identical to the design of B Format Data Frames. In Annotation Subframes 1 and 30, all data is set to zero, resulting in white lines. The remaining 28 Annotation Subframes (=28 lines) form a matrix of 28 lines and 504 pixels per line which display the text described above. Each character is 28 pixels high and 20 pixels wide. There are four pixels between characters. Spaces are represented by 24 pixels. Therefore, the 21 characters (including spaces) use 504 pixels per line. The remaining pixels in the annotation frame are set to zero.

Conclusion Subframe

The Conclusion Subframe is a copy of the Heading Subframe. The number of Conclusion Subframes transmitted in the individual transmission format is:

- One for all A Formats and BI, BIV, BW, and BVW
- Two for BIW, BIVW and BV