INSTRUCTION MANUAL

FM SUBCARRIER DIGITIZER

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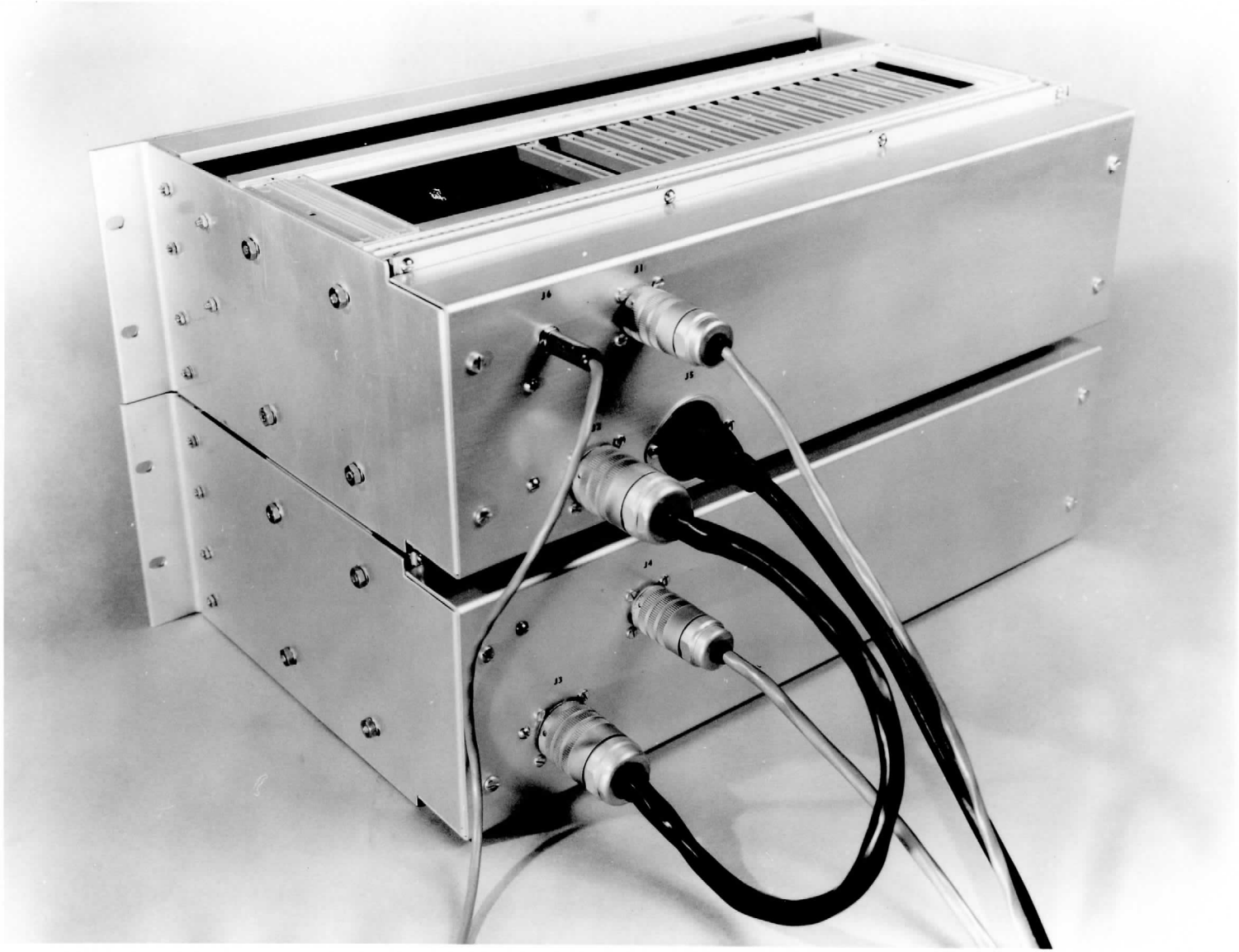
SUBCARRIER DIGITIZER
MANUAL
INHIBIT
WRITE
AUTO
MODE
WRITE
INHIBIT
ON
POWER
UNIVERSITY OF WISCONSIN INSTRUMENTATION LABORATORY MADISON, WISCONSIN

POWER SUPPLY
1001A
ADJ
ON
OFF
POWER SUPPLY
1001A
ADJ
ON
OFF



1.0 INTRODUCTION

1.1 GENERAL

This manual contains information for the installation, operation and maintenance of the Subcarrier Digitizer.

The Digitizer is designed for operation with a modified EMR Model 210 Subcarrier Discriminator. It samples and converts to digital data the frequency of the Discriminator VCO. A six-line digital output and appropriate command signals are provided for recording the data on a Precision Instrument Incremental Tape Recorder, Model RSL-150-7C. or Model PI-1157.

1.2 FUNCTIONAL DESCRIPTION

When appropriate signals are received from the Discriminator, the frequency of the Discriminator VCO is regularly sampled by a period measurement method. In each sample taken, the signal from a 100 KHz. clock is counted by an eight-bit data counter for the duration of eight complete cycles of signal. The contents of the data counter, and word designator bits, are read out in two six-bit characters at a 125 character per second rate.

The Digitizer is constructed of plug-in printed circuit cards in two separate card cages designed for mounting in 19" racks. The upper cage, Unit A, contains signal processing, timing, and control circuitry, with all normal operating controls and indicators located on the front panel. The lower cage, Unit B, contains the data counter, storage buffer, and readout logic circuitry. Each cage contains a Model 1001A regulated power supply which provides all normal operating voltages required for the circuits in the cage, except for - 105 v. DC, which is taken from the EMR equipment.

Test points are provided on a Test Point Card located in the upper cage, and a row of neon indicators which display the steady state contents of the data counter are located on a card in the lower cage. Both front

panels are hinged and may be swung open to provide easy access to all circuits and test points. Measurements may be made on any circuit by using the extender cards provided.

An output is provided which indicates whether or not a digital record is being written. This output may be recorded by a pen recorder simultaneously with the analog output of the EMR Discriminator to facilitate correlation between digital and analog records.

2.0 SPECIFICATIONS

2.1 AUXILIARY EQUIPMENT

The Digitizer is designed for operation with a EMR Model 210 Subcarrier Discriminator supplied and consisting of

Model 210A-05-26492B Discriminator (modified)

Model 210B-02-0.66-7.5%-26492B Channel Selector

and Model 210C-01-00160.0-26492B Output Filter

Specifications of the Discriminator are given in Section 2 of the Instruction Manual of the EMR Model 210 Subcarrier Discriminator.

The specifications given in the paragraphs below relate only to the Subcarrier Digitizer.

2.2 ELECTRICAL SPECIFICATIONS

2.2.1 Input Signals: Test points TP-3 (LIM) and TP-4 (VCO) of the EMR Model 210A Discriminator provide the necessary signal inputs for the operation of the Digitizer.

2.2.2 Input Frequency: Unambiguous outputs are obtained for an input frequency range of 656.25 ± 7.5% using prescribed data counter presets. Frequency deviations up to ± 10% may be measured, depending on the preset chosen.

2.2.3 Sample Accuracy: Quantization noise error is ± 1 count. Error due to slight variation from exact periodicity of the sampling period, is less than 0.5 counts for modulating frequencies up to 6.25 cps. at ± 7.5% deviation.

The total error is then less than ± 1.5 counts, which corresponds to a subcarrier frequency measurement within ± 0.91 cps. of the true frequency and an information accuracy within ± 0.93%.

2.2.4 Output Signals: The data and incremental recorder control outputs are two-level logic signals. A "logical 0" is represented by a voltage level in the range -0.2 ± 0.2 volts and a "logical 1" by -10 ± 2 volts. The 10 - 90% rise time is less than 0.5 μs.

The data is presented to the recorder 80 μs. before the STEP command, and the inter-record GAP signal follows a last step command by at least 10 ms.

The output format is given in appendix A.

2.2.5 Output Load: The maximum load on any output is the combination of 1000 pf. to signal ground, 880 ohms to -12 volts DC, and 1400 ohms to DC ground. Any combination of loads may be applied, but no single type of load should exceed the value stated.

2.2.6 Line Voltage: Power line supply voltage required is 117 volts, 60 cycle AC.

2.3 MECHANICAL SPECIFICATIONS

a. Physical Dimensions: Each section of the Digitizer is 5 3/16" high, 17 1/2" wide, excluding the brackets for mounting in a 19" rack, and 10 3/8" deep, excluding front and rear panel projections.

b. Operating Temperature: 0° to 50° C.

c. Cooling: Natural air convection.

3.0 INSTALLATION AND OPERATION

3.1 INSTALLATION

3.1.1 EQUIPMENT SUPPLIED

The complete Digitizer equipment consists of the following:

Unit A - Upper chassis

Unit B - Lower chassis

Interconnection cables - W1, W2, W3, W4

Power Cord

Instruction Manual (2 copies)

Spare Printed Circuit Cards - one each of the following:

- 4XH-M
- A35-M
- 026-L
- A26-M
- 8SA-M
- 4XG-M
- ZLD-1101
- SCD-1102
- MNO-1106
- PRS-1103 (3 cards)

An EMR Channel Selector and Output Filter described in Section 2.1 is also supplied.

3.1.2 MOUNTING

Unit A should be mounted directly above Unit B in a 19" rack.

3.1.3 COOLING

Adequate cooling should be provided to limit the ambient temperature to a maximum of 50 degrees Centigrade.

3.1.4 ELECTRICAL CONNECTIONS

3.1.4.1 Power: Connect the power cord between the power receptacle on Unit A and a 115 volt, 60 cycle, "U" grounded power outlet.

3.1.4.2 Discriminator to Digitizer: Terminate the wires of the cut end of W1 with supplied terminal lugs and connect to TB 1 of the EMR Rack Adapter as listed below.

W1 Wire	TB 1 Terminal
Black	20
Brown	19
Green	18
White	17
Red	16

Connect the female connector of W1 to J1 on Unit A.

3.1.4.3 Unit A to Unit B: Connect cable W2 between receptacles J2 on Unit A and J3 on Unit B.

3.1.4.4 Digitizer to Recorder: Connect cable W3 between J4 on Unit B and J105 of the PI Recorder.

3.1.4.5 Printed Circuit Card Connections: Plug the printed circuit cards securely into the card connectors.

The sixteen card locations in each rack are numbered (but not marked) from left to right. The proper card type for each location is listed below.

Unit A		Unit B	
Location	Card Type	Location	Card Type
1	No Card	1	EXT
2	KG-100	2	EXT
3	4XH	3	No Card
4	4XH	4	No Card
5	4XH	5	No Card
6	A35	6	4XG
7	026	7	MNO
8	N26	8	PRS
9	A26	9	4XH
10	8SA	10	4XG
11	TPC	11	N26
12	4XG	12	4XH
13	4XH	13	N26
14	4XH	14	026
15	SCD	15	N18
16	ZLD	16	8SA

3.1.5 EMR DISCRIMINATOR MODIFICATION

The modification to the EMR Discriminator and Rack Adapter consists of adding the following wires:

Inside Discriminator

TP-3 to 1P1-C

TP-4 to 1P1-E

Discriminator to Rack Adapter

J5-C to TB1-19

J5-E to TB1-17

J5-A to TB1-16

Rack Adapter

TB2-20 to TB1-18

3.2 OPERATION

3.2.1 CONTROLS, INDICATORS, AND TEST POINTS

The location, function, and description of all indicators, test points, and operating controls are given in Tables 3-1, 3-2, and accompanying Figures 3-1 and 3-2.

3.2.2 DATA COUNTER PRESET

The card PRS must be wired to preset the data counter. The relation between preset number and output is given in Appendix A. Wiring lists for any preset are given in Table 3-3 and a diagram of card PRS in Figure 3-4.

3.2.3 INITIAL OPERATION AND ADJUSTMENT

3.2.3.1 Preliminary Inspection: Insure that the proper circuit card type is in each card location, and that each card is securely plugged into its connector. The card type designated for each location is given in Section 3.1.4.4.

3.2.3.2 Power Supply Adjustment Procedure: Energize the equipment by placing the switches on the front of each power supply and the POWER switch on the front panel to the ON position. The POWER indicator lamps above those switches should glow.

Figure 3-1. Location of Front Panel Controls and Indicators. (Ref. Table 3-1.)

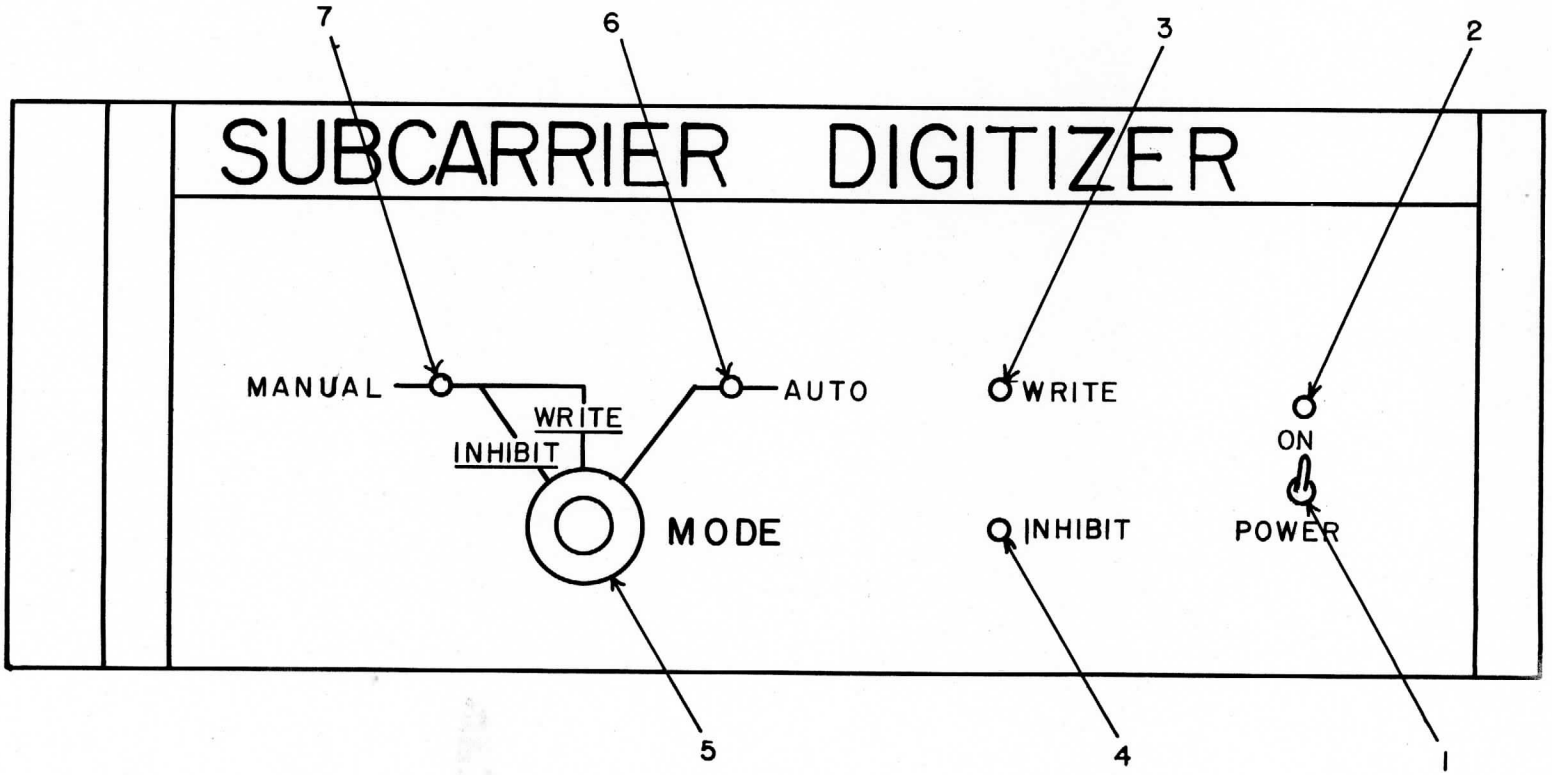


Table 3-1. Function of front panel controls and indicators (Ref. Fig. 3-1)

Ref. No.	Name	Nomenclature	Type	Function
1	POWER switch	S-1	Toggle Switch	Applies primary power to ± 12 V. power supplies
2	POWER ON indicator	I-5	Incandescent Lamp	Indicates ±12 V. power supplies are on.
3	WRITE indicator (Clear)	I-1	Neon Lamp	Indicates system is writing into incremental recorder.
4	INHIBIT indicator (Red)	I-2	Neon Lamp	Indicates system is not writing into incremental recorder.
5	MODE switch	S-2	3-pos. rotary switch	Selects mode of system operation.
6	AUTO indicator (Amber)	I-4	Neon Lamp	Indicates system is in automatic mode of operation. Writing allowed or inhibited automatically.
7	MANUAL indicator (Red)	I-3	Neon Lamp	Indicates system is in manual mode of operation. Writing is allowed or inhibited depending on position of S-2.

Figure 3-2. Location of Interior Controls, Test Points, and Indicators. (Ref. Table 3-2.)

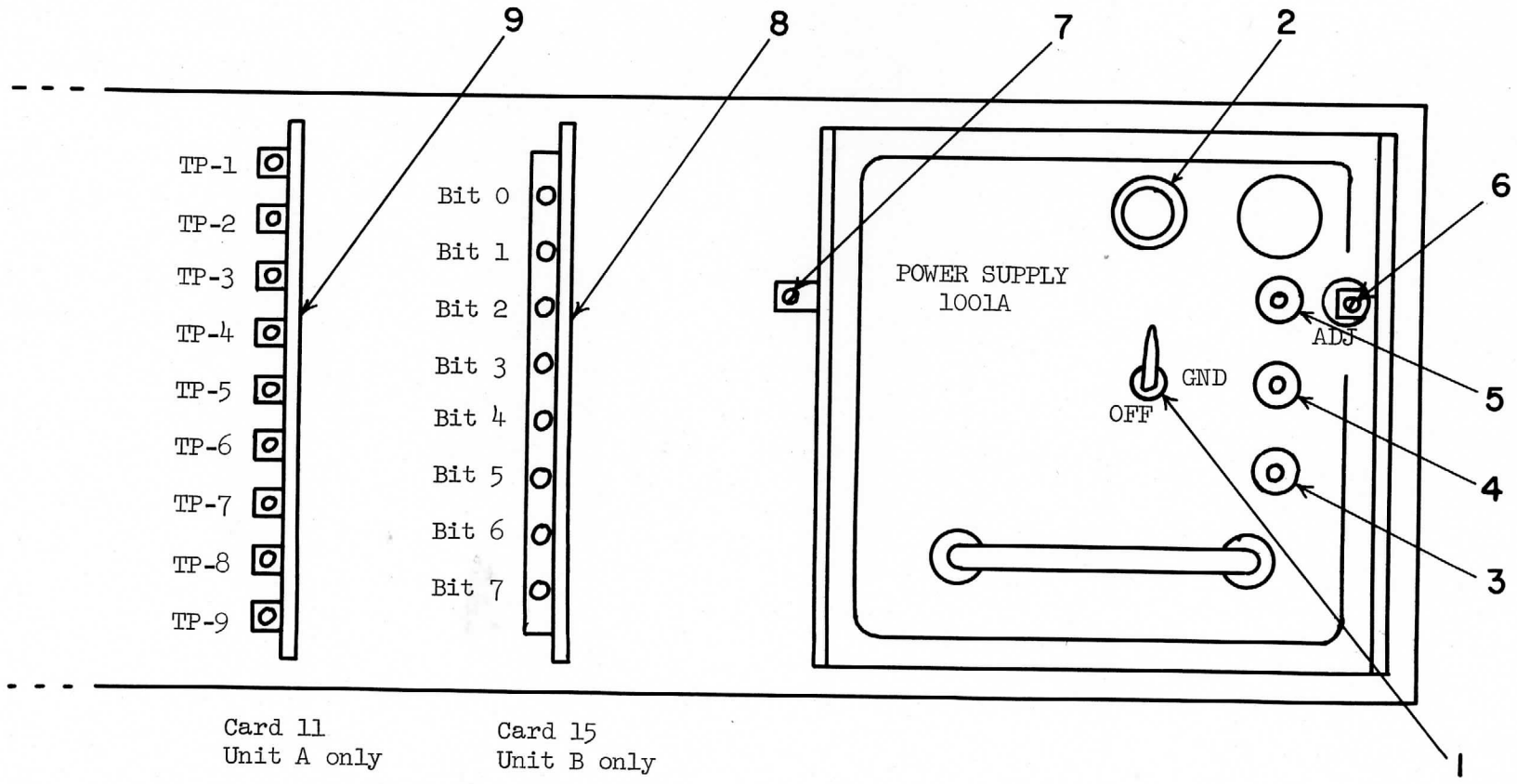


Table 3-2. Function of interior controls, test points, and indicators. (Ref. Fig. 3-2)

Ref. No.	Name	Nomenclature	Type	Function
1	POWER switch	None	Toggle switch	Applies primary power to supply.
2	POWER ON indicator	None	Neon Lamp	Indicates primary power circuit closed.
3	-	None	Black Test Point	Used to monitor -12V. supply output.
4	GND	None	White Test Point	Used as ground reference for testing.
5	+	None	Red Test Point	Used to monitor +12V. supply output.
6	MIN ADJ	R6	Potentiometer	Adjusts output of -12V. supply.
7	PLUS ADJ	R6	Potentiometer	Adjusts output of +12V. supply.
8	None	8NI	8 Neon Indicators Location B-15	Displays steady state contents of data counter. (Located in Unit B)
9	None	TPC	Test Point Card Location A-11	Provides maintenance test points.

Table 3-3. Location of Preset Card Wires

Preset Number N_p	Card Pins to be Wired													
	B	C	D	E	F	H	J	K	R	S	T	U	W	X
146	X		X		X		X		X			X		X
148	X		X			X	X		X	X				X
150	X		X			X	X		X			X		X
152			X	X	X		X		X	X				X
154			X	X	X		X		X			X		X
156			X	X		X	X		X	X				X
158			X	X		X	X		X			X		X
160	X		X		X		X			X	X		X	
162	X		X		X		X				X	X	X	
164	X		X			X	X			X	X		X	
166	X		X			X	X				X	X	X	
168			X	X	X		X			X	X		X	
170			X	X	X		X				X	X	X	
172			X	X		X	X			X	X		X	
174			X	X		X	X				X	X	X	
176	X		X		X		X			X	X			X
178	X		X		X		X				X	X		X
180	X		X			X	X			X	X			X
182	X		X			X	X				X	X		X
184			X	X	X		X			X	X			X
186			X	X	X		X				X	X		X
188			X	X		X	X			X	X			X
190			X	X		X	X				X	X		X
192	X		X		X			X	X	X			X	
194	X		X		X			X	X			X	X	
196	X		X			X		X	X	X			X	
198	X		X			X		X	X			X	X	
200			X	X	X			X	X	X			X	
202			X	X	X			X	X			X	X	
204			X	X		X		X	X	X			X	
206			X	X		X		X	X			X	X	
208	X		X		X			X	X	X				X
210	X		X		X			X	X			X		X
212	X		X			X		X	X	X				X
214	X		X			X		X	X			X		X
216			X	X	X			X	X	X				X
218			X	X	X			X	X			X		X

Figure 3-3. Card PRS Shown Wired For Preset Number (N_p) = 180.

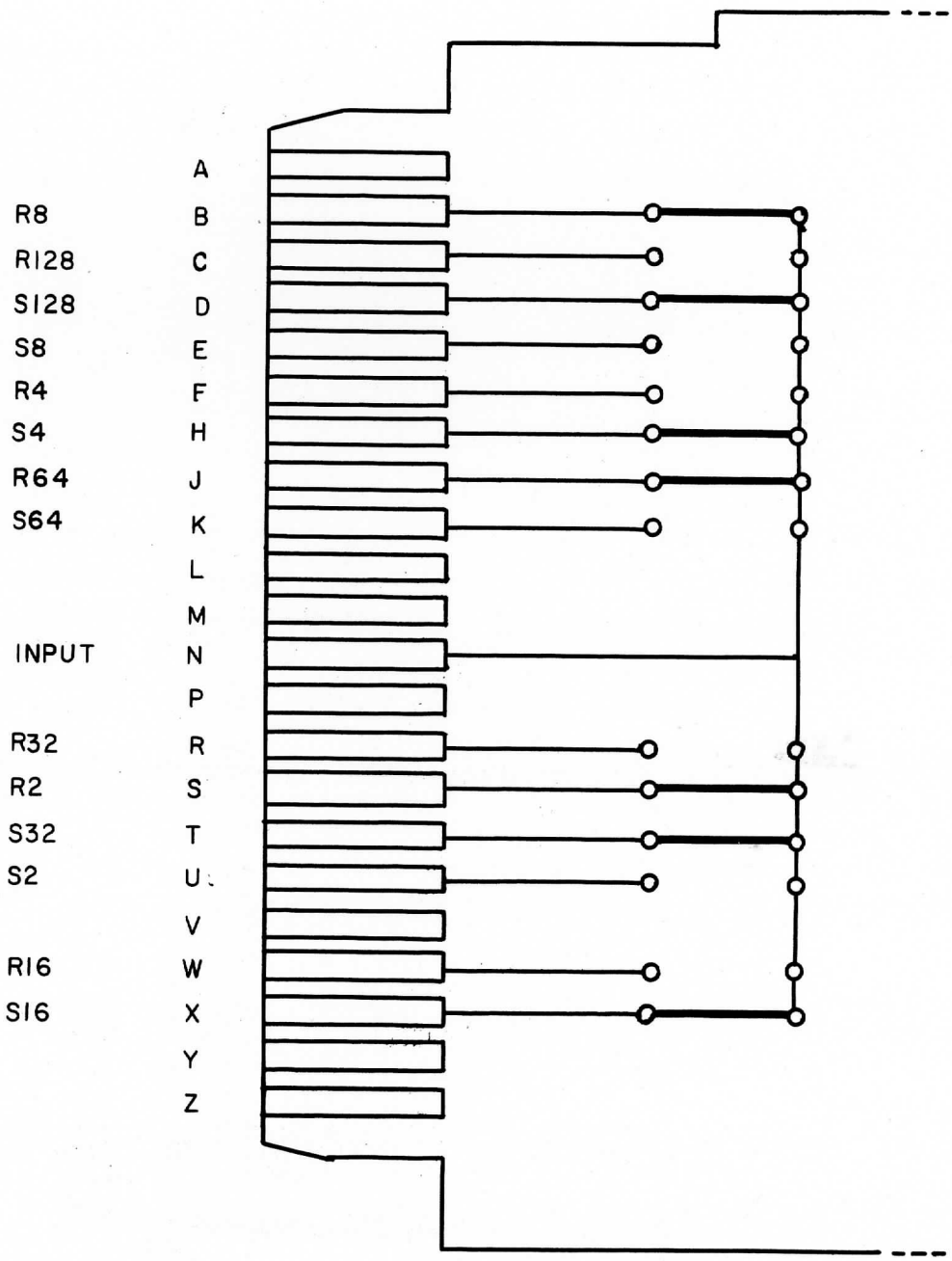
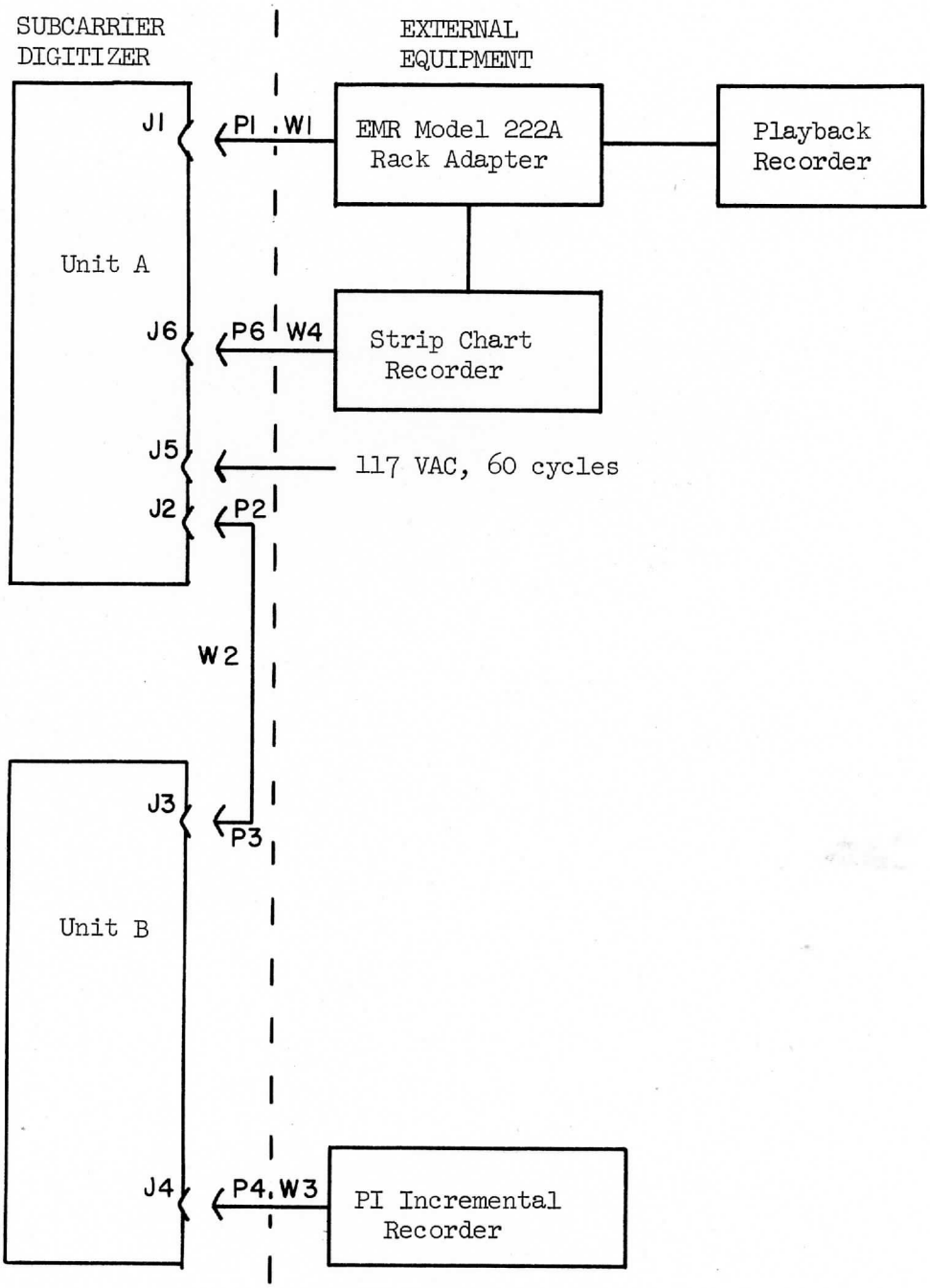


Figure 3-5. System

Interconnection Diagram



Measure the power supply output voltages from the test points provided on the front panel of each supply and adjust each to (±) 12.0 volts with the potentiometers R6. These locations are shown in Figure 3-2 by designators 6 and 7.

3.2.3.3 System Checkout:

1. Determine the data counter preset number N_p, and calculate the output numbers as in the chart below:

Input Frequency (cycles/sec)	N_o Calculation	Output Number for N_p = 180
705	$401-N_p$	221
656	$316-N_p$	136
607	$217-N_p$	37

2. Connect an audio oscillator output to the input of the EMR Discriminator, adjust the oscillator frequency to 656 ± 1 cps. and amplitude to at least 60 millivolts as indicated on the SUBCARRIER AMPLITUDE meter of the EMR Discriminator power supply.

3. Place the MODE switch of the digitizer in the WRITE position. The MANUAL and WRITE indicators only should glow.

Observe the neon indicators on the card in Unit B of the Digitizer (Location B-15). Add the numbers printed on the card next to lighted indicators. The sum should agree closely (within 1 or 2) with the output number calculated for a 656 cycle input in paragraph 1 of this section.

4. In a similar manner, check the output numbers obtained for input frequencies of 607 and 705 cps.

5. With a signal input as described above, between 607 and 705 cps, place the MODE switch in the AUTO position. Now only the AUTO and WRITE indicators should be lighted. No change should be noted in the output number neon indicators when the switch is made.

6. Change the audio oscillator frequency to a point well above or below the frequency at which the EMR Discriminator LOCK LOSS indication occurs. The WRITE indicator on the Digitizer should turn off and the INHIBIT indicator should glow.

7. Ready the Incremental Tape Recorder for operation and place the Digitizer MODE switch in the WRITE position. The recorder should step regularly at 125 steps per second. Stepping may be stopped by returning the MODE switch to the INGIBIT position. Each time the Digitizer switches from WRITE to INHIBIT mode, the incremental recorder should record an inter-record gap, regardless of whether the mode switch is performed automatically or manually.

8. If the Digitizer fails to operate as described above, refer to Section 5 for appropriate corrective maintenance.

3.2.4 NORMAL OPERATION

a. Adjust speed of playback tape recorder to the appropriate speed. The center frequency of the subcarrier signal should be 656 cps.

b. Adjust output amplitude of the playback recorder to a level between 60 mv. and 10 v. r.m.s. (See EMR Subcarrier Discriminator Instruction Manual for complete specifications regarding signal input.)

c. Energize the Digitizer and place the MODE switch in the AUTO position.

d. Load the incremental recorder.

e. Start the playback recorder. It should be noted that the WRITE indicator lamp glows only when the EMR Discriminator maintains phase lock with the signal input from the playback recorder. When phase lock is lost and the Digitizer switches to the INHIBIT mode, the incremental recorder will write an interecord gap.

4.0 THEORY OF OPERATION

4.1 SYSTEM OPERATION (Refer to Figure 4-1)

Signals from the EMR Discriminator VCO and limiter are processed by the Signal Detector card (SCD). The Signal Detector enables the Timer only when phase lock exists between the discriminator limiter and VCO signals (WRITE mode). If phase lock is lost, due to excessive noise or loss of subcarrier signal at the input to the EMR Discriminator, the Signal Detector will inhibit operation of the Timer and initiate generation of an inter-record GAP command (INHIBIT mode). If the MODE switch is placed in one of the MANUAL positions, the Signal Detector is rendered inoperative and the mode of system operation is determined by the MODE switch position.

System timing is derived from the 100 KHz crystal controlled clock (Card KG-100-A2).

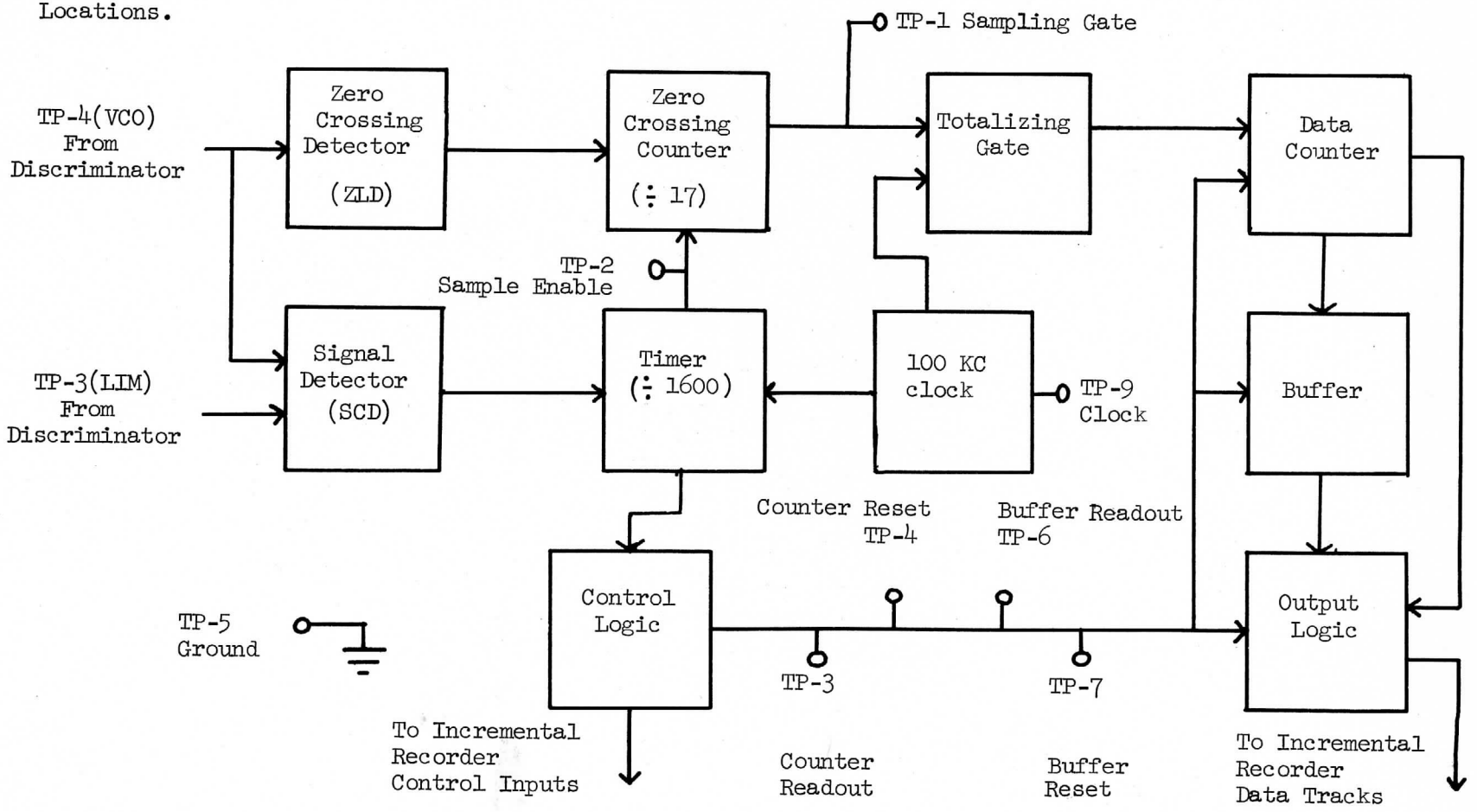
Timing signals to sequence the operation of the system circuitry and the Incremental Recorder are generated by the Timer and associated Control Logic. The Timer is a 12-bit binary counter which resets every 1600 counts to establish a system operation cycle of 16 ms. Timing signals for the sequencing of the operations performed during the 16 ms. cycle are generated by the Control Logic from certain combinations of logical states in the Timer flip-flops.

The Zero Crossing Detector (Card ZLD - A16) generates a 10 μs. pulse at each zero crossing of the signal from the EMR Discriminator VCO.

At the beginning of the 16 ms. cycle of the timer (Reset) the Zero Crossing Counter is enabled. The Zero Crossing Counter opens the Totalizing Gate (A35-5-A6) when the next output pulse from the Zero Crossing Detector occurs (Figure 4-2). The Totalizing Gate is closed upon counting

Figure 4-1. Subcarrier Digitizer Block Diagram.

NOTE:
See Figure 3-3
For Test Point
Locations.



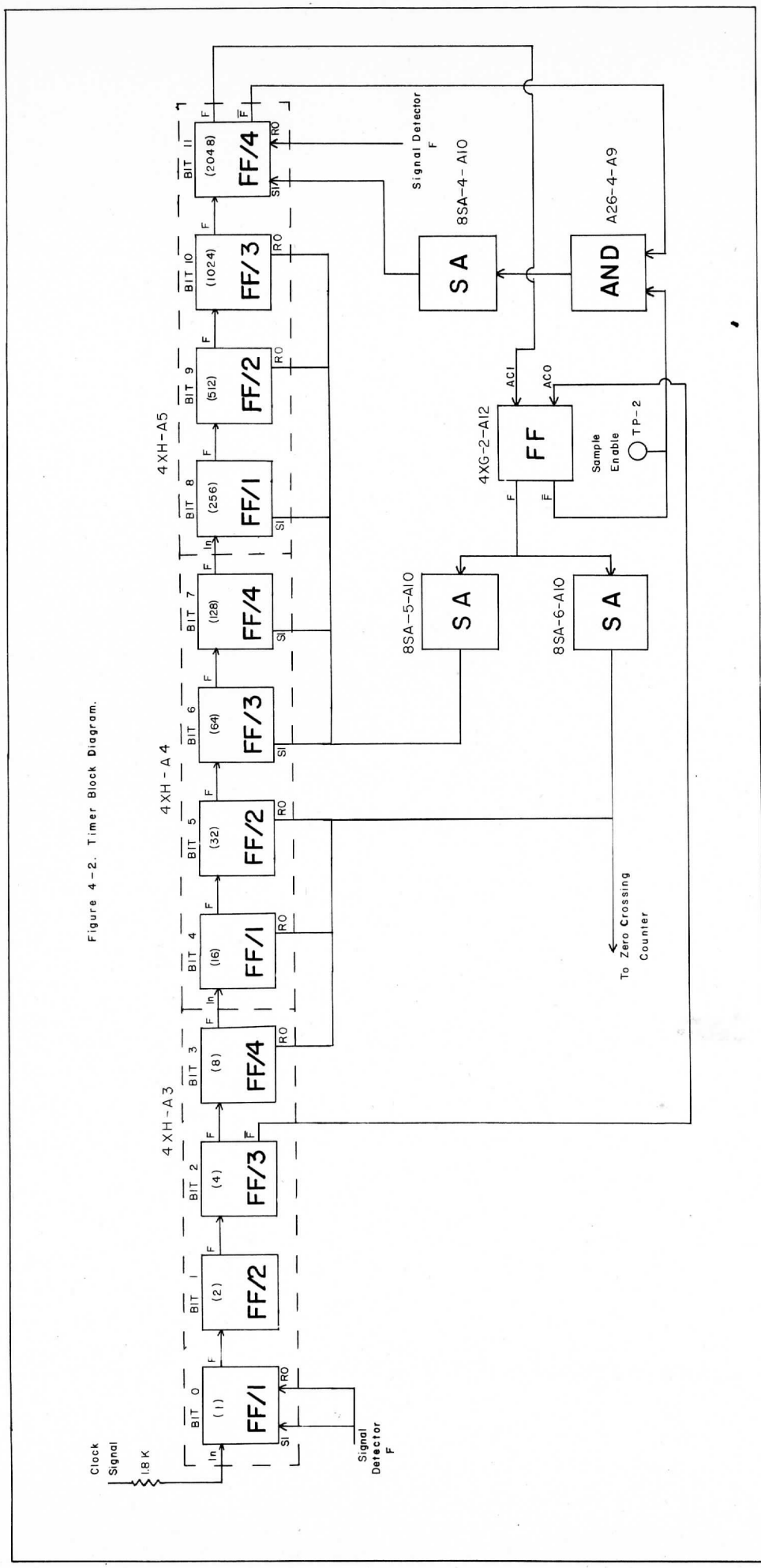


Figure 4-2. Timer Block Diagram.

the seventeenth zero crossing pulse after the Zero Crossing Counter has been enabled. The Totalizing Gate will have then been open for eight complete cycles of VCO signal input. When the seventeen zero crossing pulses have been counted, the Zero Crossing Counter resets until it is again enabled by the Timer.

The Data Counter is an eight bit binary counter. It is preset to a state determined by the wiring of the preset card (Card PRS - B8) 180 μs. before the Zero Crossing Counter is enabled. The Data Counter counts clock pulses for the interval that the Totalizing Gate is open and its contents are read out to the Buffer and Output Logic circuits 140 μs. before the next preset occurs. The Totalizing Gate is always closed before Data Counter readout occurs, provided that the input signal frequency to the system is not less than 400 cps. This frequency is far lower than any subcarrier frequency expected and represents a frequency deviation much larger than that allowed for an unambiguous data output.

The eight bits of data are read out in groups of four bits every 8 ms., to the incremental tape recorder. When the Counter Readout signal occurs, the data of the four most signigicant bits are presented to the recorder through the Output Logic circuits and the data of the four least significant bits are transferred to the Buffer. The Buffer consists of four J-K flip-flops with input AND gates (Card 4XG, B11). The sequence of buffer readout and reset is similar to and follows the counter sequence by 8.00 ms.

The Output Logic gates the counter and buffer outputs with eight NOR gates (Cards N26, B12-B13) using gate signals from the Control Logic, and channels these outputs with six OR gates (Card O-26, B15) to the Squaring Amplifiers (Card 8SA, B16). The Squaring Amplifier outputs are applied to the data track inputs of the incremental recorder.

4.2 DETAILED THEORY

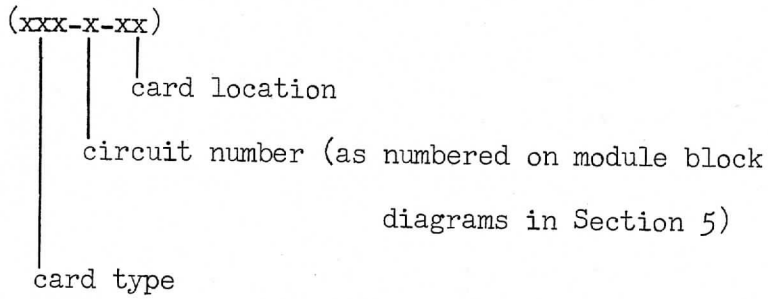
4.2.1 GENERAL

Throughout the Digitizer system, circuit output levels of -10 ± 2 v. correspond to a logical "one" and output levels of -0.2 ± 0.2 v. correspond to a logical "zero".

In the discussion to follow, counter stages and their outputs are referred to by numbers from 0 to N, where N + 1 is the total number of stages in the counter. The 0 stage is the stage containing the least significant bit and suceeding stages are numbered in order to N, which contains the most significant bit.

The number contained in any counter is here always defined as the binary number represented by the logical levels of the F outputs of the counter. In the discussion, the decimal equivalent of those numbers is always given. See Appendix B for example of converting a counter state to a decimal number.

Wyle Laboratories Germanium Logic Modules are described here in terms of logical function only. Individual circuits are designated by a code in the form



Example: (8SA-6-A10) refers to Squaring Amplifier 6 on the card in location A10.

A description of the operation of the logic circuits used in this system is also given in Appendix B.

4.2.2 SIGNAL DETECTOR (Figures 4-2.1, 4-2.1a, and Dwg. 101-02A)

The signal from the Limiter of the EMR Discriminator is applied to the emitter follower stage (Q201), which presents a high input impedance to the Limiter signal. The network between the emitter of Q201 and diode D201 sums the Limiter signal (a square wave) and the VCO signal, which is differentiated by the small input capacitor C203 and the resistance of the network.

The positive pulses of the differentiated VCO signal will forward-bias D201 and trigger the 1.5 ms. multivibrator (Q202, Q203), unless the negative half-cycle of the Limiter signal is present at the same time.

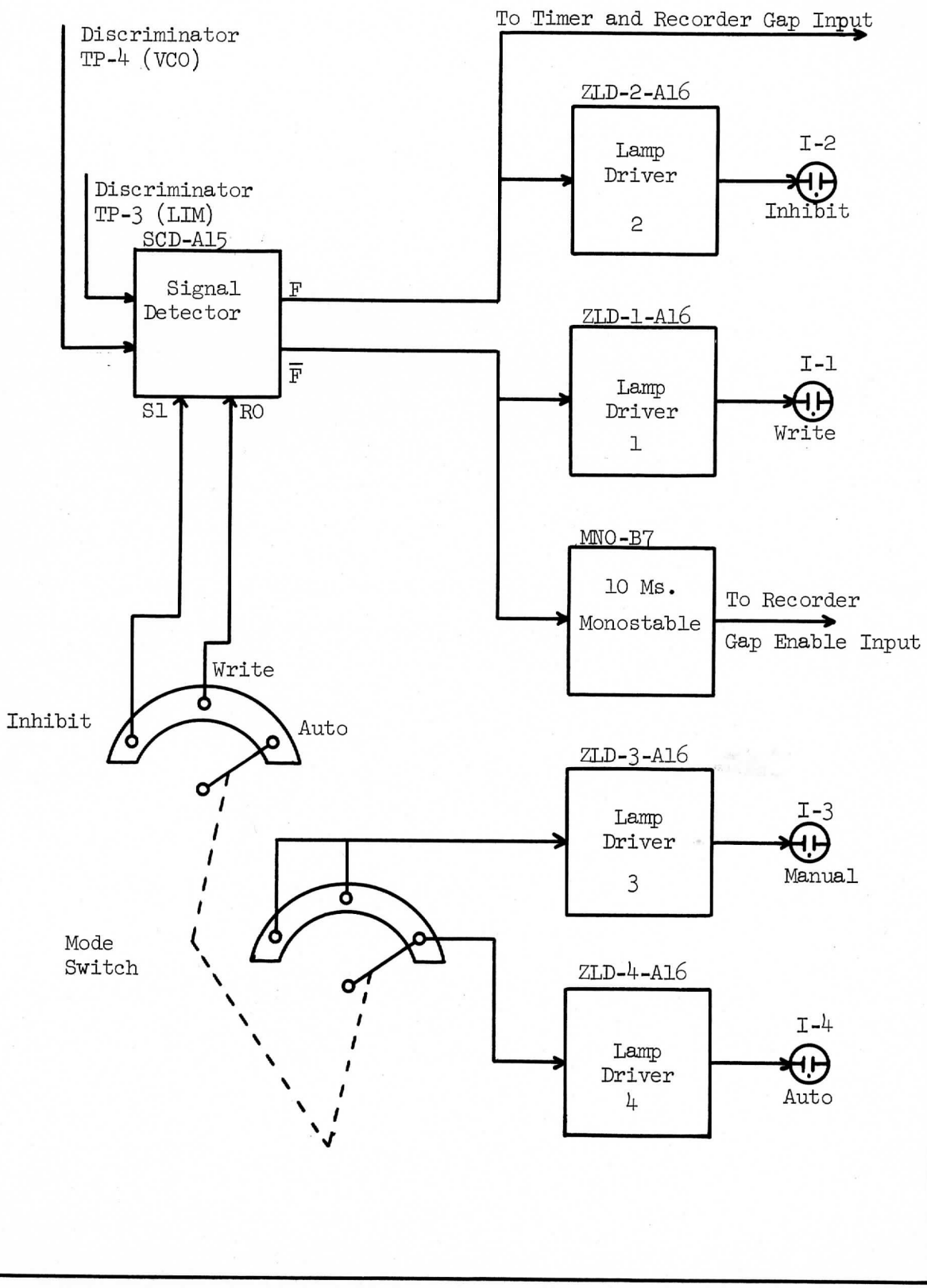
The signal conditions necessary to trigger the monostable are 1) loss of phase lock between the Limiter and VCO in the EMR Discriminator, or 2) there is no signal output from the Limiter. The first condition results from excessive frequency deviation or noise in the (subcarrier) input signal to the EMR Discriminator and the second results from a loss of input signal.

Signals from the monostable are detected and integrated by the network consisting of D202, R209, and C205. If a lock loss or signal loss persists, capacitor C205 will charge to a voltage sufficient to turn on the Schmitt trigger circuit (Q204, Q205). The Schmitt trigger will remain on until phase lock is again restored.

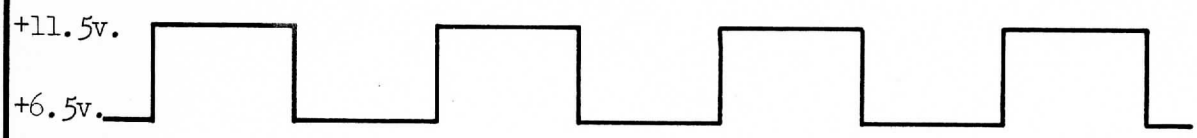
The output of the Schmitt trigger is amplified and placed at proper logic level voltages by the final two stages (Q206, Q207).

The output of the Signal Detector sets the mode of system operation to WRITE or INHIBIT. In the WRITE mode (normal signal present and Schmitt trigger off), the F output is at a logical zero level and the $\bar{F}$ output is at a logical one level. These output levels are reversed when the Schmitt trigger is turned on due to loss of phase lock, and the system operation is inhibited (INHIBIT mode).

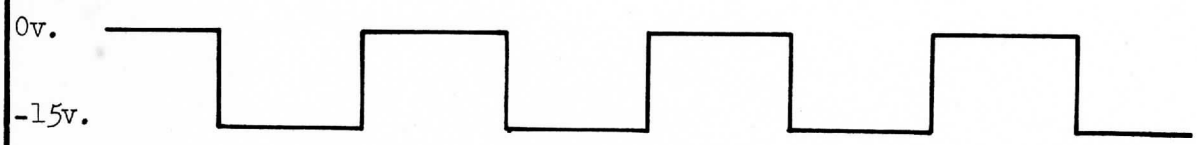
Figure 4-2.1. Signal Detector Block Diagram.



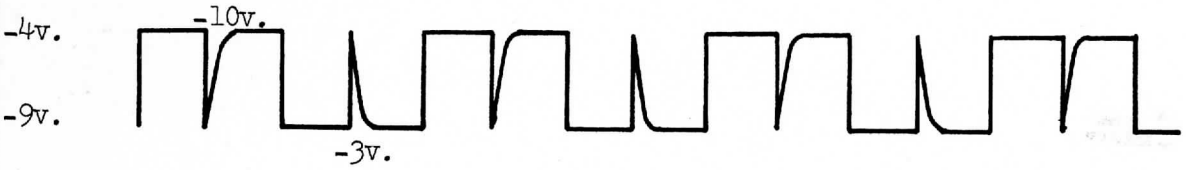
1. Limiter signal to loss of lock circuit:



2. VCO signal to loss of lock circuit:



3. Coincidence of 1 and differentiated 2:
(normal operation)



4. Coincidence of 1 and differentiated 2:
(loss of lock operation)

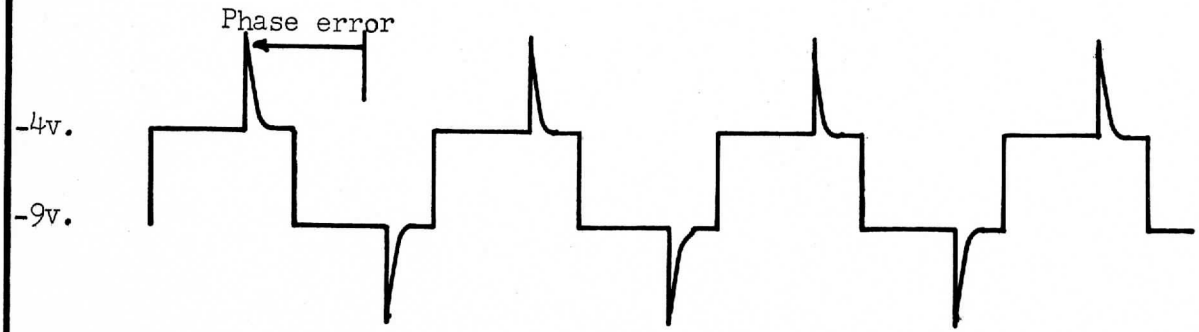


Figure 4-2.1a

VCO Waveforms

The state of the Signal Detector is indicated on the front panel by lamps I-1 (WRITE) and I-2 (INHIBIT). These lamps are controlled by Lamp Drivers 1 and 2 respectively, which are located on card ZLD-A16.

Lamp Drivers 1 and 2 and lamps I-3 and I-4 indicate whether the mode is selected manually (MANUAL) or automatically (AUTO) as shown in Figure 4-2.1.

The incremental recorder requires two input signals, GAP and GAP ENABLE, to record a inter-record gap on the tape. If one of those inputs has been at a logical 1 level for at least 10 ms., the transition of the other input from logical 0 to logical 1 will initiate the gap recording sequence. The Signal Detector F output presents the first logical 1 to the GAP input when the Digitizer switches to the INHIBIT mode. At the same time, the Signal Detector F output triggers the monostable MNO-B7. After 10 ms., the monostable output applies the 0 to 1 transition to the recorder GAP ENABLE input.

4.2.3 CLOCK

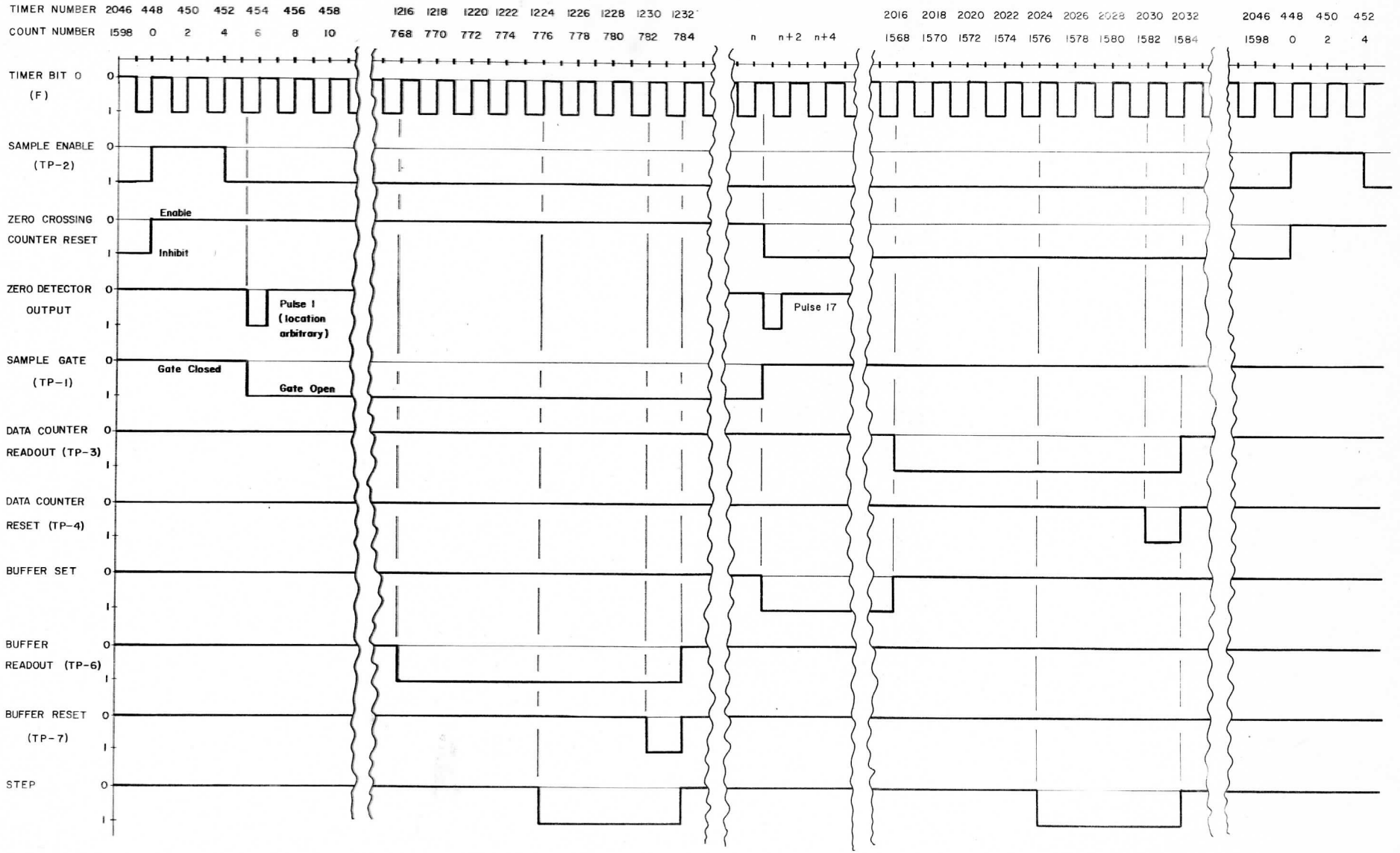
The system clock is a 100 KHz. crystal controlled oscillator (KG-100-1-A2) with a frequency stability of approximately 1 part in 10^5 under normal operating conditions and 1 part in 10^4 over the temperature range 0 to 50° C. The output is a square wave alternating between normal system logic levels.

4.2.4 TIMER

A block diagram of the Timer circuits is given in Figure 4-2. Also refer to the system Logic Sequence Chart, Figure 4-3.

The Timer contains a 12-bit counter driven by the Clock. Outputs from this counter are used in the Control Logic, by which most system timing

Figure 4-7 System Logic Sequence Diagram



signals are generated. Counter outputs are designated by the binary bit place and the side of the flip-flop from which it is taken, for example, Bit 0 F represents the F output of the first stage of the counter.

In the WRITE mode (Signal Detector F output at logical 0), there is a logical 0 at the Bit 0 DC Set and Reset inputs and the counter is allowed to operate.

When the counter number reaches 2048, Bit 11 F switches from logical 1 to logical 0. This signal sets flip-flop 4XG-2-A12 to a logical 1 state. The logical 1 output of the flip-flop is applied to appropriate DC Set or DC Reset inputs of the Counter. The combination of inputs selected resets the counter number to 448, so that 1600 clock pulses are required to bring the counter to the next reset operation.

Forty μs. (four counts) after the reset logical 1 occurs, Bit 2 $\bar{F}$ switches from logical 1 to logical 0 and resets flip-flop 4XG-2-A12, ending the reset operation. At the same time, the $\bar{F}$ output of 4XG-2-A12 and the $\bar{F}$ output of Bit 11 are ANDed (A26-4-A9) to produce a logical 1 which restores the F output of Bit 11 to a logical 1.

Squaring amplifiers shown in Figure 4-2 are used where necessary to meet loading requirements.

When an INHIBIT signal is received (Signal Detector F at logical 1), the Timer counter is stopped by applying a logical 1 to the DC Set and Reset inputs of Bit 0. Also, a logical 1 is applied to the DC Reset input of Bit 11, which sets the Bit 11 F output to a logical 0, initiating a reset signal.

Counter operation resumes with the return of a WRITE signal and the reset operation is ended as described above.

4.2.5 CONTROL LOGIC

The sequence of operation of the Control Logic circuits is given below with reference to the Control Logic Block Diagram (Figure 4-4) and the System Logic Sequence Diagram (Figure 4-3). Numbers in parenthesis indicate the decimal equivalent of the number contained in the Timer counter. The action of the Timer counter in reaching that number initiates the operation described.

(1216) The inputs 10 F, 7 F, 6 F, 8 $\overline{F}$, 9 $\overline{F}$ arrive at logical 1, switching the AND gate (A26-3-A9) output to logical 1. This AND output is inverted by the inverting amplifier (N26-3-A8) to set flip-flop 4XG-4-A12 to the 1 state. This initiates the Buffer Readout signal and applies a logical 0 to NOR gate N26-1-A8.

(1224) Input 3 $\overline{F}$ switches to a logical 0 and sets the NOR gate to a logical 1. Either NOR gate in the Control Logic at logical 1 produces the Step command via OR gate 026-1-A7 and Squaring Amplifier 8SA-8-B16.

(1230) The inputs 1 $\overline{F}$ and 2 $\overline{F}$ switch to a logical 0 to produce a logical 1 at the output of the NOR gate (N26-4-A8). The combination of logical 1's from the NOR gates (N26-4-A8, N26-1-A8) applied to the AND gate (A26-1-A9) results in a logical 1 output. That output is the Buffer Reset signal which is applied to the Buffer via Squaring Amplifier (8SA-2-A10).

(1232) Input 4 $\overline{F}$ switches to a logical 0. This 1) resets the flip-flop, ending the Buffer Readout pulse, and 2) returns the NOR (N26-1-A8) output to logical 0, ending the Step command. With the NOR output at logical 0, the AND gate (A26-1-A9) output also goes to zero to end the Buffer Reset pulse.

(2016) The combination of AND gates A35-1-A6, A35-4-A6 and A26-5-A9 perform the same logic operation as a single 6-input AND gate. Flip-flop

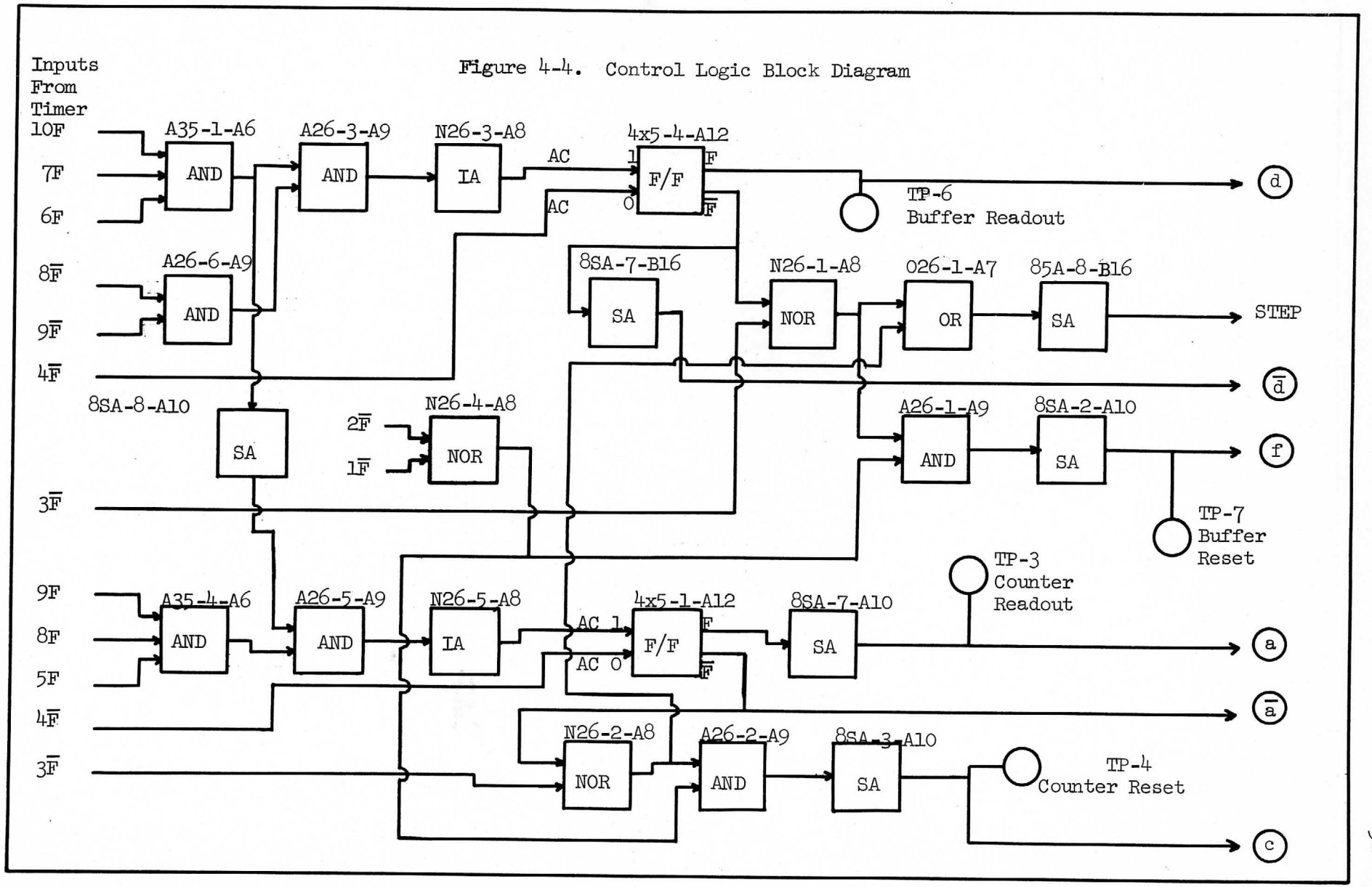


Figure 4-4. Control Logic Block Diagram

4XG-1-A12 is therefore set when inputs 10 F, 7 F, 6 F, 9 F, 8 F and 5 F all reach the logical 1 state. From this point, the arrangement and sequence of operation of the circuits generating the Data Counter Readout and Reset commands is exactly similar to that of the circuits generating commands to operate the Buffer. The sequence of operation here follows the sequence described above by exactly 800 counts (8 ms.), hence the operations which occur at (1224), (1230), and (1232) are repeated in the Data Counter control circuitry at (2024), (2030), and (2032) respectively.

4.2.6 ZERO CROSSING DETECTOR (ZLD-A16, Dwg. 101-01A)

The input emitter follower (Q101) presents a high impedance input for the signal taken from the EMR Discriminator VCO. The emitter follower output is "squared" by amplifier (Q102) and differentiated by the networks C101, R106 and C102, R107 to give alternating positive and negative pulse outputs. The 10 μs. multivibrator is triggered on the negative pulses through D101 and on the positive pulses through D102. A negative pulse output from the monostable is then obtained with each zero crossing of the input signal from the VCO. This output is used to trigger the Zero Crossing Counter.

4.2.7 ZERO CROSSING COUNTER

Refer to the Zero Crossing Counter Block Diagram (Figure 4-5) and the System Logic Sequence Diagram (Figure 4-3).

After a sample is completed (Pulse #17 has occurred), the Zero Crossing Counter (ZCC) is in the following state:

1) Flip-flop 4XG-3-A12 is set and a reset logical 1 is applied to appropriate inputs of Bits 0 through 4 to reset the ZCC number to 15. A logical 0 is also applied to one input of the AND gate (A35-2-A6) to block input pulses from the Zero Crossing Detector.

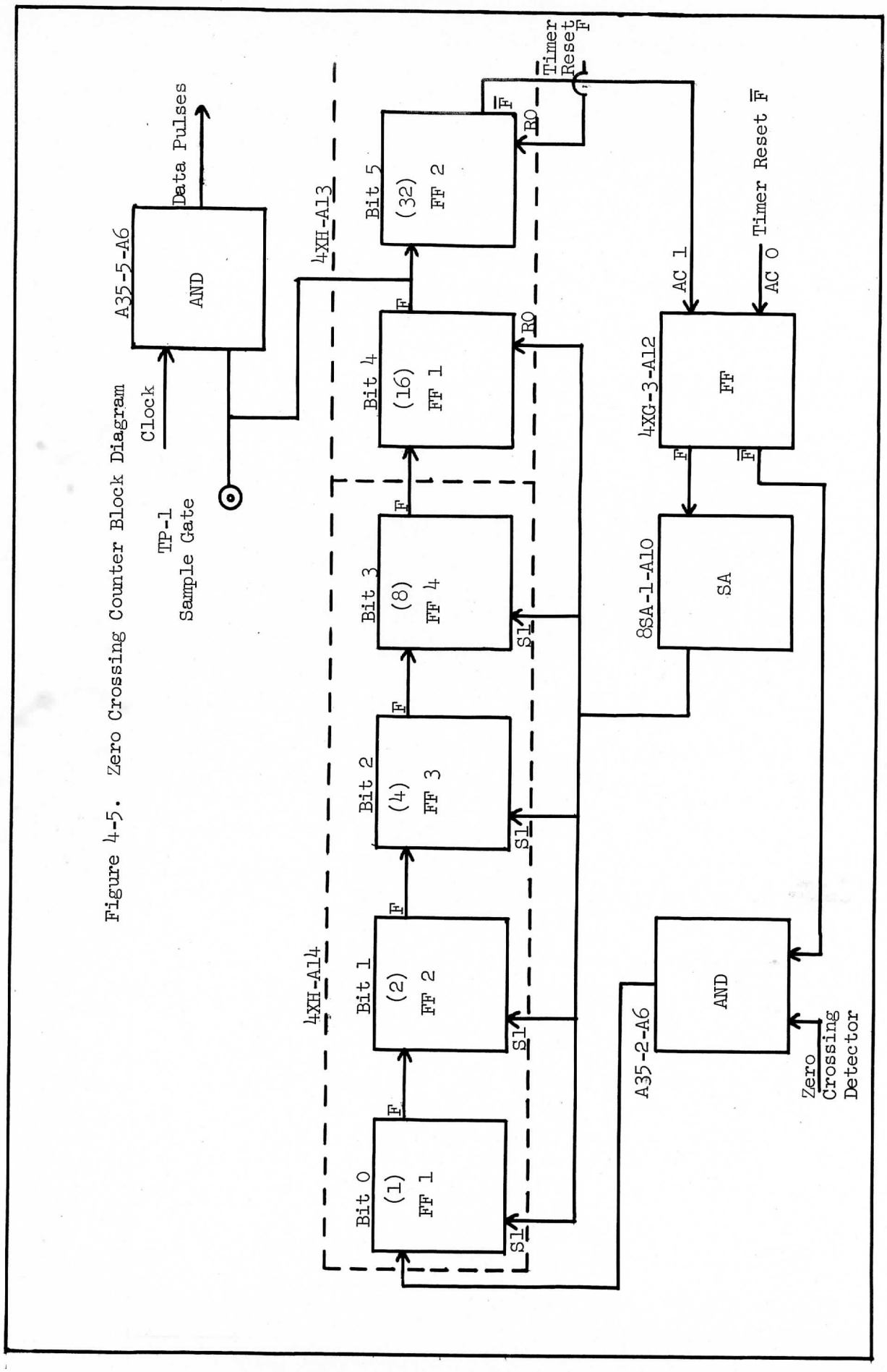


Figure 4-5. Zero Crossing Counter Block Diagram

2) Bit 5 $\bar{F}$ output is at a logical 0.

When the Timer reset pulse is applied to the flip-flop (4XG-3-A12) AC 0 input, the flip-flop resets and returns the ZCC reset signal to logical 0. Also, a logical 1 is now applied to the AND gate (A35-2-A6) to enable the ZCC to count pulses from the Zero Crossing Detector. The Timer reset pulse also sets Bit 5 $\bar{F}$ output to a logical 1 level.

With the ZCC enabled, the next output pulse from the Zero Crossing Detector (Pulse #1) advances the ZCC number to 16, switching the Bit 4 F output to a logical 1. The Data Counter is allowed to count clock pulses applied to AND gate (A35-5-A6) as long as the ZCC Bit 4 F output remains at logical 1, so the sample is begun with the arrival of Pulse #1.

The ZCC continues counting normally until Pulse #17 occurs. This pulse advances the counter number to 32, at which Bit 4 F and Bit 5 $\bar{F}$ output move to the logical 0 state.

When Bit 4 F returns to logical 0, the clock input to Data Counter is stopped, so that Pulse #17 ends the sampling interval.

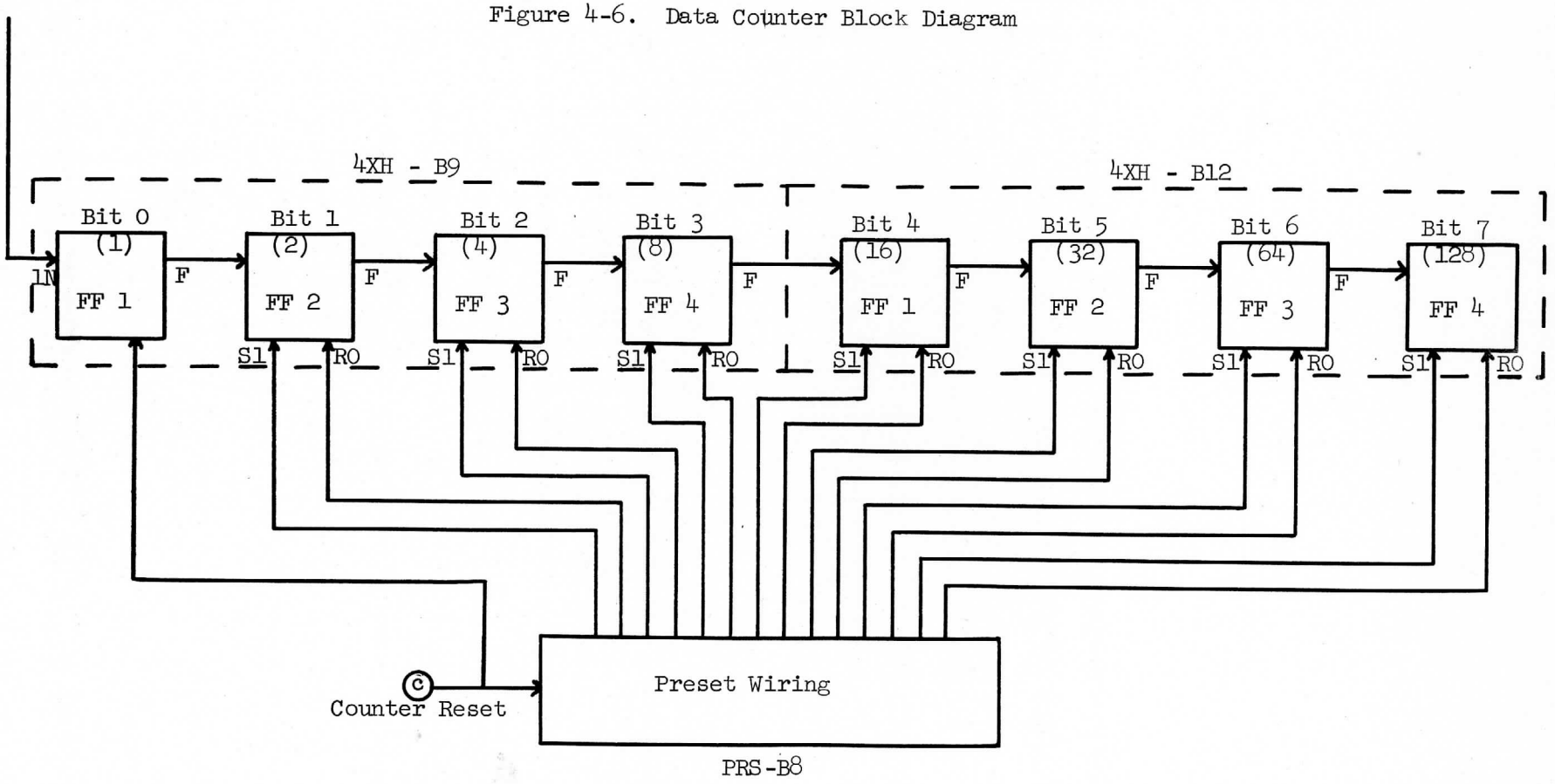
The action of Bit 5 $\bar{F}$ moving to a logical 0, resets flip-flop 4XG-3-A12 to a logical 1, to again reset the ZCC. The ZCC is now in the state first described and is again ready for another sequence of operation.

4.2.8 DATA COUNTER (Figure 4-6)

The Data Counter is an 8-bit counter consisting of the two 4-bit modules 4XH-B9 and 4XH-B12. The Preset Card wiring determines the number to which the counter is reset, depending on the choice of counter reset inputs connected to the Counter Reset lead.

The Data Counter counts clock pulses during the interval that the Sample Gate input from the Zero Crossing Counter is at a logical 1, and stops counting when the Sample Gate input is at logical 0.

Figure 4-6. Data Counter Block Diagram



In normal operation, the Counter Reset pulse will occur only when the Zero Crossing Counter is stopped.

4.2.9 BUFFER (Figure 4-7)

The contents of the four least significant bits are read into the four flip-flops (4XG-B11) of the Buffer when the Counter Readout pulse occurs. The leading edge of the Counter Readout pulse (complemented) applied to the AC 0 input of flip-flop (4XG-2-B6) switches the F output of that flip-flop from a logical 1 to a logical 0.

If the AC1 input of a Buffer flip-flop is at a logical 1 when the Counter Readout pulse occurs, that flip-flop will switch to the Set state (F output at 1, F output at 0). If the AC1 input is at a logical 0 when the Counter Readout Pulse occurs, the flip-flop will remain in the Reset state as established by a previous Buffer Reset pulse. The Buffer Reset is applied to the DC Reset input of the Buffer module.

Flip-flop (4XG-2-B6) F output is returned to a logical 1 state when the Sample Gate switches to the logical 0 state at the end of a sample.

4.2.10 OUTPUT LOGIC (Figure 4-8)

The Buffer outputs are complemented by their respective NOR gates when the Buffer Readout complement signal goes to a logical 0 (during Buffer readout interval). The NOR outputs are then presented to the recorder data tracks 4, 8, A, and B via their respective OR gates and squaring amplifiers as shown in Figure 4-8.

At the same time, the Buffer Readout signal at logical 1 (not complemented) is applied to the OR gates leading to data tracks 1 and 2, so that a 1 will always be recorded on those with each Buffer readout.

(See Appendix B for description of the operations performed by various logic elements.)

Figure 4-7. Buffer Block Diagram

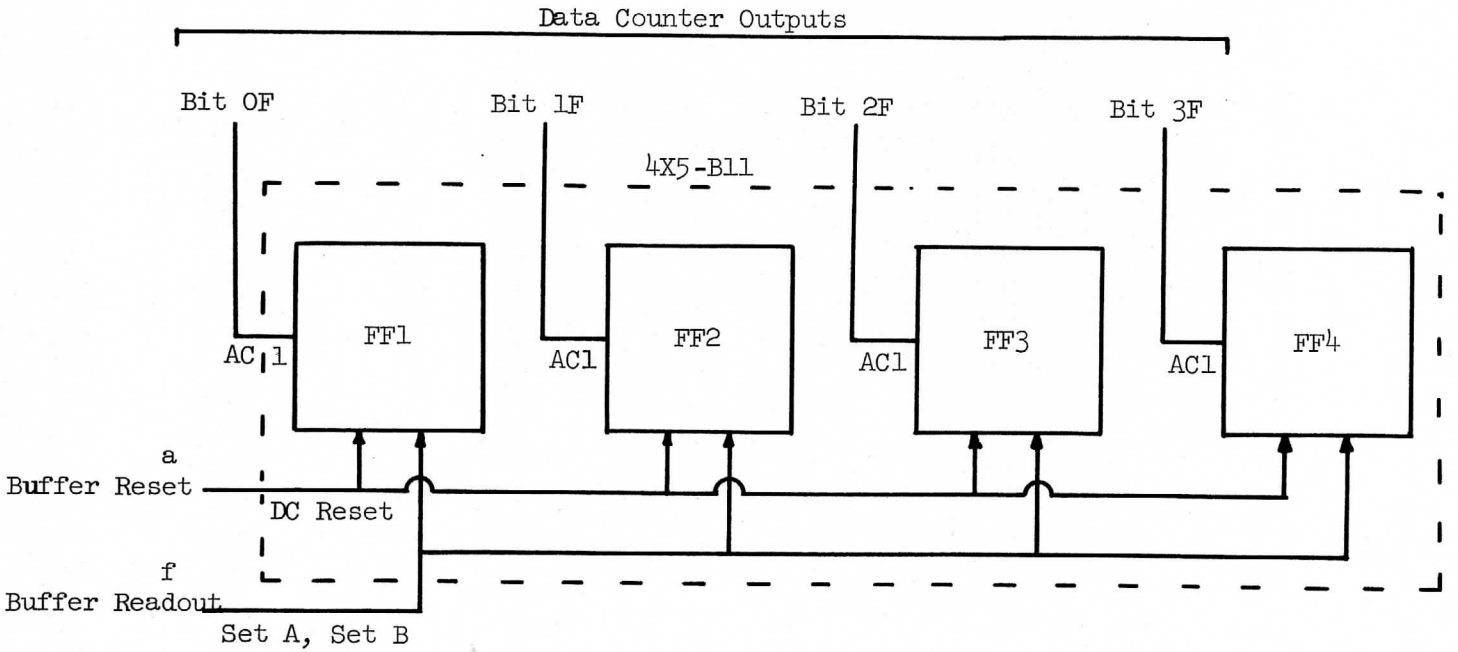
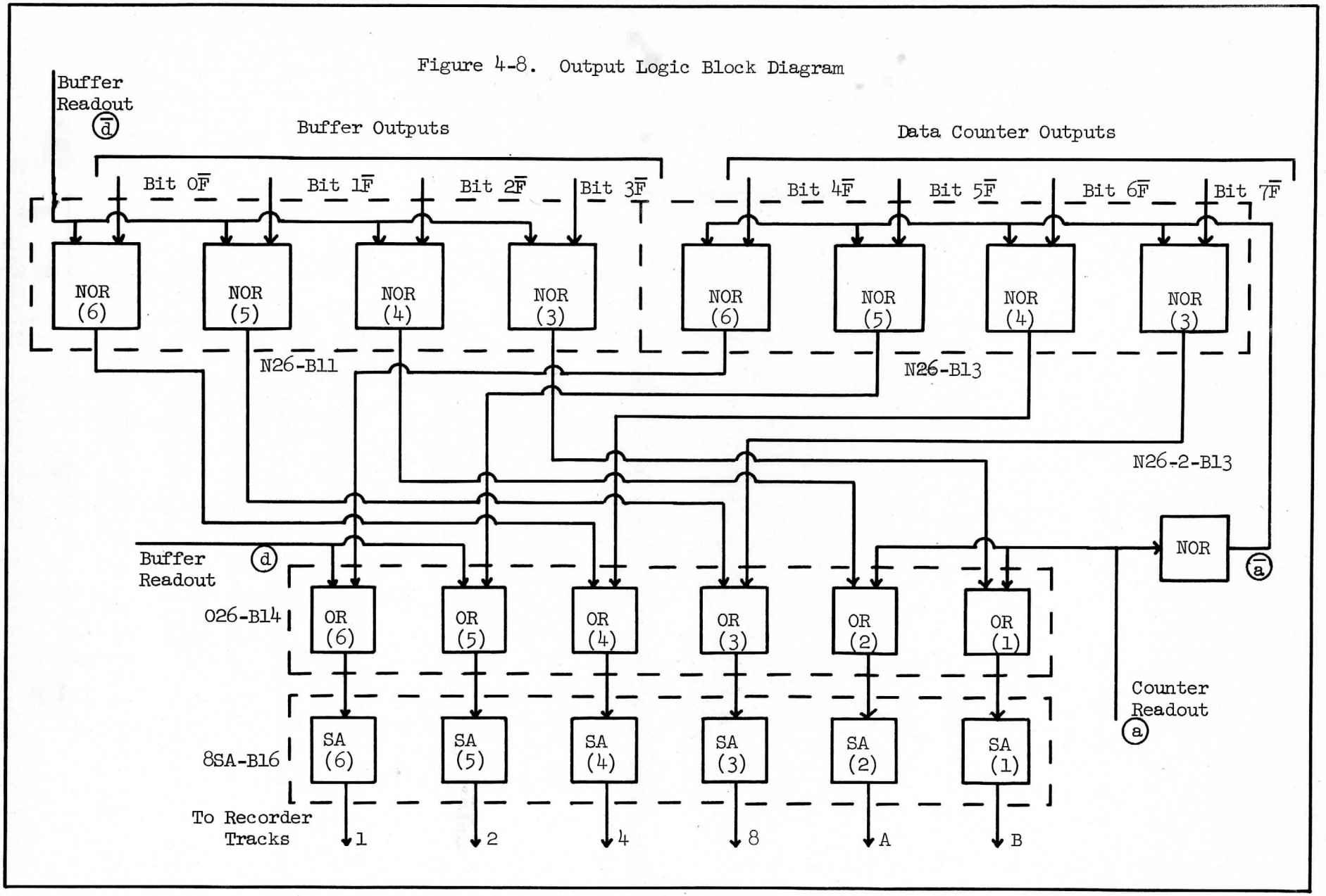


Figure 4-8. Output Logic Block Diagram



The four most significant Data Counter bits are read out in a similar manner with the Counter Readout signal, with which a logical 1 is always presented to recorder data tracks A and B.

A Step command follows 80 μs. after either a Counter Readout or a Buffer Readout pulse occurs.

5.0 MAINTENANCE

5.1 If the Digitizer fails to operate as described in Section 3.2, the corrective maintenance procedure outlined below should be followed.

5.1.1 VISUAL INSPECTION

Check for loose cards, cards in wrong locations, burned or broken components and wires on cards and front panel, etc.

Check operation of indicator lamps.

5.1.2 VOLTAGE CHECK

If trouble is not found by visual inspection, measure the voltage outputs of the two power supplies (See Section 3.2.3 b.). If any power supply output is not in the range of 11.75 to 12.25 volts, adjust to 12.0 volts and check for normal system operation.

5.1.3 SIGNAL TRACING

The trouble may usually be quickly localized by observing the operating deficiencies, front panel neon indicators, Data Counter output neon indicators, and the signals on the Test Point Card, all with reference to the System Block Diagram (Figure 4-1) and System Logic Sequence Diagram (Figure 4-3).

Detailed signal tracing may be performed by referring to the subsystem block diagrams of Section 4 and the circuit drawings and wiring lists contained in this section. The Extender Cards, normally stored in locations B1 and B2, allow easy access to any point in the system circuitry.

5.1.4 DETECTION OF FAULTY SIGNALS

If a circuit does not respond normally to an input signal, check the voltage levels and rise times of all inputs to the Wyle circuit modules.

All logical 1 levels should be -10 ± 2 v. and all logical 0 levels should be -0.25 ± 0.25 v.

The 10 - 90% rise times of signal inputs to flip-flops and counters should not be less than 0.5 μs.

If inputs are not as specified, the trouble may be in the circuitry providing those inputs, rather than in the circuit which does not respond.

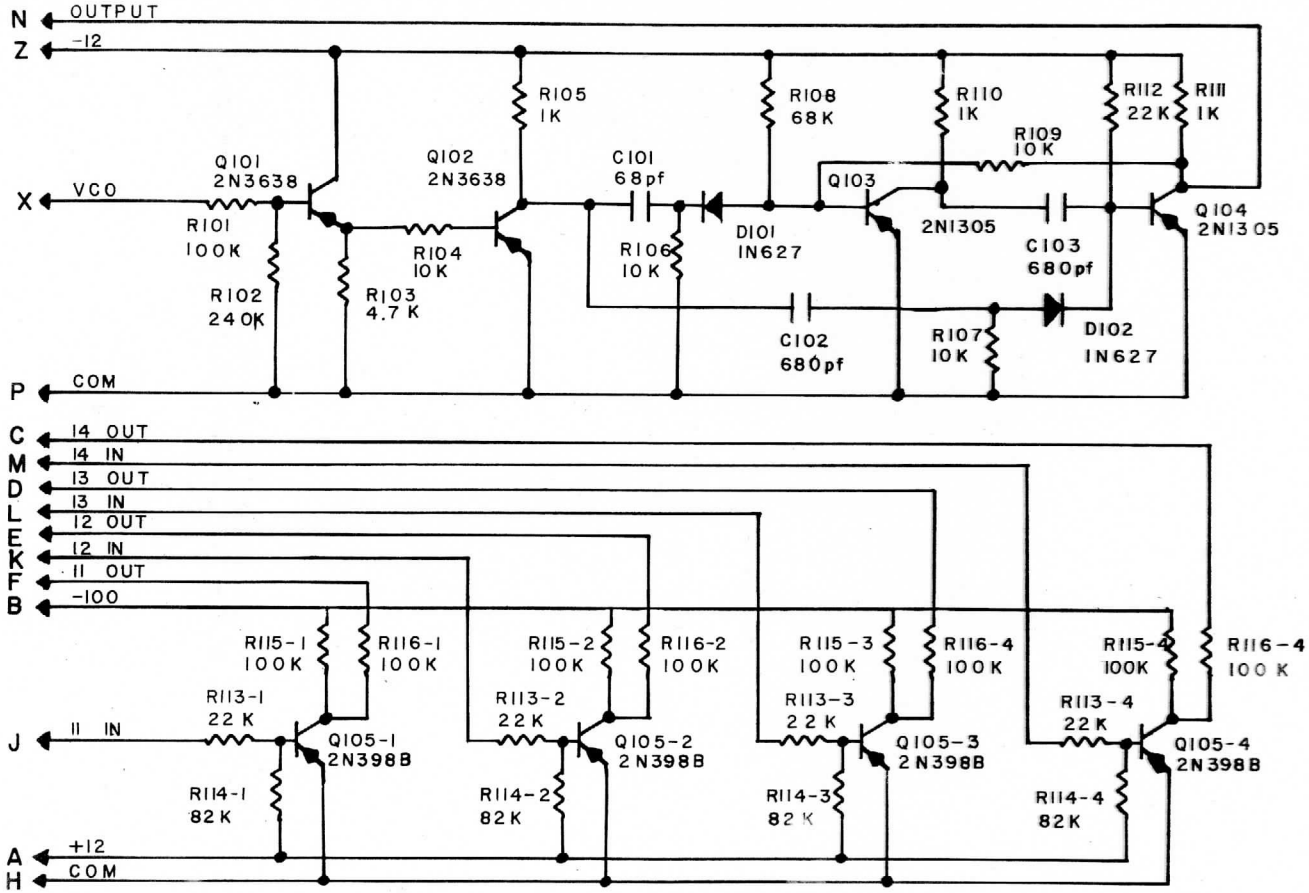
5.1.5 CIRCUIT REPAIR

Wyle circuit modules which prove defective in workmanship or materials before January 1, 1976 should be returned to

Wyle Laboratories Products Division
133 Center Street
El Segundo, California 90246
Phone (213) ORegon 8-4251
TWX 910-348-6283

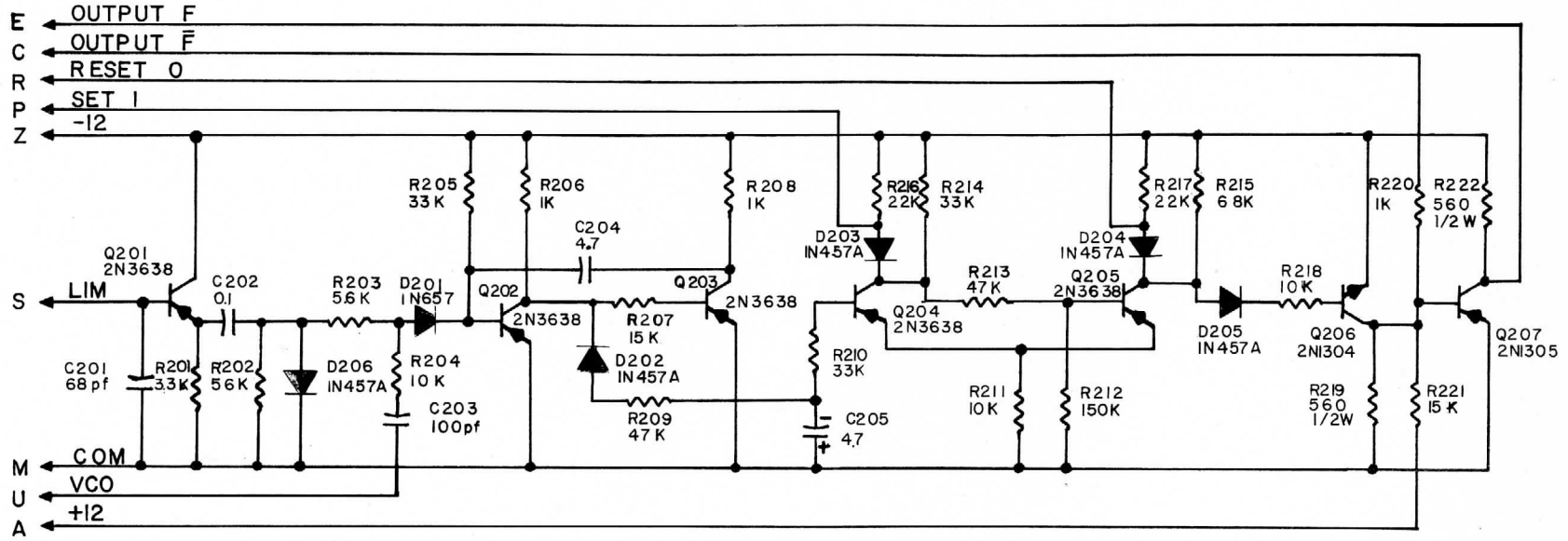
The manufacturer's warranty provides for replacement and repair of modules which prove defective, if not operated over published rating or subjected to other misuse. Transportation costs of these modules, to and from the user will be paid by Wyle Laboratories.

Other circuit modules in the system including power supply may be repaired by the user.



Capacitors in μf		UNLESS OTHERWISE NOTED
Resistors in OHM ¼w, 10%		
Dr. GEW	Eng.	Date
Dwg. No. 101-01A		

UNIVERSITY OF WISCONSIN
Electrical Standards and Instrumentation Laboratories
ZLD
1101



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Resistors in OHMS ¼w, 10%			
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Dwg. No. 101-02A			

UNIVERSITY OF WISCONSIN
Electrical Standards and Instrumentation Laboratories

SCD
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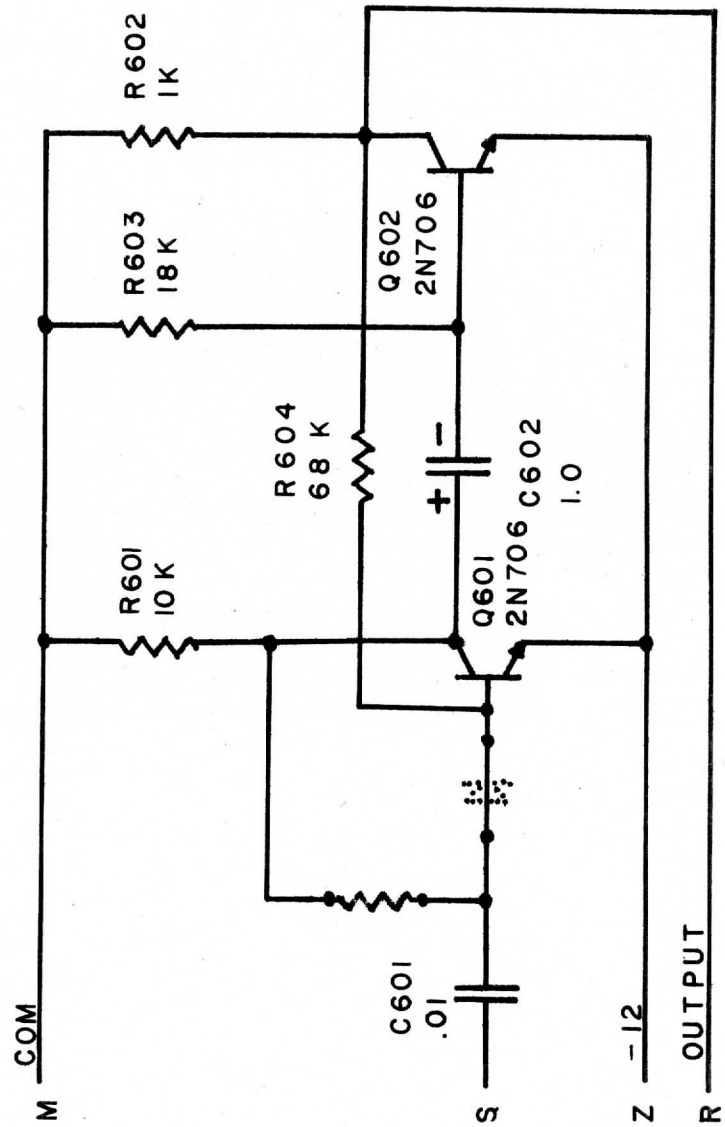

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Electrical Standards and Instrumentation Laboratories

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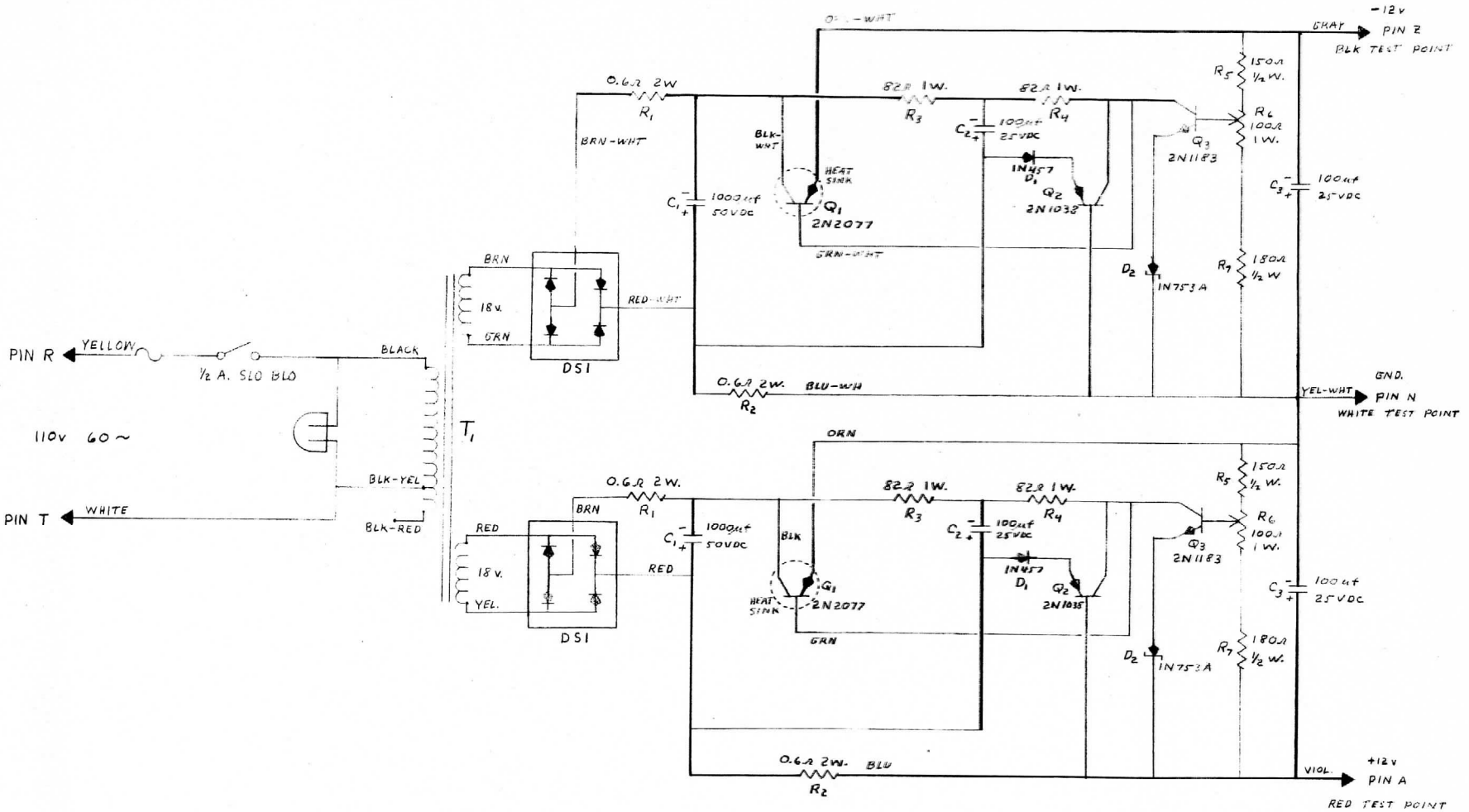
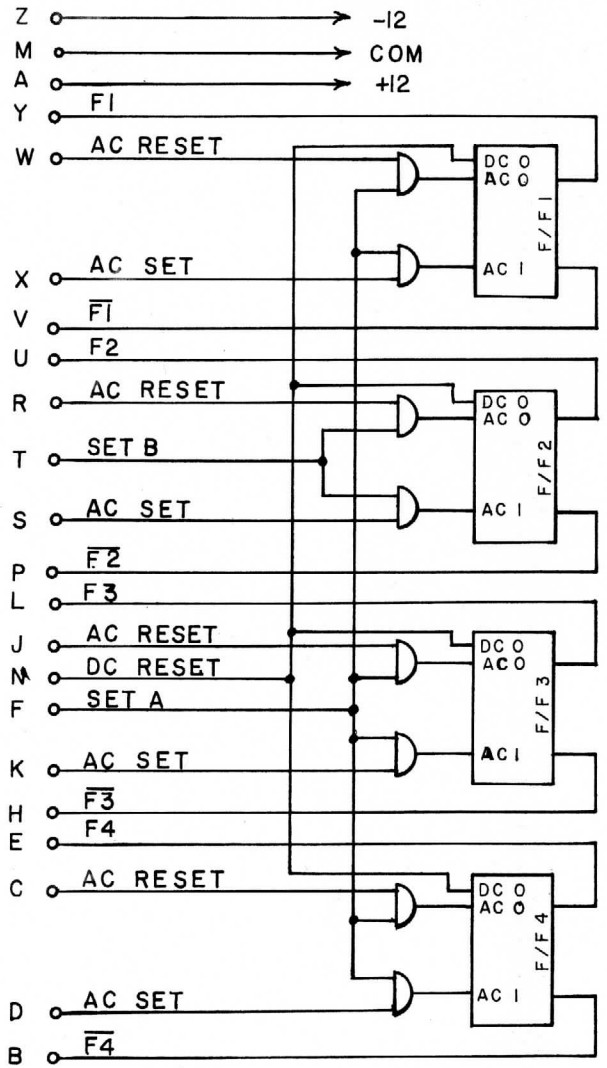


Dr. TJS		SEPT. 22, 1965
101-04A		

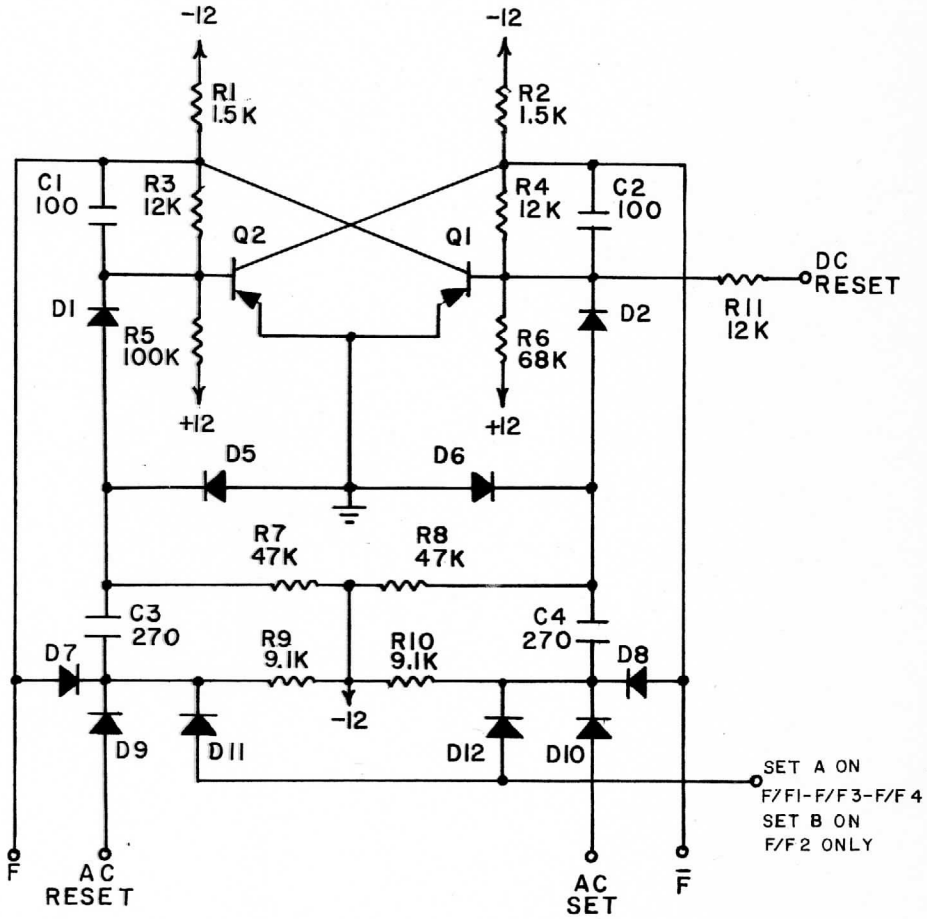
POWER SUPPLY 1001A

45

BLOCK DIAGRAM



TYPICAL CIRCUIT



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Resistors in OHMS		10%	
Dr. GEW	Eng.	Date	
Dwg. No. 101-05A			

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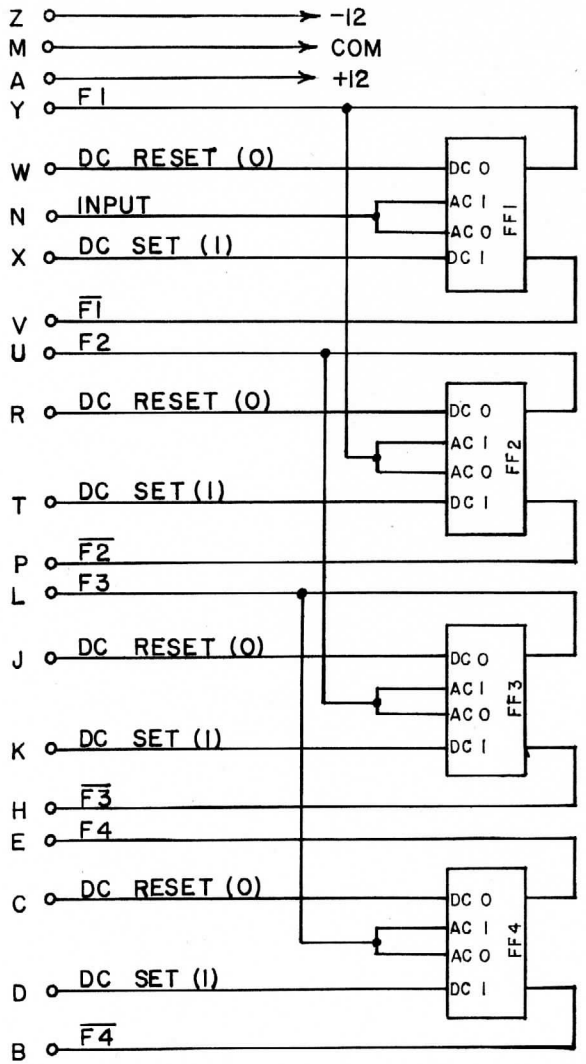
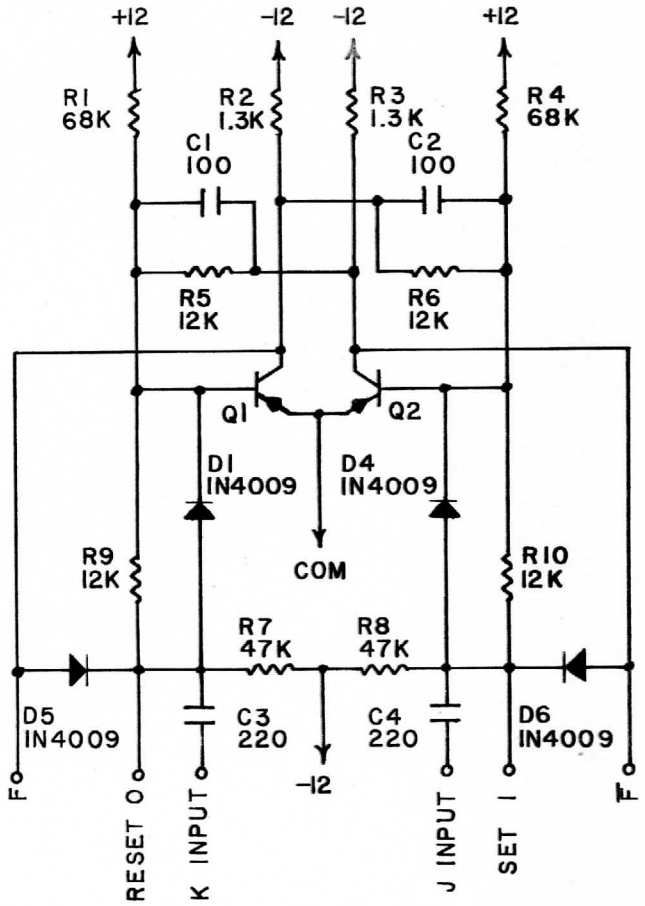
Electrical Standards and Instrumentation Laboratories

WYLE TYPE 4XG-M





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Resistors in OHMS		10%	
Dr. GEW	Eng.	Date	
Dwg. No. 101-06A			

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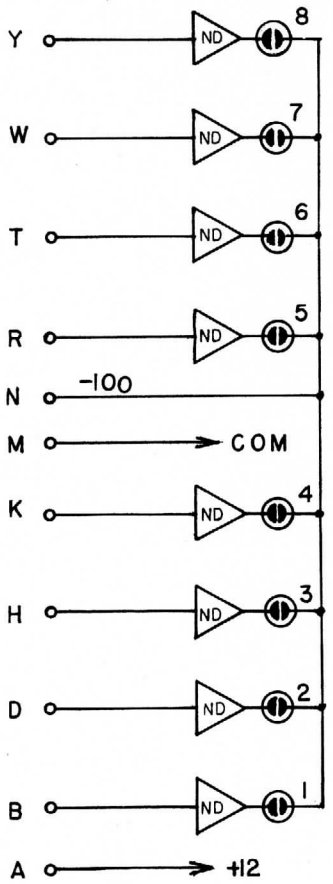
Electrical Standards and Instrumentation Laboratories

WYLE TYPE 4XH-M

47

BLOCK DIAGRAM



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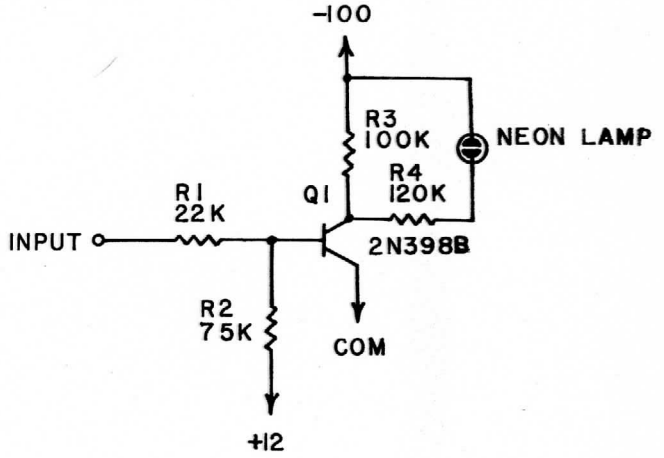

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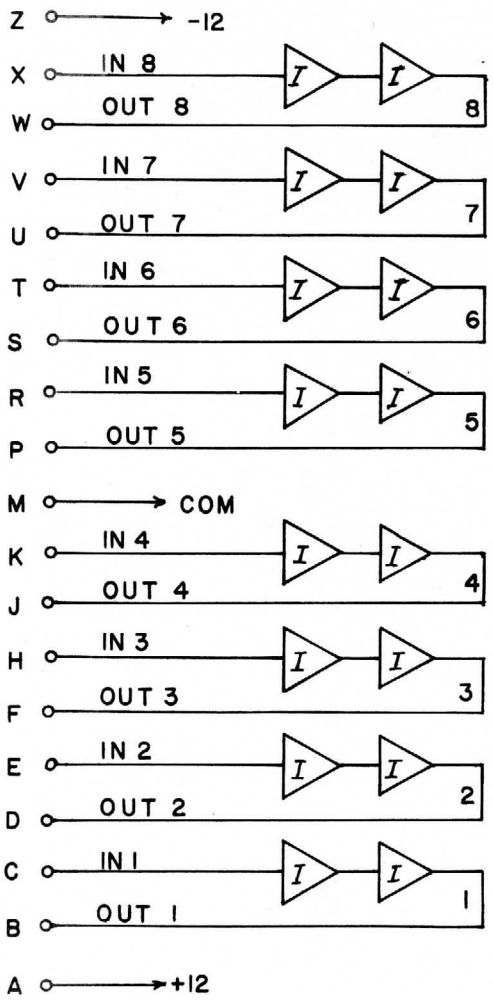
Dr. GEW	Eng.	Date	
Dwg. No. 101-07A			

UNIVERSITY OF WISCONSIN
Electrical Standards and Instrumentation Laboratories

WYLE
TYPE 8NI-D

BLOCK DIAGRAM



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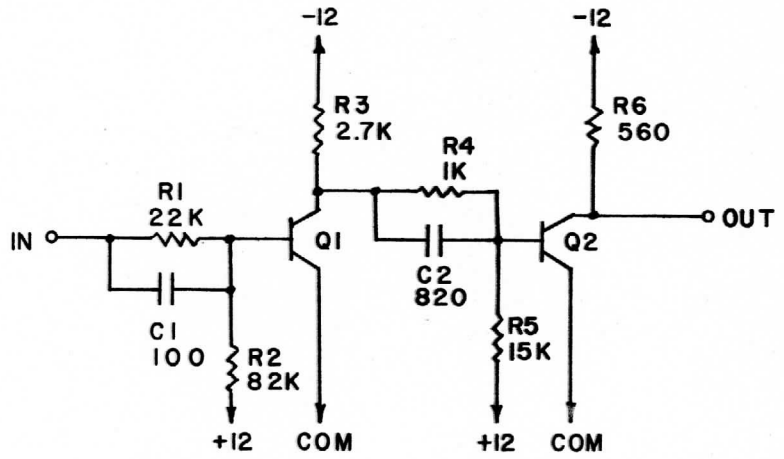

Capacitors in pf			UNLESS OTHERWISE NOTED
Resistors in OHMS		10%	
Dr. WCB	Eng.	Date	
Dwg. No. 101-08A			

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Electrical Standards and Instrumentation Laboratories

WYLE
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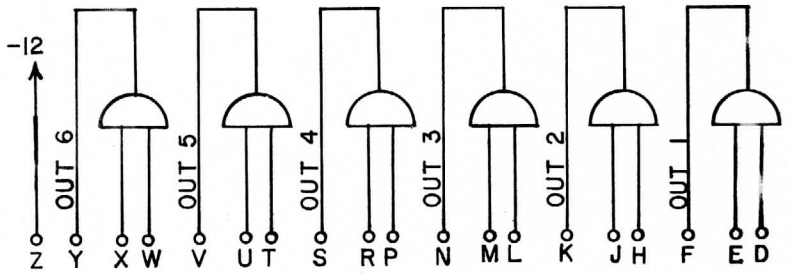

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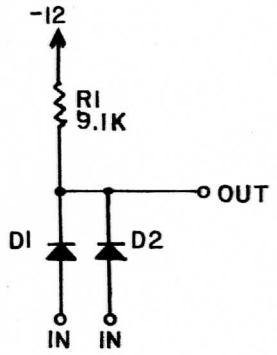
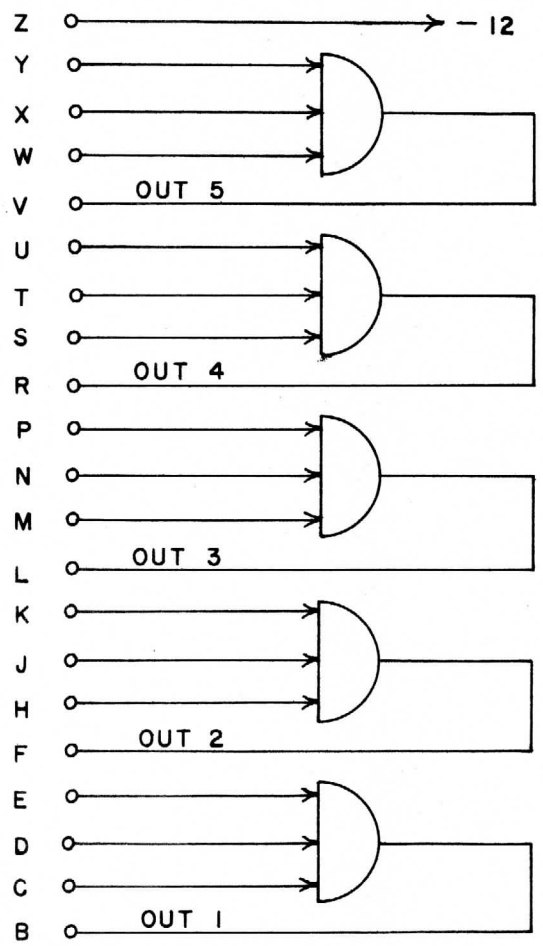


Capacitors in _____ Resistors in OHMS 10%			UNLESS OTHERWISE NOTED
Dr. GEW	Eng.	Date	
Dwg. No. 101-09 A			

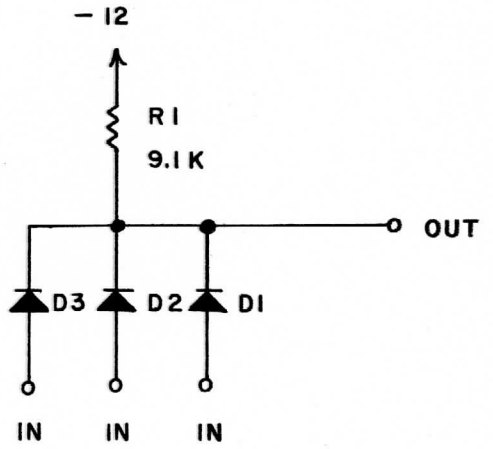
UNIVERSITY OF WISCONSIN
Electrical Standards and Instrumentation Laboratories

WYLE
TYPE A26-M

BLOCK DIAGRAM



TYPICAL CIRCUIT



Capacitors in _____ Resistors in OHMS 10%			UNLESS OTHERWISE NOTED
Dr. RAP	Eng.	Date	
Dwg. No. 101-10A			

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Electrical Standards and Instrumentation Laboratories

WYLE
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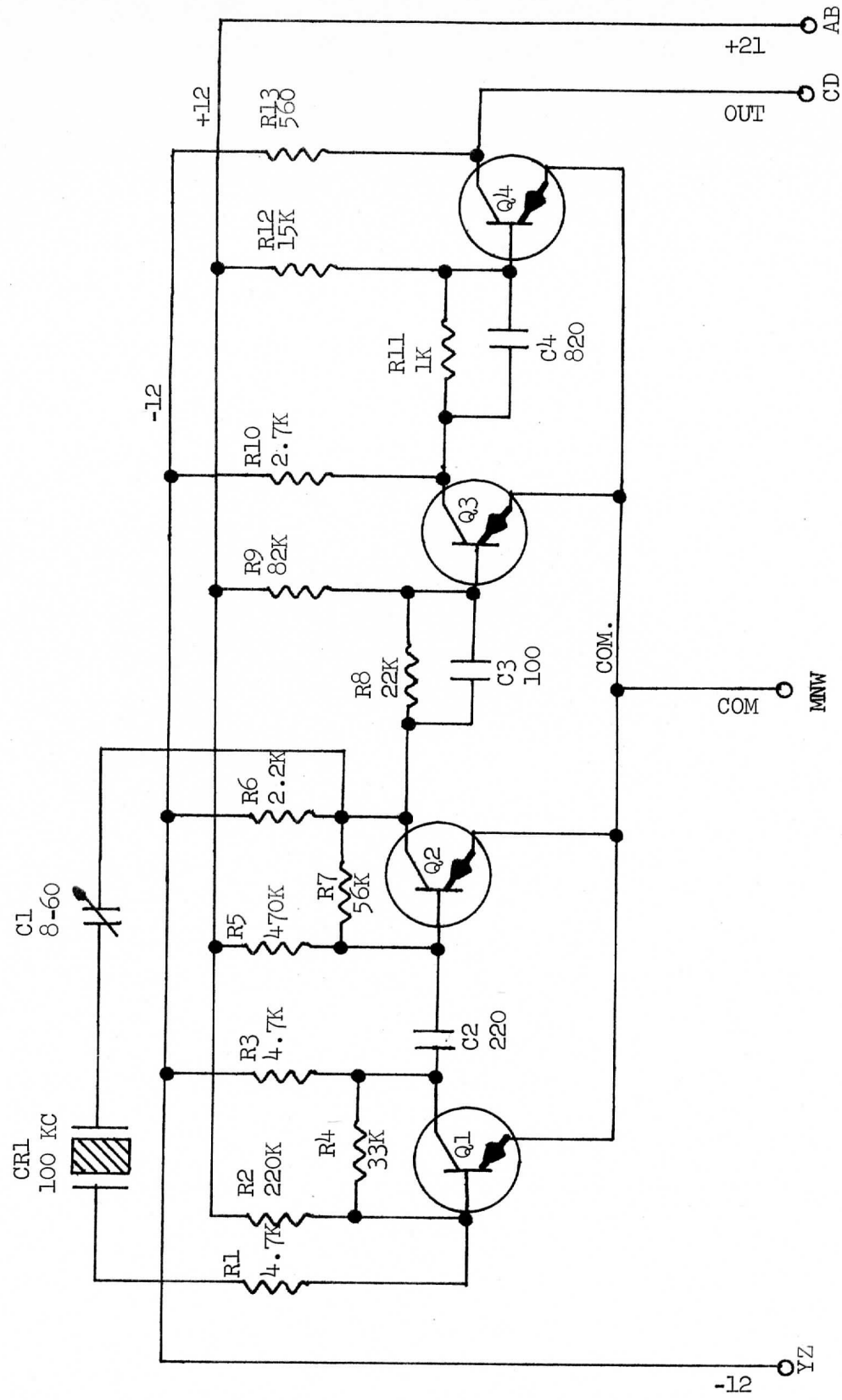
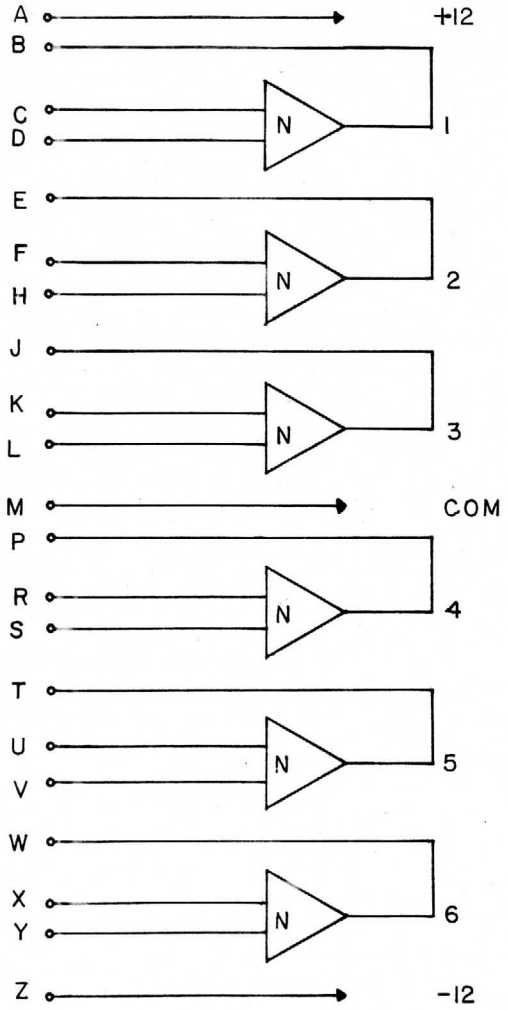


Capacitors in Pf			UNLESS OTHERWISE NOTED
Resistors in OHMS			10%
Dr. R.A.P.	Eng.	Date	
Dwg. No. LOI-LIA			

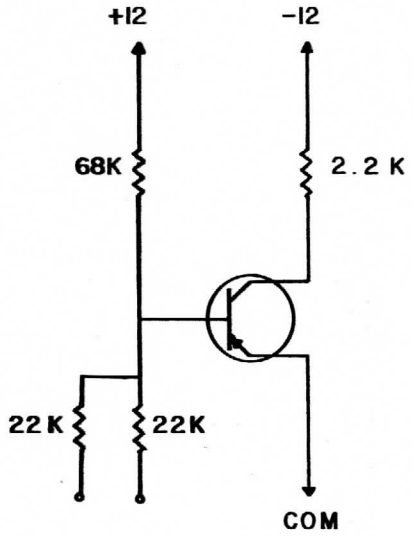
UNIVERSITY OF WISCONSIN
Electrical Standards and Instrumentation Laboratories

WYLE
TYPE KG100-M

BLOCK DIAGRAM



TYPICAL CIRCUIT



Capacitors in ~			UNLESS OTHERWISE NOTED
Resistors in Ohms		10%	
Dr. AWC	Eng.	Date	
Dwg. No. 101-12A			

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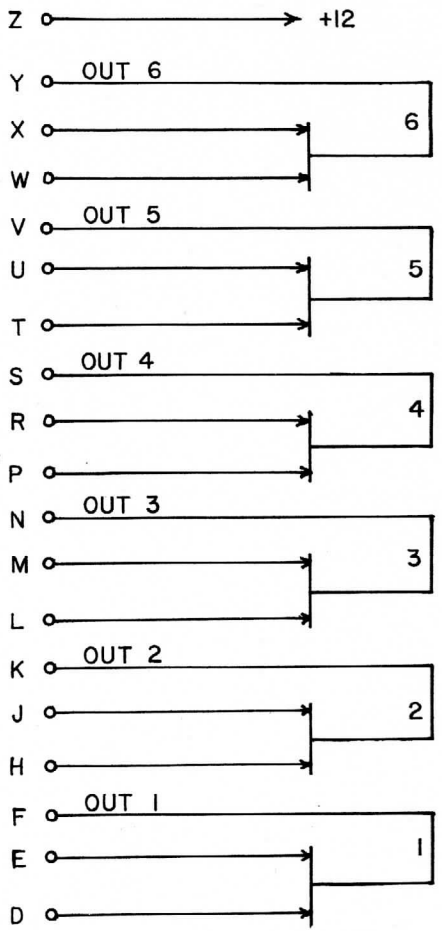
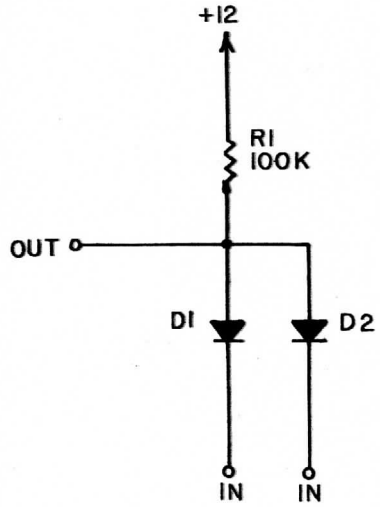
WYLE
TYPE N26-L

BLOCK DIAGRAM



TYPICAL CIRCUIT



Capacitors in _____ Resistors in OHMS 10%			UNLESS OTHERWISE NOTED
Dr. GEW	Eng.	Date	
Dwg. No. 101-13A			

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Electrical Standards and Instrumentation Laboratories

WYLE
TYPE 026-L

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SECTION 6

REPLACEABLE PARTS LIST

Table 6-1 Subcarrier Digitizer Replaceable Parts

Circuit Symbol	Description	Manufacturer	
		Name	Part No.
	PANEL, Front, Unit A	ESIL	
	PANEL, Front, Unit B	ESIL	
	PANEL, Rear, Unit A	ESIL	
	PANEL, Rear, Unit B	ESIL	
	ENCLOSURE, Card (Except side panels)	Elco	03-9016-06-1-00
	PANELS, Side, for Card Enclosure	ESIL	
	GUIDE, Printed Circuit Board, Polycarbonate plastic	Elco	53-9016-1204
	KNOB	Raytheon	DS125-3-2
	CONNECTOR, Printed Circuit Card, 22 pin	Amphenol	143-022-03
	MODULE, 4 General Purpose Flip-flops	Wyle	4XG-M
	MODULE, 4 Bit Binary Counter	Wyle	4XH-M
	MODULE, Six 2-input AND Gates	Wyle	A26-M
	MODULE, Five 3-input AND Gates	Wyle	A35-M
	MODULE, Six 2-input OR Gates	Wyle	O26-L
	MODULE, Six 2-input NOR Gates	Wyle	N26-L
	MODULE, 8 Squaring Amplifiers	Wyle	8SA-M
	MODULE, Crystal Controlled Oscillator	Wyle	KG100-M
	MODULE, 8 Neon Indicators and Drivers	Wyle	8NI-D
	MODULE, Zero Crossing Detector and Lamp Drivers	ESIL	ZLD-1101
	MODULE, Signal Detector	ESIL	SCD-1102
	MODULE, Preset Wiring Card	ESIL	PRS-1103
	MODULE, Test Point Card	ESIL	TPC-1104
	MODULE, Extension Card	ESIL	
	MODULE, Monostable Flip-flop	ESIL	MNO-1106
	POWER SUPPLY, ± 12V., 800 ma. output	ESIL	1001A
C101, C102, C103	CAPACITOR, 680 Pf., 1000 WVDC, 5%	Sprague	10TCU-T68
C201	CAPACITOR, 68 Pf., 1000 WVDC, 5%	Sprague	10TCC-Q68
C202, C602,	CAPACITOR, 0.1 μf., 35 WVDC	Kemet	KR1C35K
C203	CAPACITOR, 35 Pf., 1000 WVDC, 5%	Sprague	10TCC-Q39
C601	CAPACITOR, 0.01 μf., 200 WVDC, 10%	Sprague	192P-10392
C205, C204,	CAPACITOR, 4.7 μf., 35 WVDC	Kemet	K4R7C35K
D101, D102, D201	DIODE	Sylvania	1N627
D202, D203, D204, D205, D206	DIODE	TI	1N457A
I1	NEON CARTRIDGE, /W/Clear Lens	Dialco	38-937
I2, I3	NEON CARTRIDGE, /W/Red Lens	Dialco	38-931
I4	NEON CARTRIDGE, /W/Amber Lens	Dialco	38-933
I5	INCANDESCENT LAMP CARTRIDGE, /W/Red Lens	Dialco	39L-14-1471
	CLIP, Lamp Cartridge	Dialco	7538-XP51
	CONNECTOR, Lamp Cartridge	Dialco	7538-XP50

Table 6-1 (Cont'd.)

Circuit Symbol	Description	Manufacturer	
		Name	Part No.
J1	CONNECTOR, Panel, 5 Contact, Female	Amphenol	165-35
J2	CONNECTOR, Panel, 24 Contact, Female	Amphenol	165-28
J3	CONNECTOR, Panel, 24 Contact, Male	Amphenol	165-27
J4	CONNECTOR, Panel, 20 Contact, Male	Amphenol	165-11
J5	CONNECTOR, Panel, Power, Male	Amphenol	160-5
J6	JACK, Phone	Switch-craft	42A
P1	CONNECTOR, Cable, 5 Contact, Female p/o W1	Amphenol	165-34
P2	CONNECTOR, Cable, 24 Contact, Male p/o W2	Amphenol	165-25
P3	CONNECTOR, Cable, 24 Contact, Female p/o W2	Amphenol	165-26
P4	CONNECTOR, Cable, 20 Contact, Female p/o W3	Amphenol	165-10
P6	PLUG, Phone, p/o W4	Switch-craft	755
	CORD, Power, 3-Conductor	Belden	17460
Q101, Q102, Q201, Q202 Q203, Q204 Q205	TRANSISTOR	Fairchild	2N3638
Q103, Q104, Q207	TRANSISTOR	TI	2N1305
Q105-1, Q105-2, Q105-3, Q105-4	TRANSISTOR	RCA	2N398B
Q206	TRANSISTOR	TI	2N1304
Q601, Q602	TRANSISTOR	RCA	2N706
	TRANSISTOR MOUNTS	Thermal-loy	7717-5
R101, R115-1, R115-2, R115-3, R115-4, R116-1, R116-2, R116-3, R116-4	RESISTOR, 100K, 1/4W., 10%		
R102	RESISTOR, 240K, 1/4W., 5%		
R103	RESISTOR, 4.7K, 1/4W., 10%		
R104, R106, R107, R109, R204, R211, R601, R218	RESISTOR, 10K, 1/4W., 10%		
R105, R110, R111, R206, R208, R220, R602	RESISTOR, 1K, 1/4W., 10%		
R108, R215 R604	RESISTOR, 68K, 1/4W., 10%		
R112, R113-1, R113-2, R113-3 R114-4, R216, R217	RESISTOR, 22K, 1/4W., 10%		
R114-1, R114-2 R114-3, R114-4	RESISTOR, 75K, 1/4W., 5%		
R201	RESISTOR, 3.3K, 1/4W., 10%		

Table 6-1 (Cont'd.)

Circuit Symbol	Description	Manufacturer	
		Name	Part No.
R205	RESISTOR, 33K, 1/4W., 10%		
R203	RESISTOR, 5.6K, 1/4W., 5%		
R207,R221	RESISTOR, 15K, 1/4W., 10%		
R209,213	RESISTOR, 47K, 1/4W., 10%		
R210, R214	RESISTOR, 33K, 1/4W., 10%		
R212	RESISTOR, 150K, 1/4W., 10%		
R219, R222	RESISTOR, 560, 1/2W., 10%		
R603	RESISTOR, 18K, 1/4W., 5%		
S1	SWITCH, Toggle, DPDT	Alcoswitch	215N
S2	SWITCH, Rotary, 3 Pos., 2 Section	Centralab	2505
W1	CABLE ASSEMBLY	ESIL	
W2	CABLE ASSEMBLY	ESIL	
W3	CABLE ASSEMBLY	ESIL	

APPENDIX A

TECHNICAL NOTE TN-FMD-1

FM Subcarrier Digitizer Output and Output Format

1. Tape Format

The content of the 8-bit data counter is read out in two characters for recording on magnetic tape on tracks 1, 2, 4, 8, A, B in the format shown below:

Track	First Character	Second Character
1	α_4	1
2	α_5	1
4	α_6	α_0
8	α_7	α_1
A	1	α_2
B	1	α_3

← Direction of tape motion

A logical 1 will always appear on tracks A and B of the first character and on tracks 1 and 2 of the second character. A logical 1 or 0 in any other position corresponds to α_i = 1 or 0 respectively, where the α_i's represent the bit recorded.

Example

1	0	1
2	1	1
4	1	0
8	0	1
A	1	0
B	1	0

denotes

$0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 =$

$01100010_2 = 98_{10}$

An inter-record gap is generated and the operation of the Digitizer is inhibited when no usable signal is present.

2. Output and Frequency Relationships

The real time subcarrier frequency range, (10,500 Kc. ± 7.5%) is divided by 16 in playback to give a new frequency range of f = (656.25 cps. ± 7.5%). The center and upper and lower band edge frequencies are now:

f_{max} = 705.47 cps. = f_c + 49.22 cps

f_c = 656.25 cps.

f_{min} = 607.03 cps. = f_c - 49.22 cps.

The duration of eight complete cycles of f is measured in each sample by counting with a 100 Kc clock to an accuracy of ± 0.01 ms. The actual measured durations and number of clock pulses counted, n, at f_{min}, f_c, and f_{max} using

$$T = 8 \left(\frac{1}{f}\right)$$

are

T_{min} = 13.18 ms. n = 1318

T_c = 12.19 ms. n = 1219

T_{max} = 11.34 ms. n = 1134

respectively.

The total number of clock pulses into the counter will normally vary over a range of 184 counts, i.e. 1219(+ 99, - 85)

Let

N_p = preset number in which a 1 digit corresponds to the F output of that counter bit in a logical 1 state, i.e. counting forward.

N = counter number (counting forward)

N_c = counter number obtained with input frequency f_c

N_o = output number = 255-N

We have

$$n + N_p = N + (M \times 256) \qquad \text{Eq. 1}$$

where M is the number of times the counter passes through zero.

As the range of the counter is larger than the expected deviation in the number of counts, we select a preset number which will result in an equal "pad" in terms of frequency deviation at each end of the counting range. This number is obtained by requiring that the counter number N_c obtained with center frequency input satisfy the relation

$$\frac{N_c}{\text{range of counter}} = \frac{\text{negative count deviation}}{\text{range of counts}}$$

or $$N_c = \frac{256 \times 85}{184} = 118$$

Using equation 1, with $N = N_c$ and $n = 1219$

$$1219 + N_p = 118 + (M \times 256)$$

Now $$0 \leq N_p \leq 255$$

from which $$N_p = 179 \text{ and } M = 5$$

Provision is made for even numbered presets only, so assume $N_p = 180$. Then the counter number at center frequency will be 119. A frequency deviation of ± 10% will not exceed the range of the counter for this value of N_p.

The subcarrier frequency is

$$f = \frac{8}{T} \qquad \text{Eq. 2}$$

where T is the duration of the sample of eight complete cycles of subcarrier.

Since there is one count every 10^{-5} sec., or

$$n = 10^5 T$$

Eq. 2 becomes $$f = \frac{8 \times 10^5}{n}$$

Then, from Eq. 1 with M = 5,

$$f = \frac{8 \times 10^5}{(N + 1280 - N_p)} \qquad \text{Eq. 3}$$

Using $N_p = 180$ counts

and $$N_o = 255 - N \qquad \text{Eq. 4}$$

$$f = \frac{8 \times 10^5}{1355 - N_o} \text{ cycles/sec.} \qquad \text{Eq. 5}$$

More generally, if the frequency deviation is assumed to be no greater than ± 7.5%,

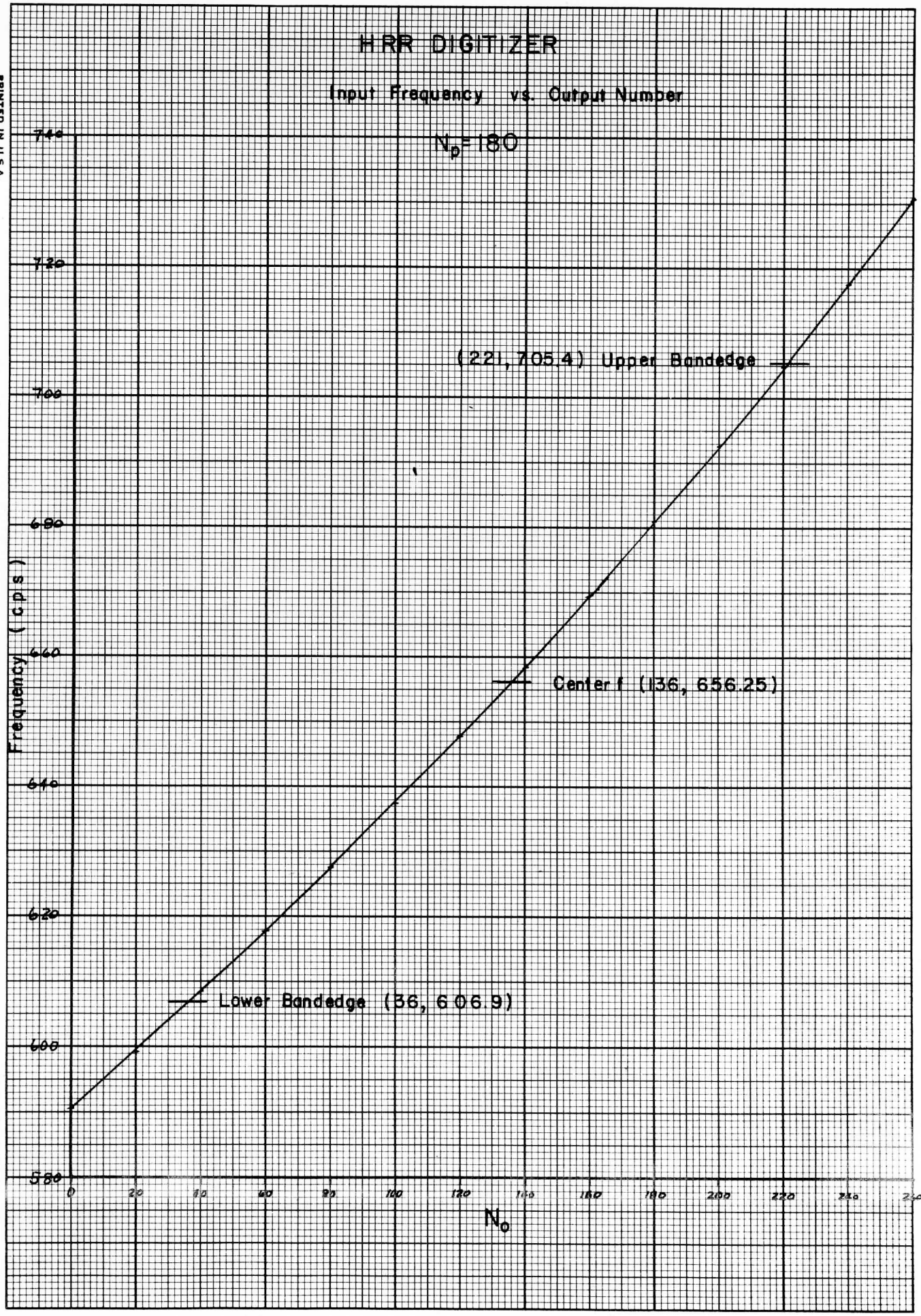
$$f = \frac{8 \times 10^5}{1535 - N_p - N_o} \qquad \text{Eq. 6}$$

where N_p is restricted to the interval

$$146 \leq N_p < 218$$

so that the range of the counter is not exceeded. N_p can be set anywhere within the above range to provide greater pad at one end or the other of the scale.

The plot on page 5 illustrates the relationship between input frequency and data counter output number. The data points were calculated using Eq. 6 with $N_p = 180$.



APPENDIX B

Logic Operations

1.1 LOGIC CIRCUITS

1.1.1 GENERAL

The following circuit representations and associated tables describe the operations performed by each type of logic circuit used in the Subcarrier Digitizer.

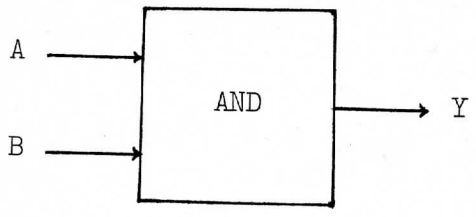
In this system, the voltages associated with each logic level are:

Logical 1	-10 ± 2 volts
Logical 0	-0.25 ± 0.25 volts

1.1.2 GATES AND AMPLIFIERS

These circuits are dc coupled, and the output is uniquely determined by the dc voltage levels present at the inputs.

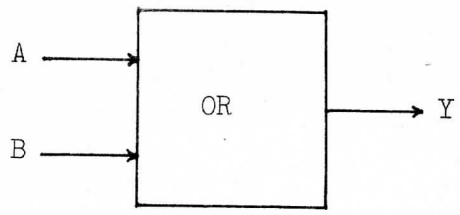
TWO INPUT AND



INPUT		OUTPUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

For more than two inputs, all inputs must be at logical 1 to produce a logical 1 output. Alternatively, if any input is a logical 0, the output is a logical 0.

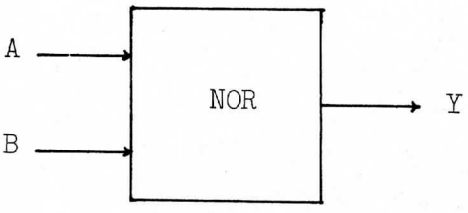
TWO INPUT OR



INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

If any input is a logical 1, the output is a logical 1.

TWO INPUT NOR

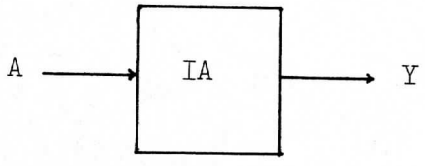


INPUT		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The NOR operation is simply the complement (opposite) of the OR.

Note that if one input of a two-input NOR is held at logical 0, the output is the complement of the logic state of the other input. Inverting amplifiers in the Subcarrier Digitizer are formed from NOR circuits in this way.

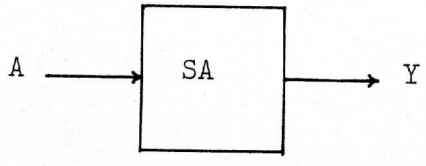
INVERTING AMPLIFIERS



INPUT	OUTPUT
A	Y
0	1
1	0

The complement of a signal A is denoted by $\overline{A}$. The inverting amplifier performs the operation $Y = \overline{A}$.

SQUARING AMPLIFIERS



INPUT	OUTPUT
A	Y
0	0
1	1

The output follows the input, Y = A. This circuit is used to meet loading requirements.

1.1.3 FLIP-FLOPS

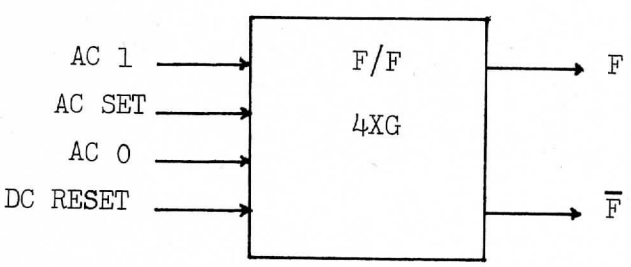
Two types of flip-flops (bistable multivibrators) are used in the Subcarrier Digitizer. These circuits have two stable states, and will remain in either of these states indefinitely until some form of external triggering is applied.

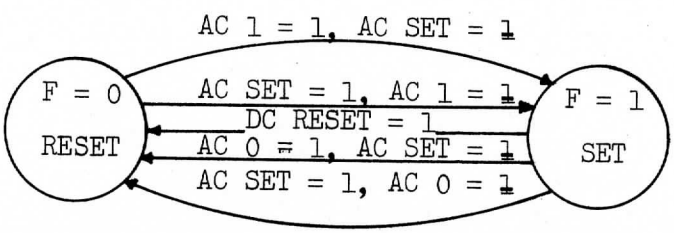
Two outputs are available from each flip-flop, which are designated F and $\overline{F}$. $\overline{F}$ is the complement of F. A flip-flop is said to be "set" when F = 1 and "reset" when F = 0.

Certain inputs to a flip-flop are AC coupled. The state of the flip-flop may change only when the transition from logical 0 to logical 1 (denoted by $\underline{1}$) occurs on these inputs.

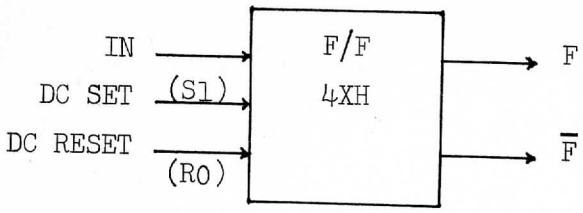
The state diagrams given below describe the inputs necessary to change the state of each type of flip-flop. If none of the input combinations described are applied, the circuit will not change state. If, at any instant, two input combinations occur which conflict (i.e. arrows point to opposite states) the resulting state is indeterminate.

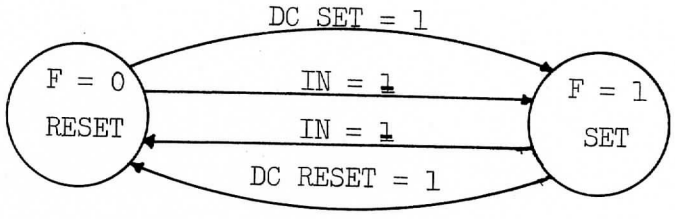
4 X G FLIP-FLOP





4 X H FLIP-FLOP (COUNTER)

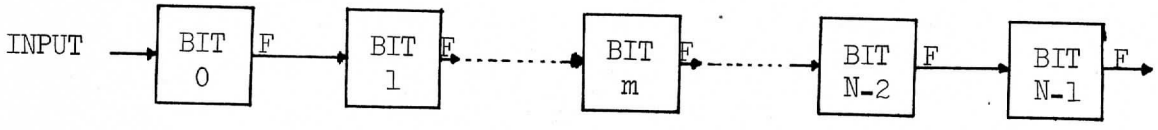




1.2 CONVERSION OF COUNTER STATE TO DECIMAL NUMBERS

Each of the many possible states of a counter is associated with a specific decimal number. These are chosen in such a way that a change to the next possible counter state increases the value of the associated decimal number by one.

The number is derived in the following way. A counter containing N stages has its stages (or bits) numbered from 0 to N - 1, as shown in the figure below.

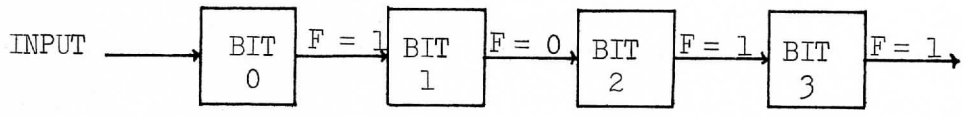


For each bit m (m = 0, 1, 2, · · ·N-1), let α_m = 1 or 0 depending on whether the F output is a logical 1 or 0 respectively. Then the decimal number D is found by the expression

$$D = \sum_{m=0}^{N-1} \alpha_m 2^m = \alpha_o \cdot 2^o + \alpha_1 \cdot 2^1 + \cdots + \alpha_{N-1} 2^{N-1}$$

Example:

A four bit counter is in the state shown below.



Then $\alpha_o = 1$, $\alpha_1 = 0$, $\alpha_2 = 1$, $\alpha_3 = 1$

and $D = \alpha_o \cdot 2^o + \alpha_1 \cdot 2^1 + \alpha_2 \cdot 2^2 + \alpha_3 \cdot 2^3$

$= 1 \cdot 1 + 0 \cdot 2 + 1 \cdot 4 + 1 \cdot 8$

$= 1 + 0 + 4 + 8$

$= 13$

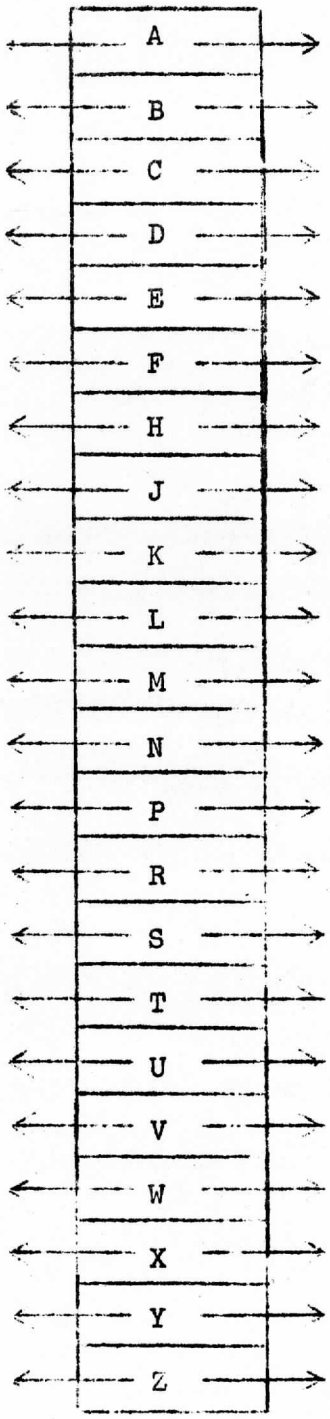
In the text of this manual, D is referred to as the <u>counter number</u>.

[redacted] Unit A to Unit B [redacted]

		J2-P2	Via W2	P3-J3
	Data Pulses	A6-V	A	B9-N
	Sample Gate	A11-C	B	B6-S
f	Buffer Reset	A10-D	C	B10-N
$\bar{d}$	Buffer Readout	A8-C	D	B16-V
d	Buffer Readout	A12-E	E	B14-U
	Step	A7-F	F	B16-X
$\bar{a}$	Counter Readout	A8-F	H	B6-R
a	Counter Readout	A10-U	J	B14-H
	Common	A02-N	K	B02-N
c	Counter Reset	A10-F	L	B8-N
	Mode	A15-E	M	B02-E
	Common	A02-V	N	B02-V
	AC	A02-R	P	B02-R
	AC	A02-T	R	B02-T
	Mode	A16-J	S	B7-S
			T	
			U	
			V	
			W	
			X	
			Y	
			Z	

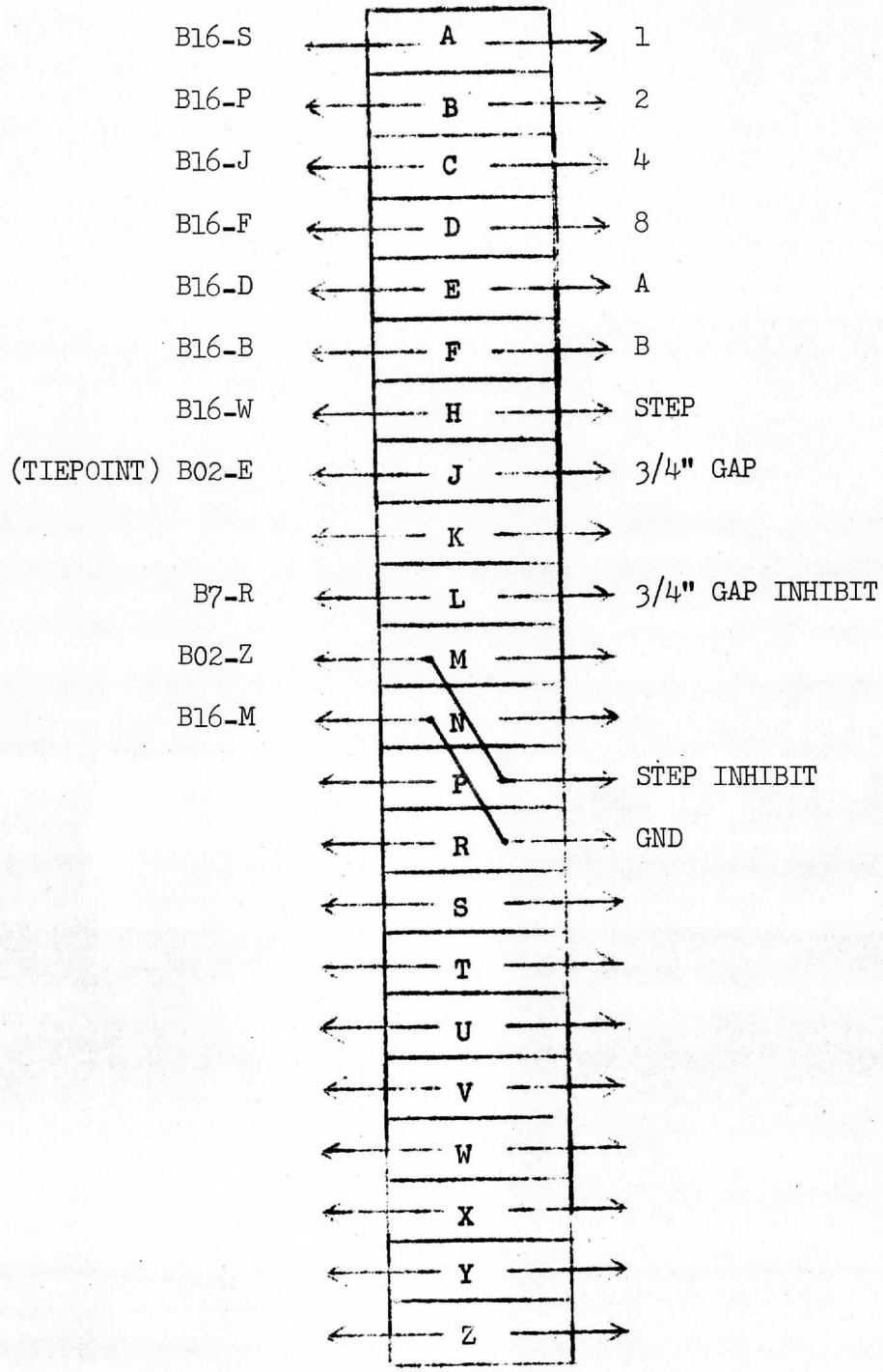
CARD TYPE xxxxxxxxxxxxxxxx EMR to Unit A CARD NO xxxxxxxxxxxxxx

TB1		Via W1	P1-J1	
(BLACK)	20	A	A02-V	(COM)
(BROWN)	19	B	A15-S	(LIM)
(RED)	16	C	A16-B	(-100 VDC)
(GREEN)	18	D	A02-N	(COM)
(WHITE)	17	E	A16-X	(VCO)



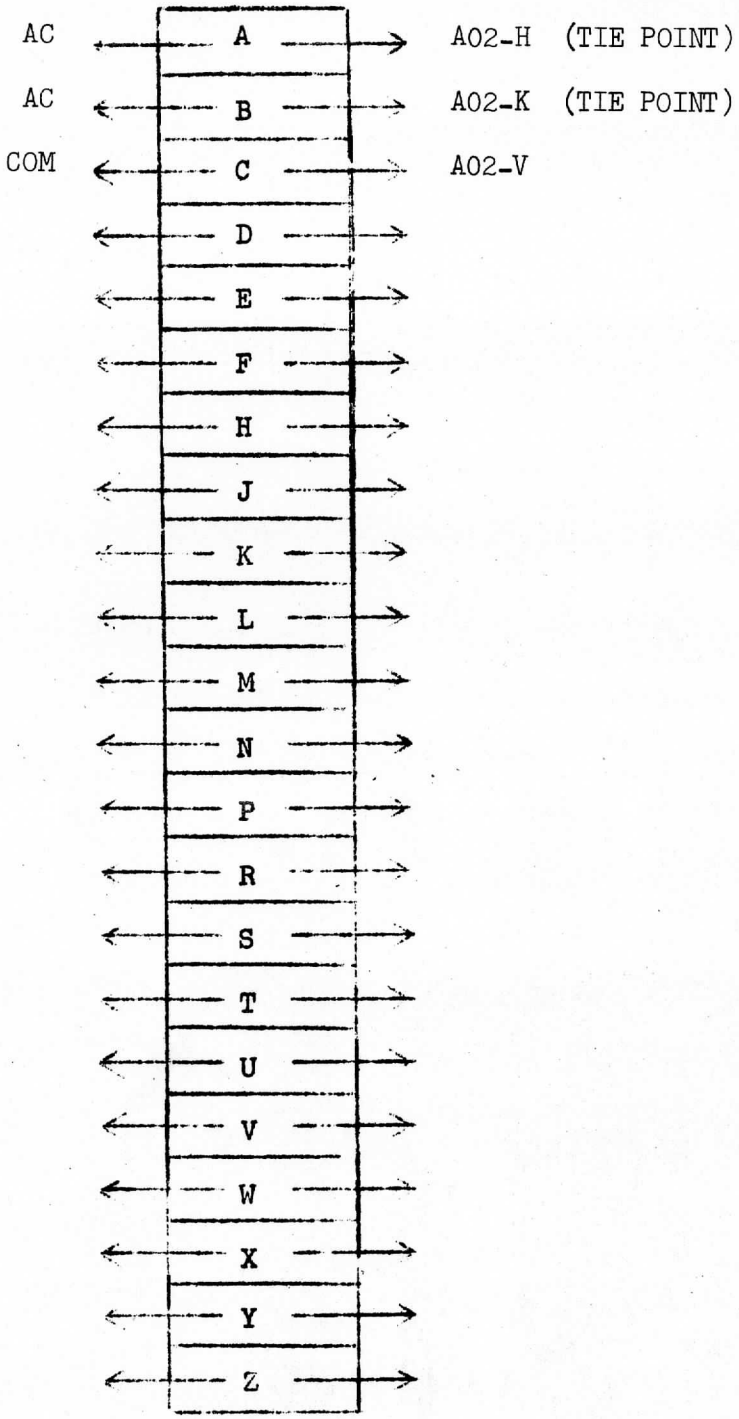
CARD TYPE XXXXXXXXXXXXXXX Unit B to Recorder CARD NO XXXXXXXXXXXX

J4-P4 Via W3 P5-(J105)



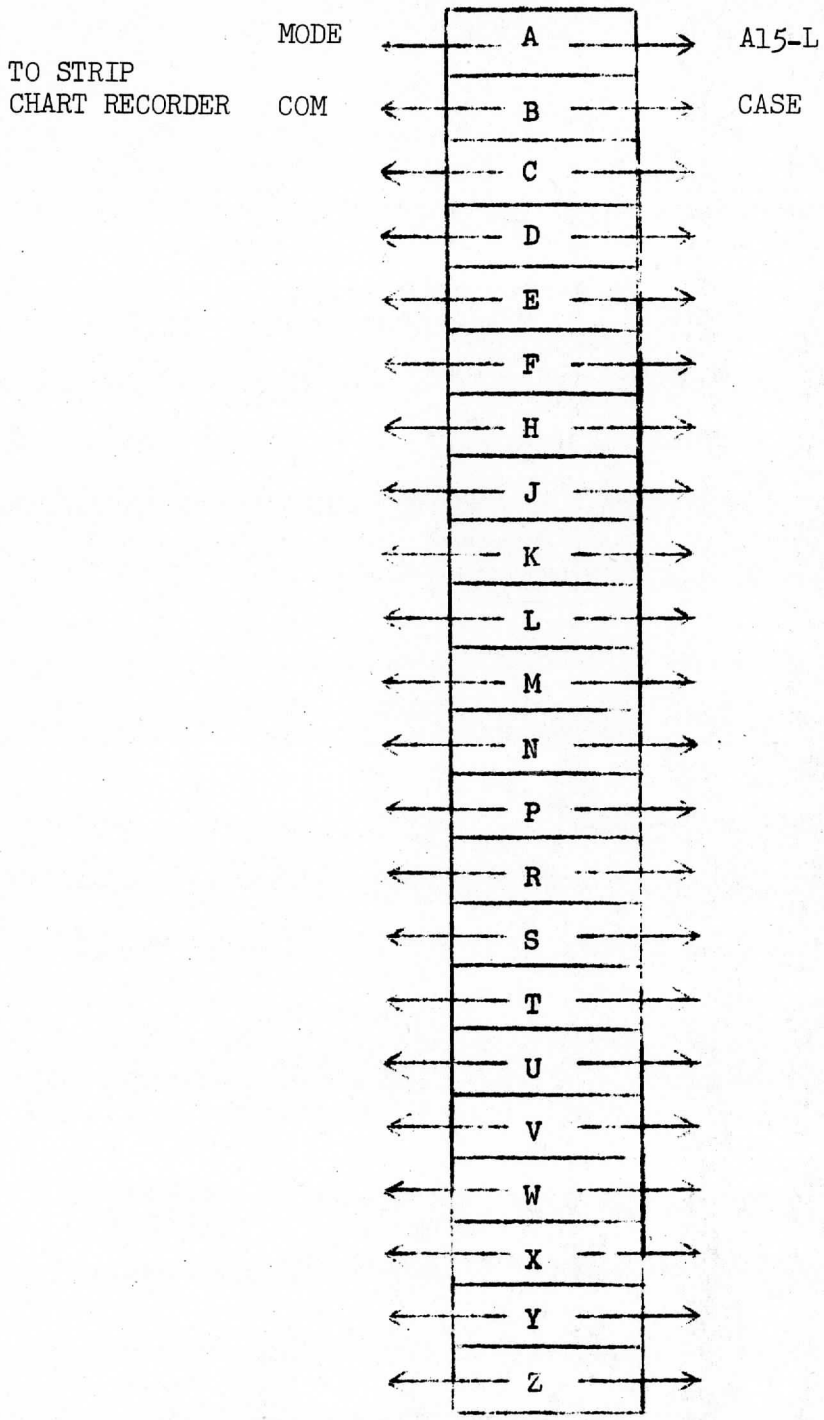
CARD TYPE Power Receptacle CARD NO

J5

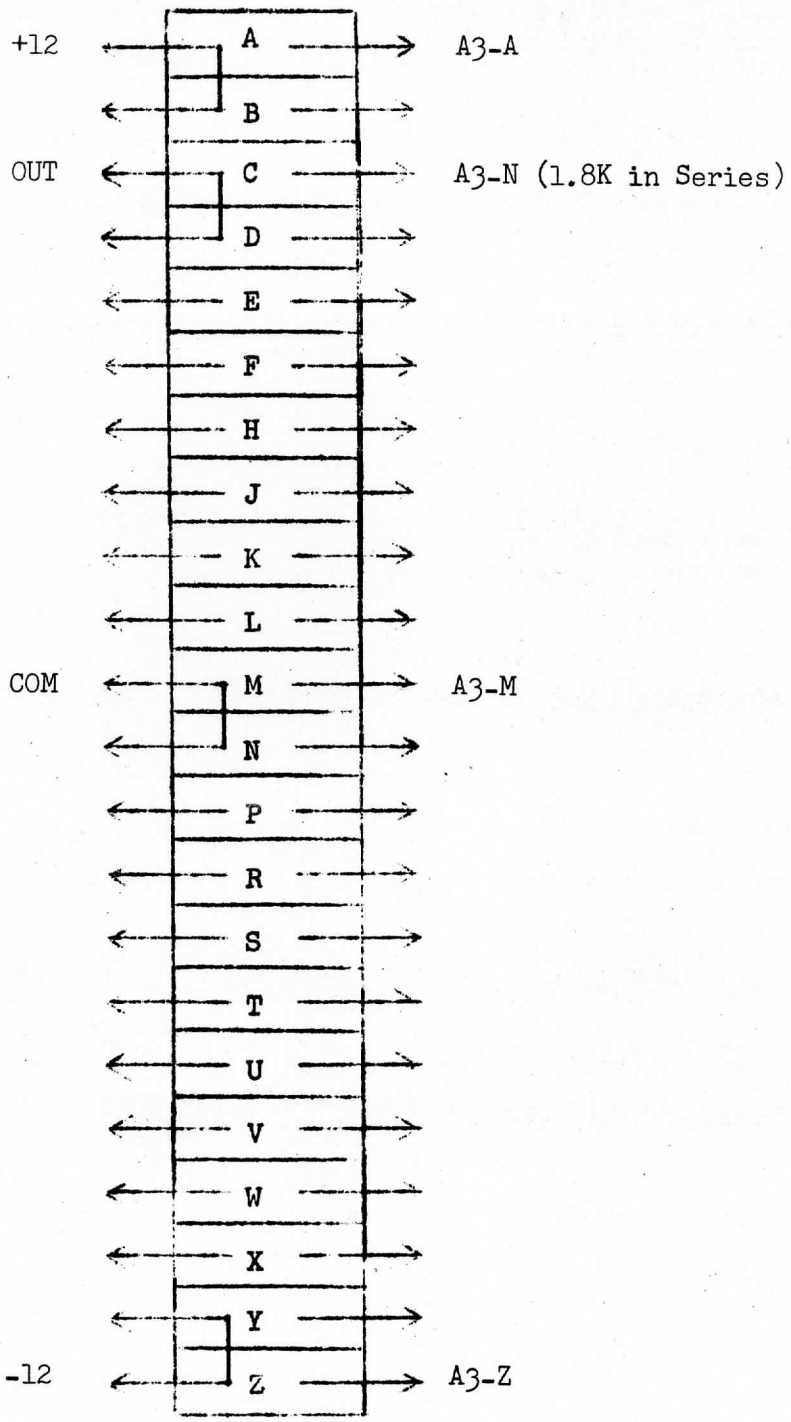


CARD TYPE xxxxxxxxxxxxxxxx Phone Jack CARD NO xxxxxxxxxxxxxxx

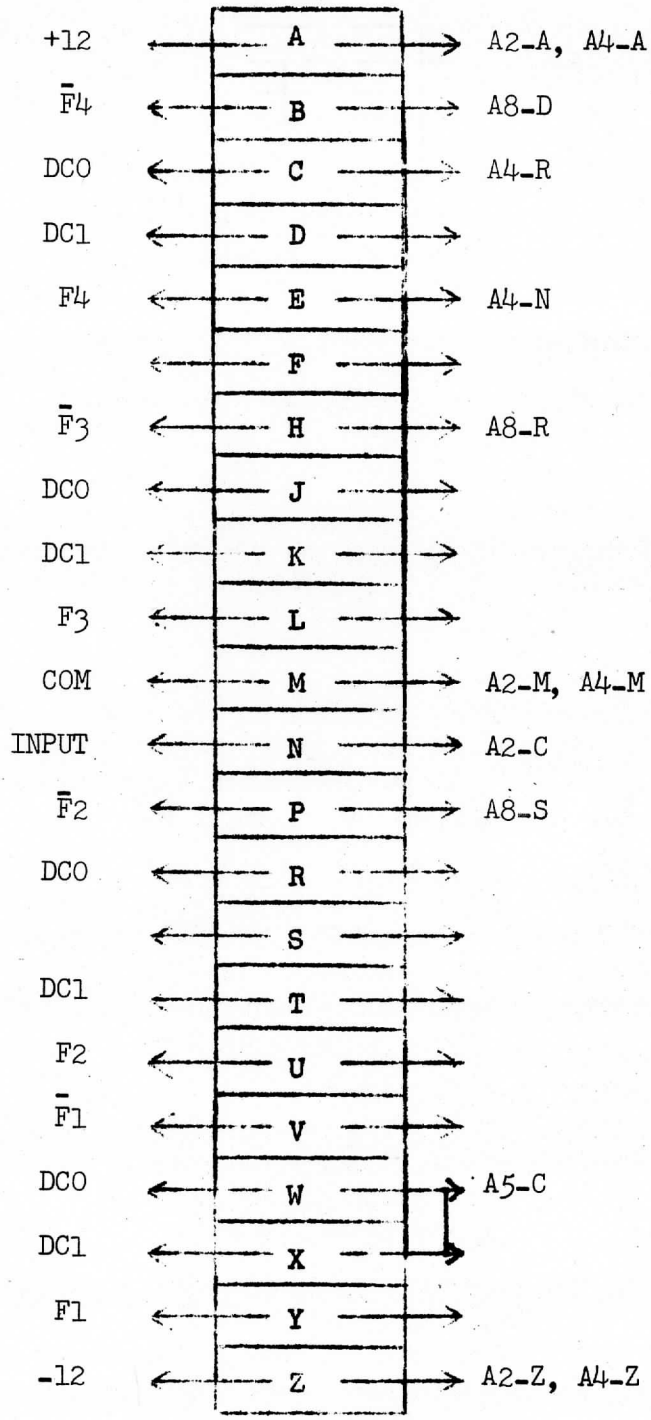
J6



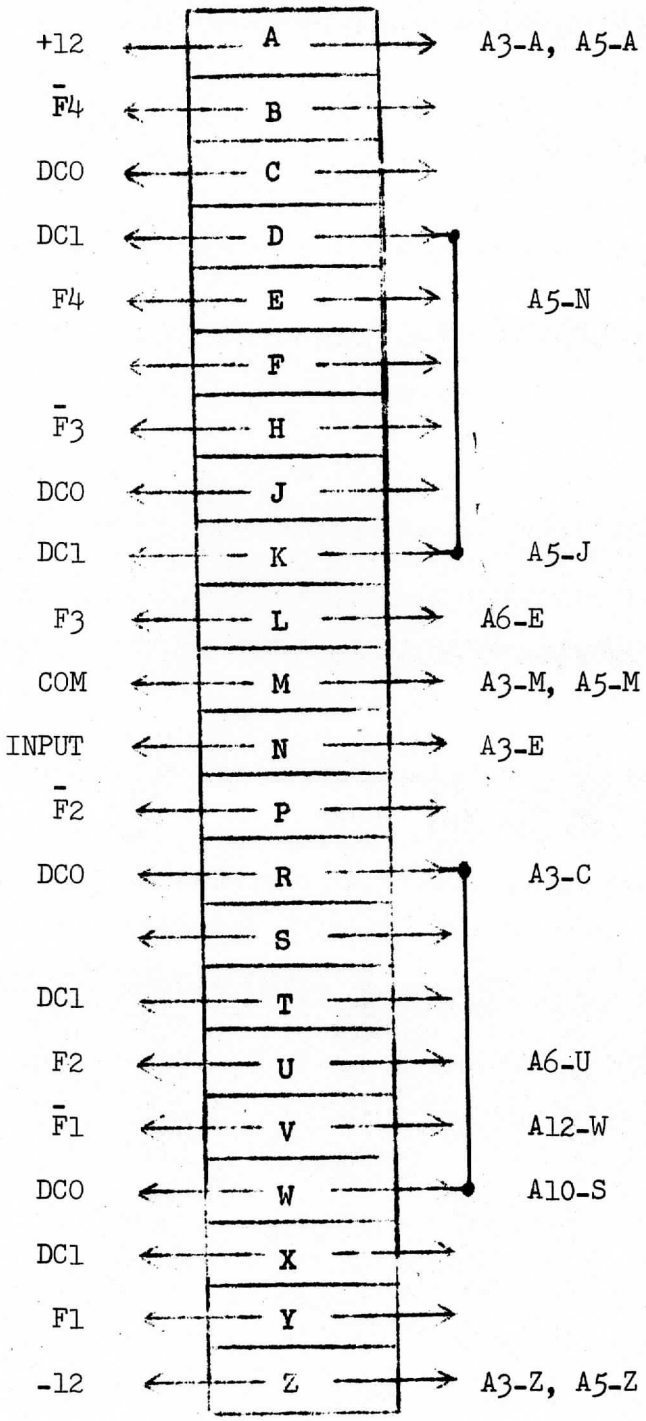
CARD TYPE KG-100 **CARD NO.** A2



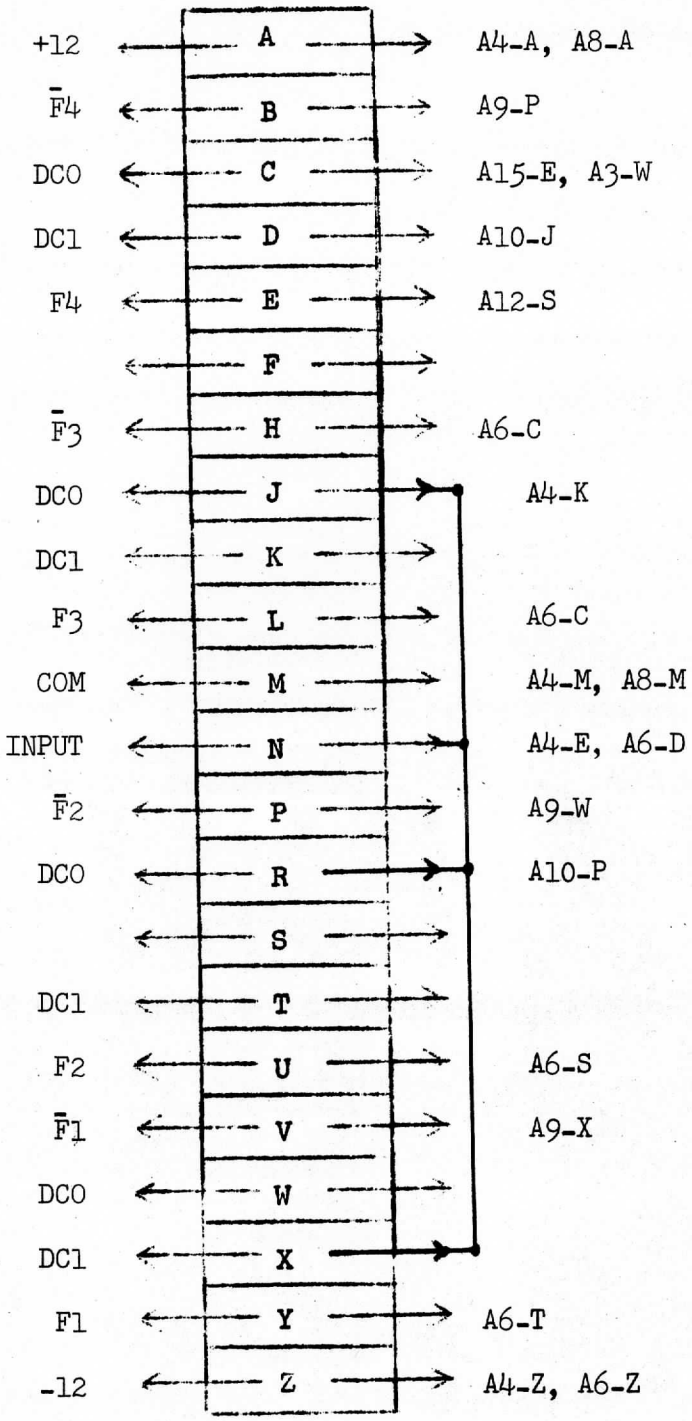
CARD TYPE 4XH **CARD NO.** A3



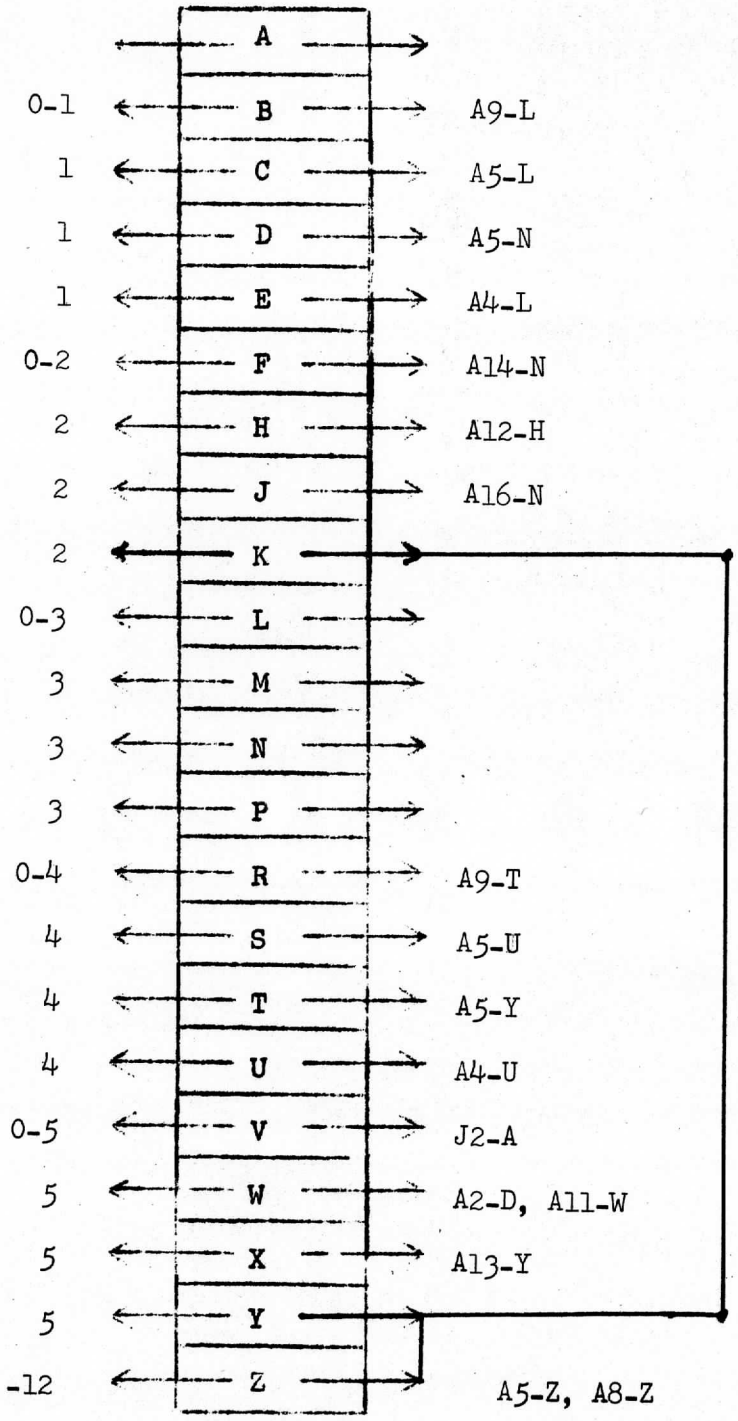
CARD TYPE 4XH CARD NO. A4



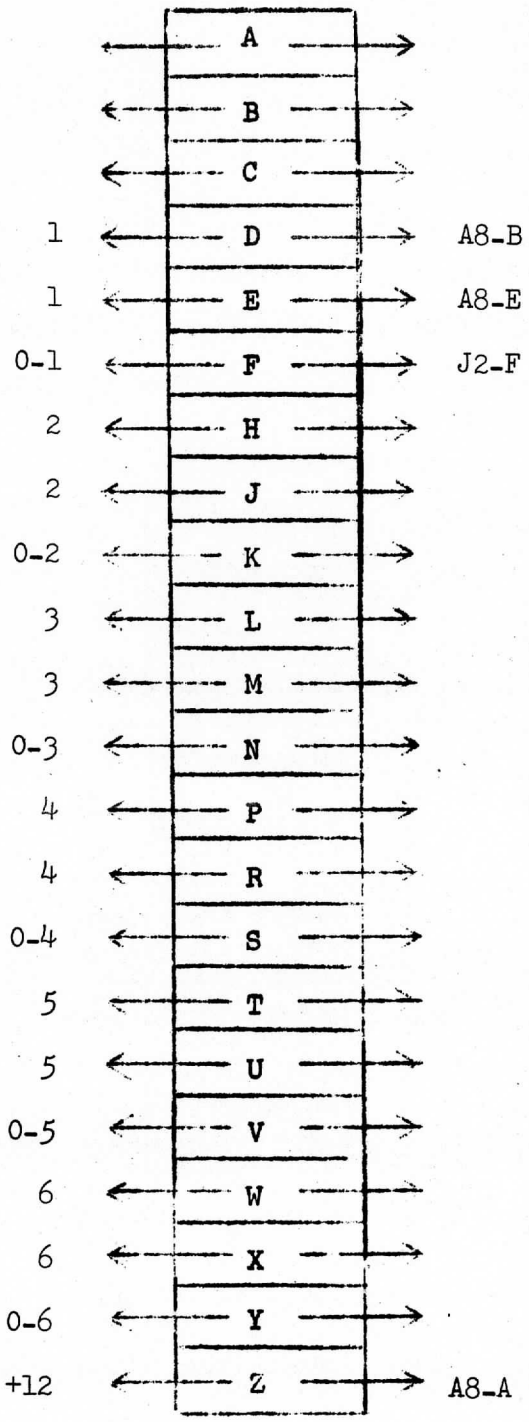
CARD TYPE 4XH **CARD NO.** A5



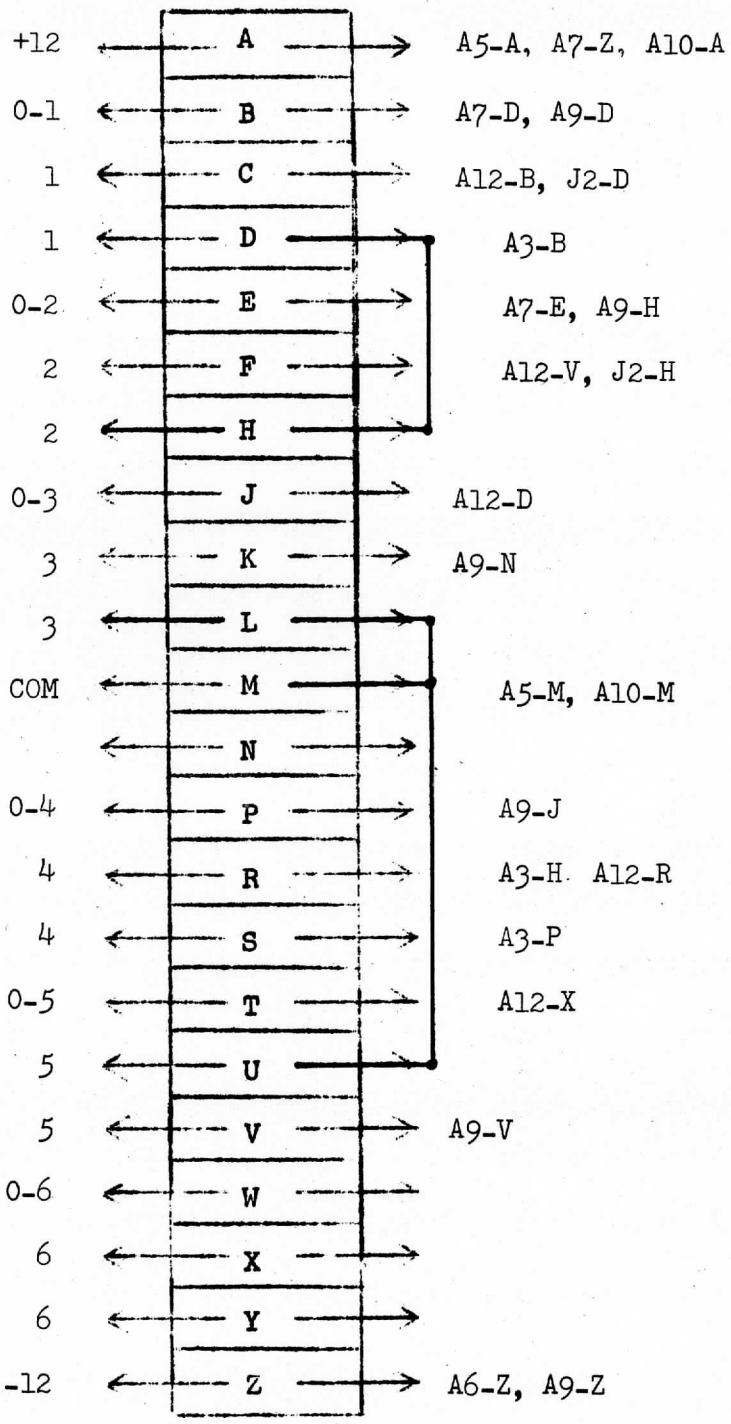
CARD TYPE A35 CARD NO. A6



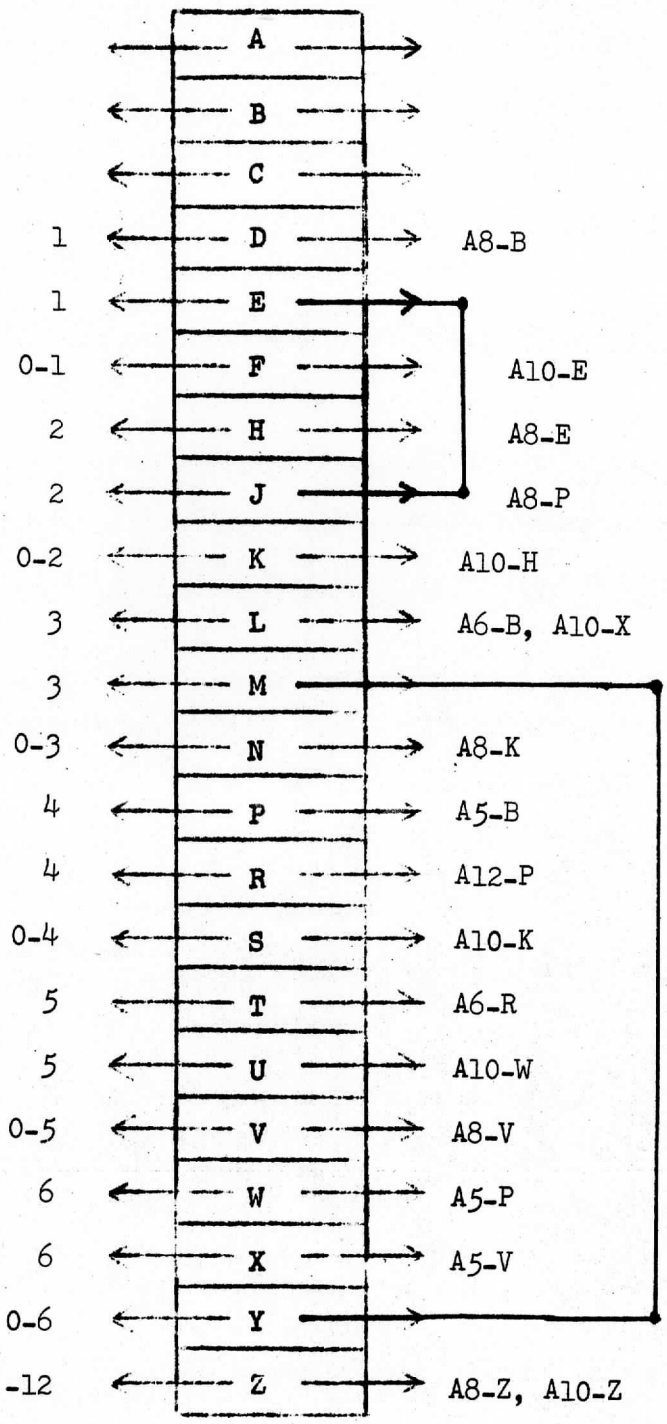
CARD TYPE 026 CARD NO. A-7



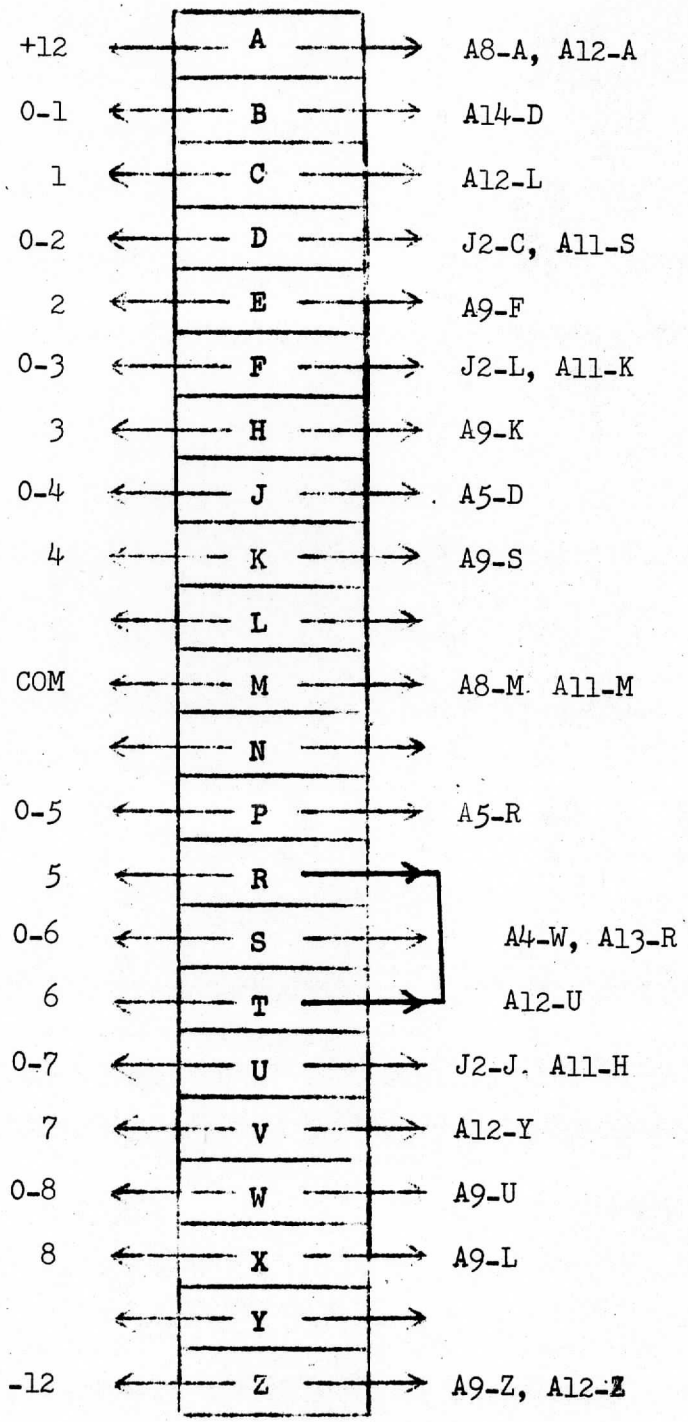
CARD TYPE N26 CARD NO. A8



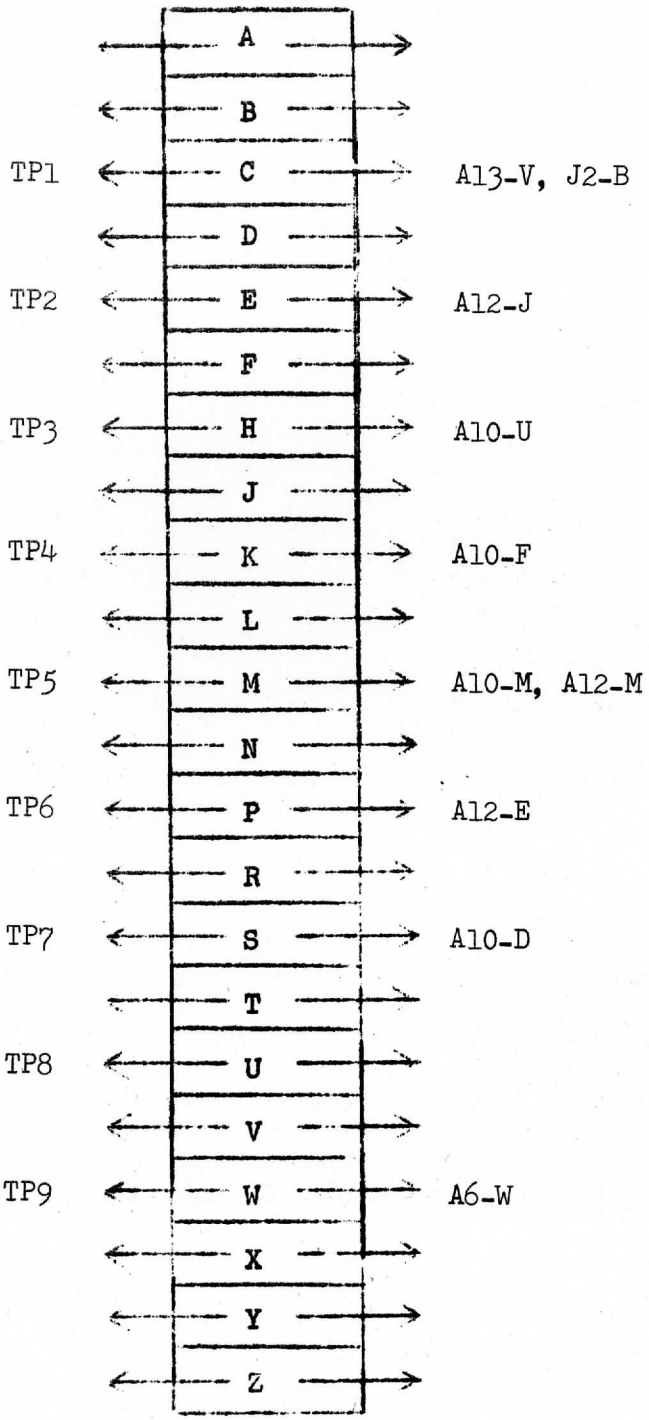
CARD TYPE A26 CARD NO. A9



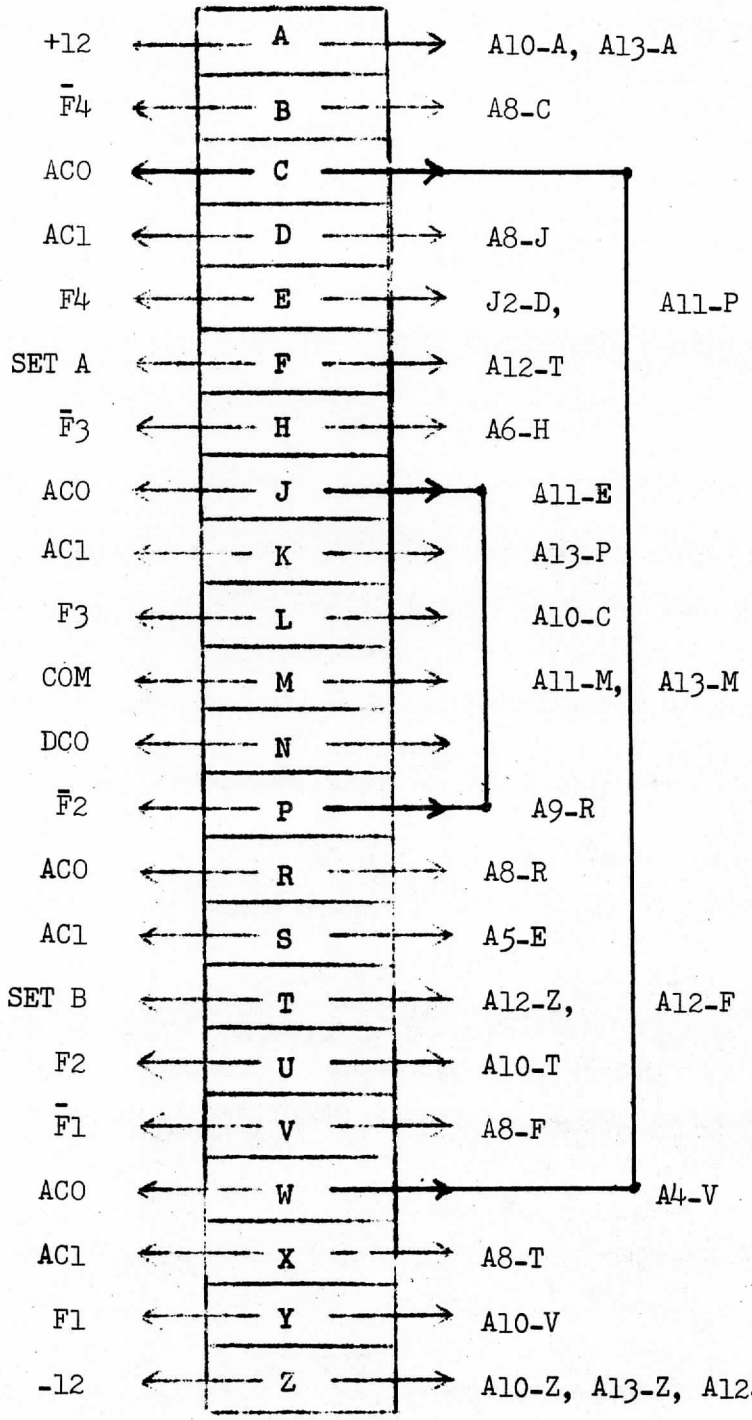
CARD TYPE 8-SA CARD NO. A10



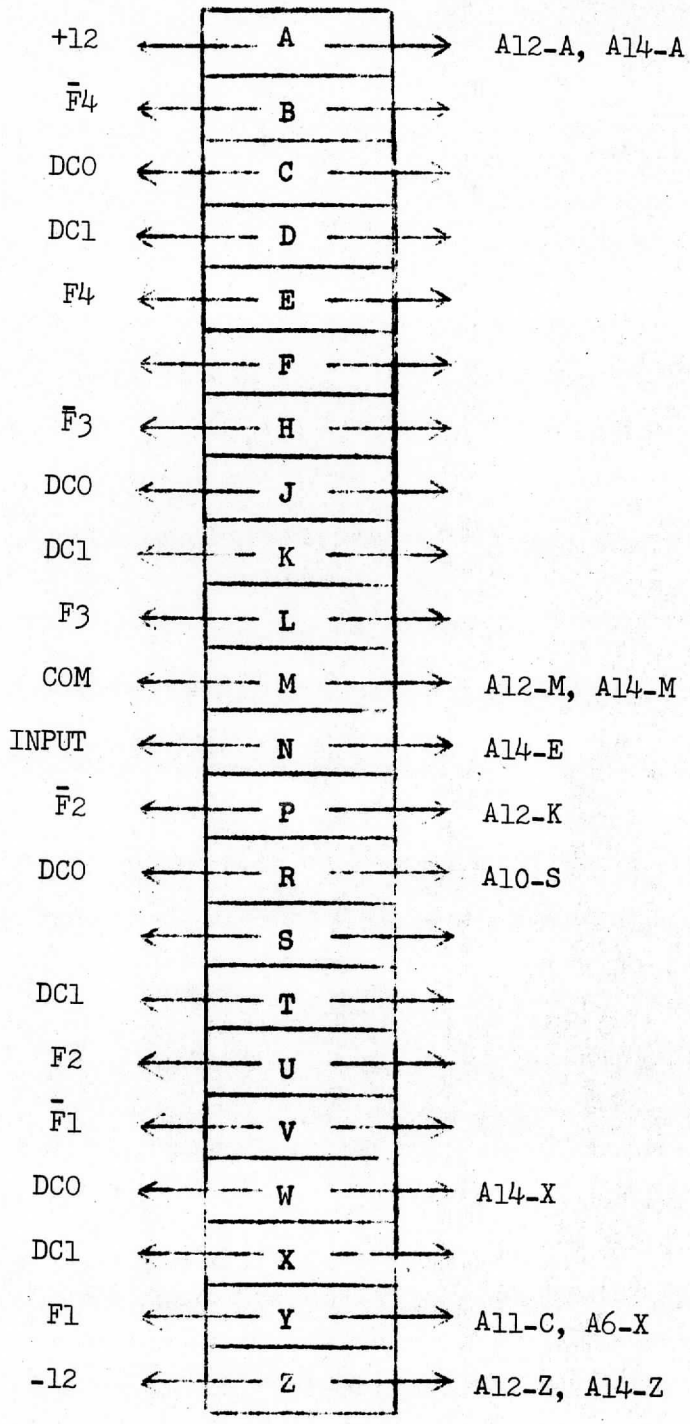
CARD TYPE TPC **CARD NO.** A11



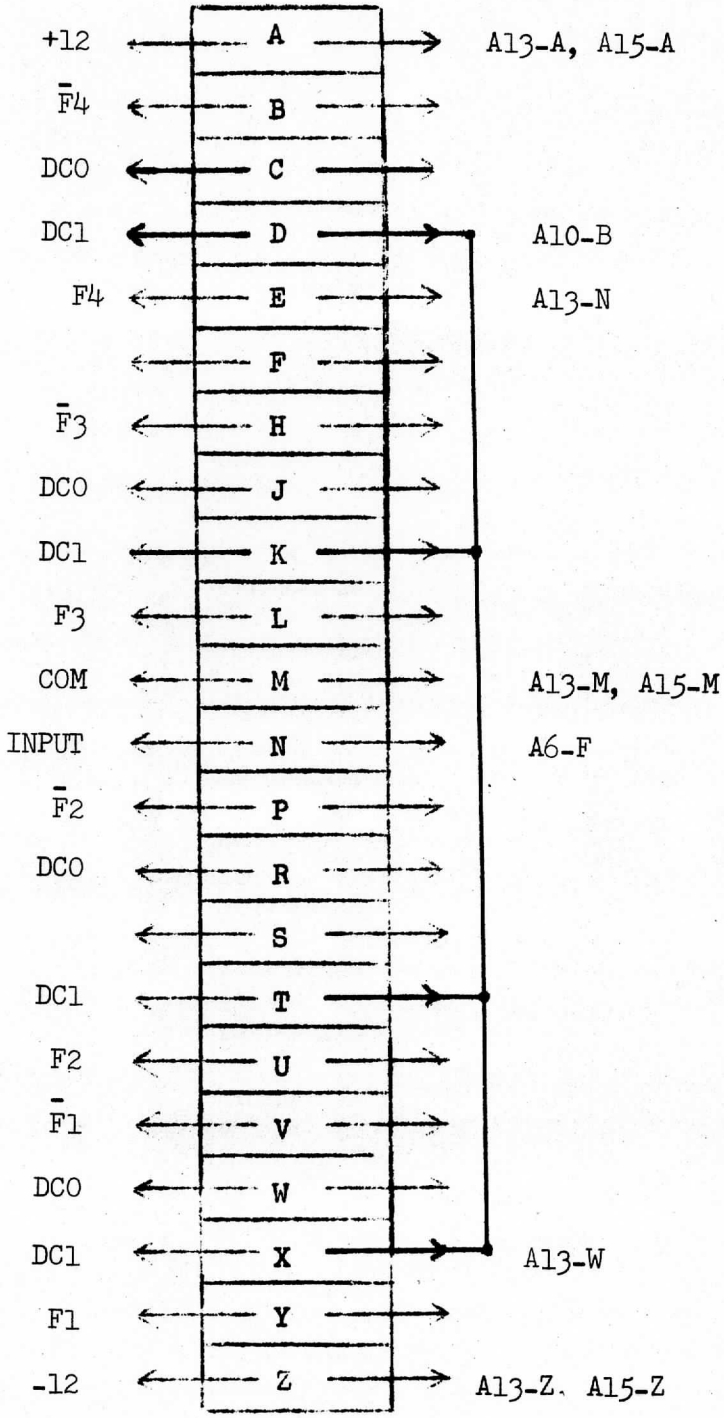
CARD TYPE 4XG CARD NO. A12



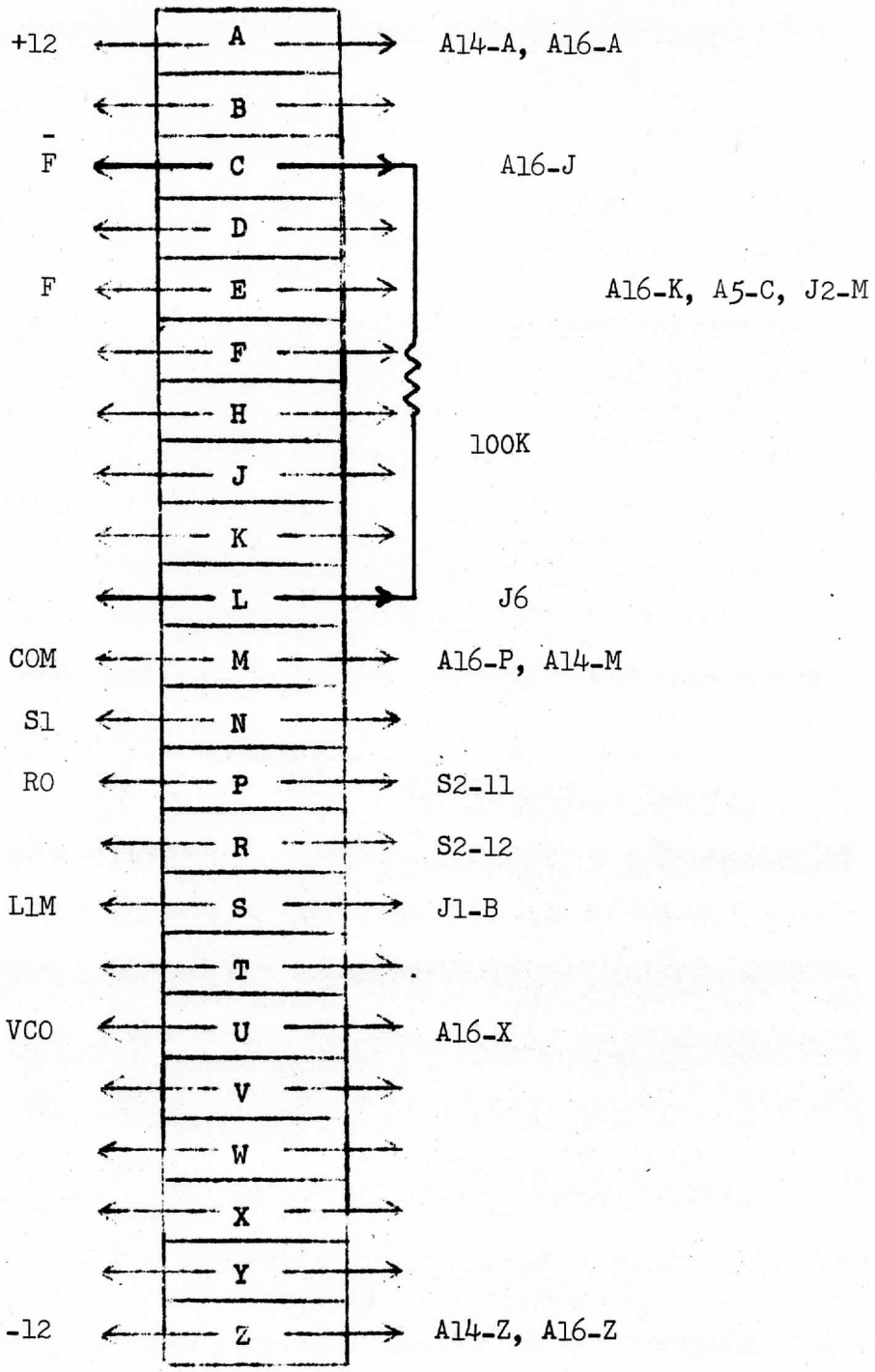
CARD TYPE 4XH CARD NO. A13



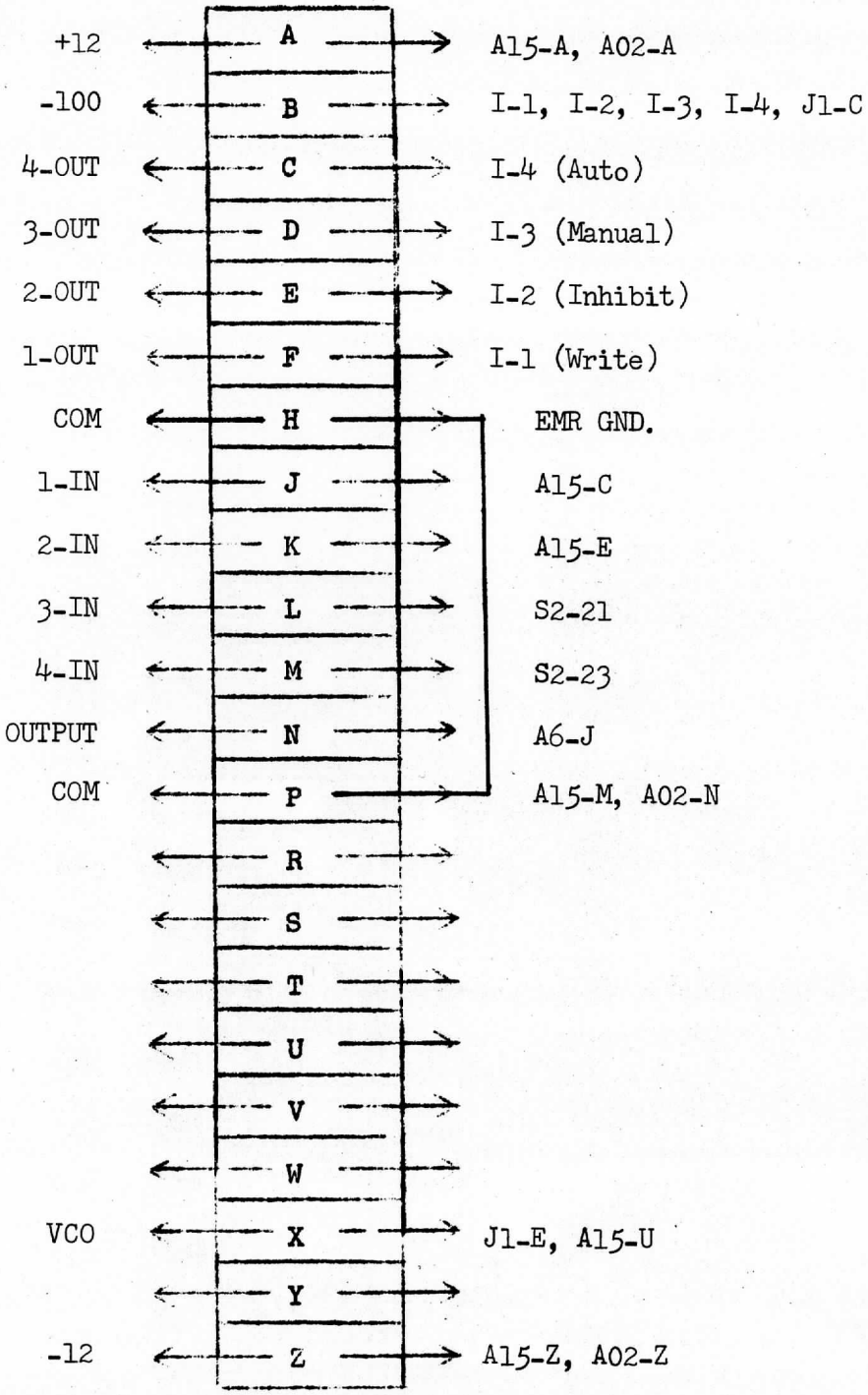
CARD TYPE 4XH CARD NO. A14



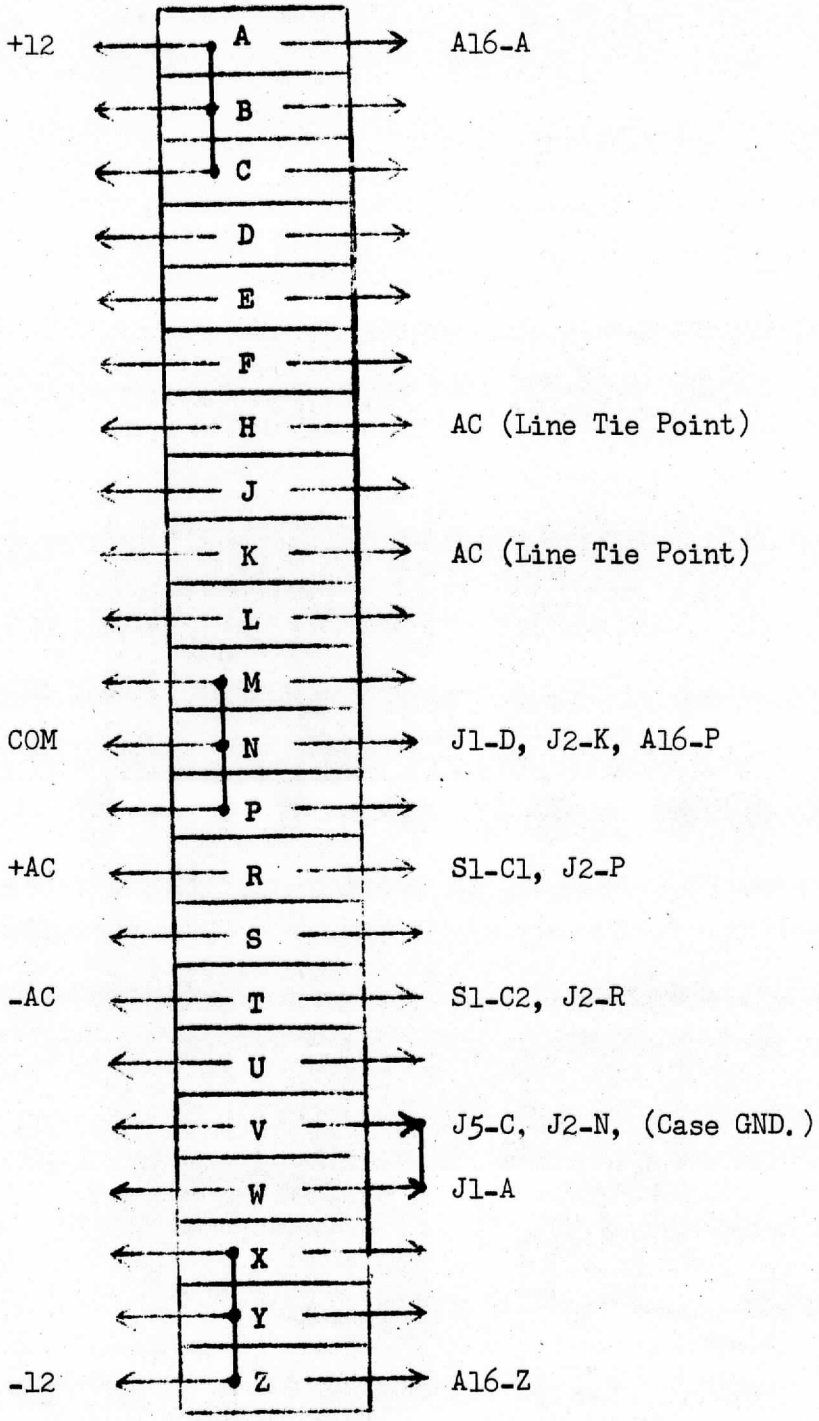
CARD TYPE SCD **CARD NO.** A15



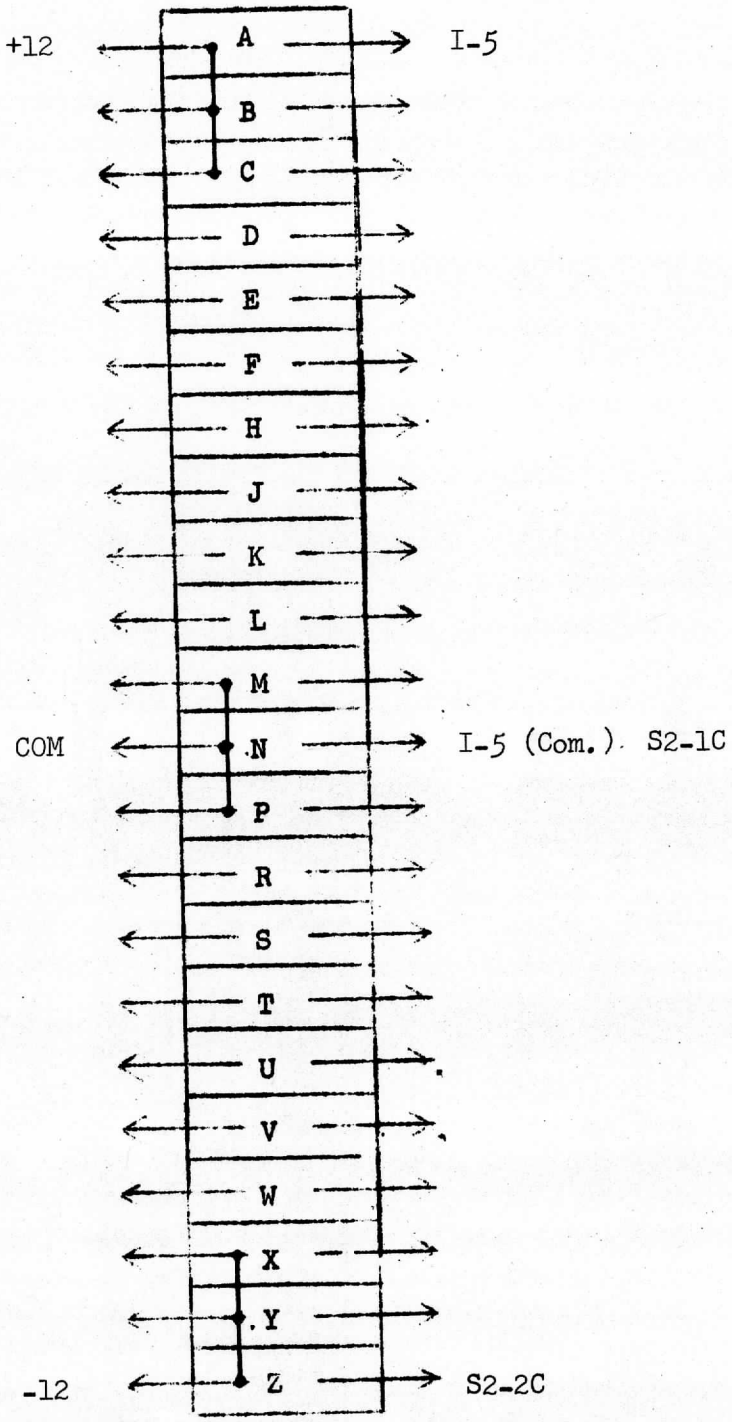
CARD TYPE ZLD **CARD NO.** A16



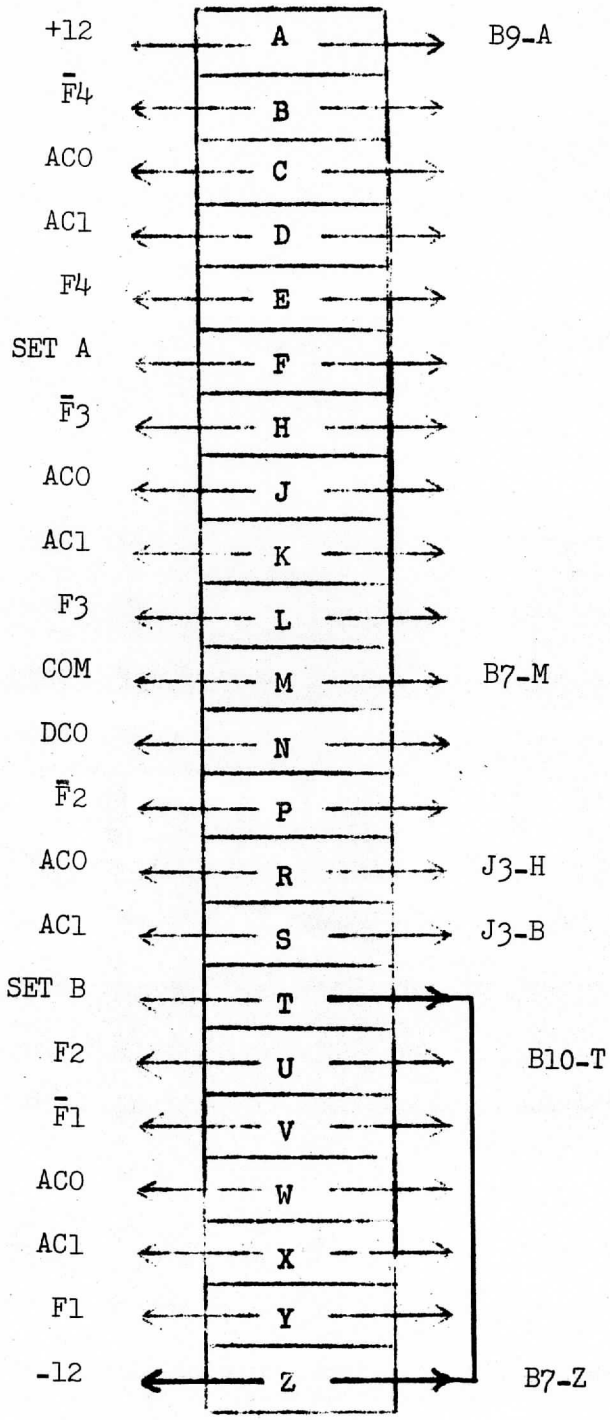
CARD TYPE Power Supply (+) **CARD NO.** A02



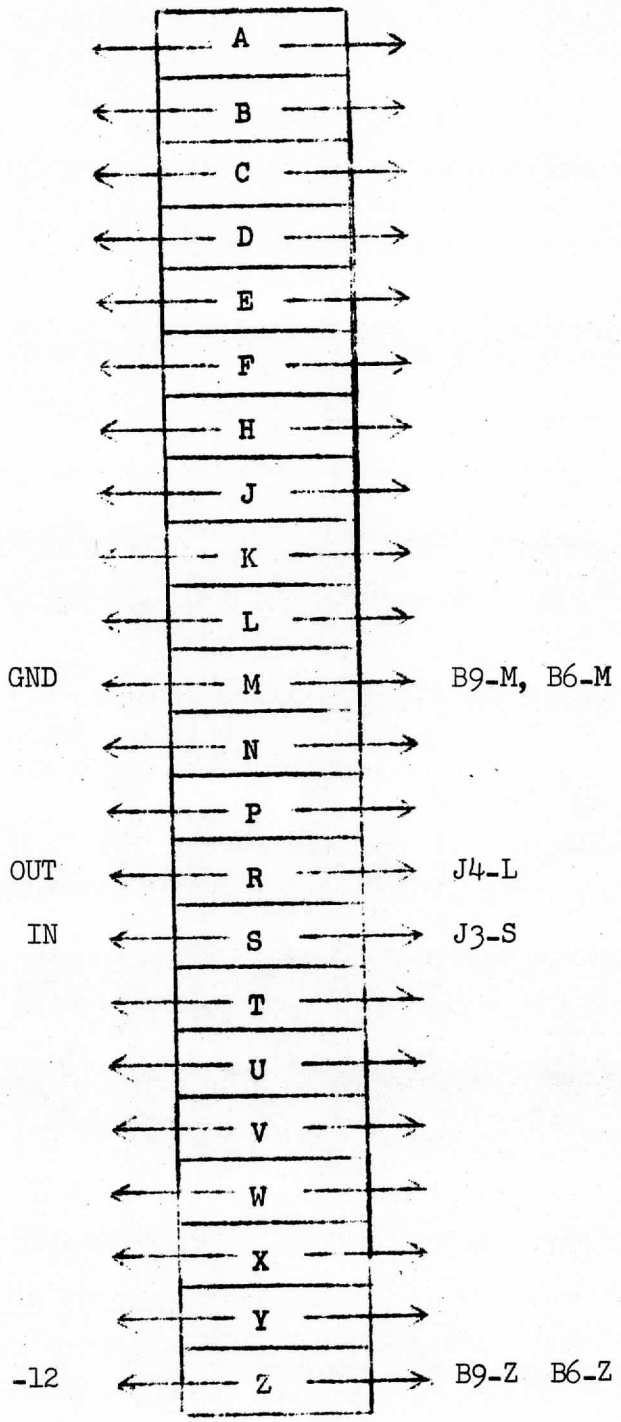
CARD TYPE Power Supply (-) **CARD NO.** A01



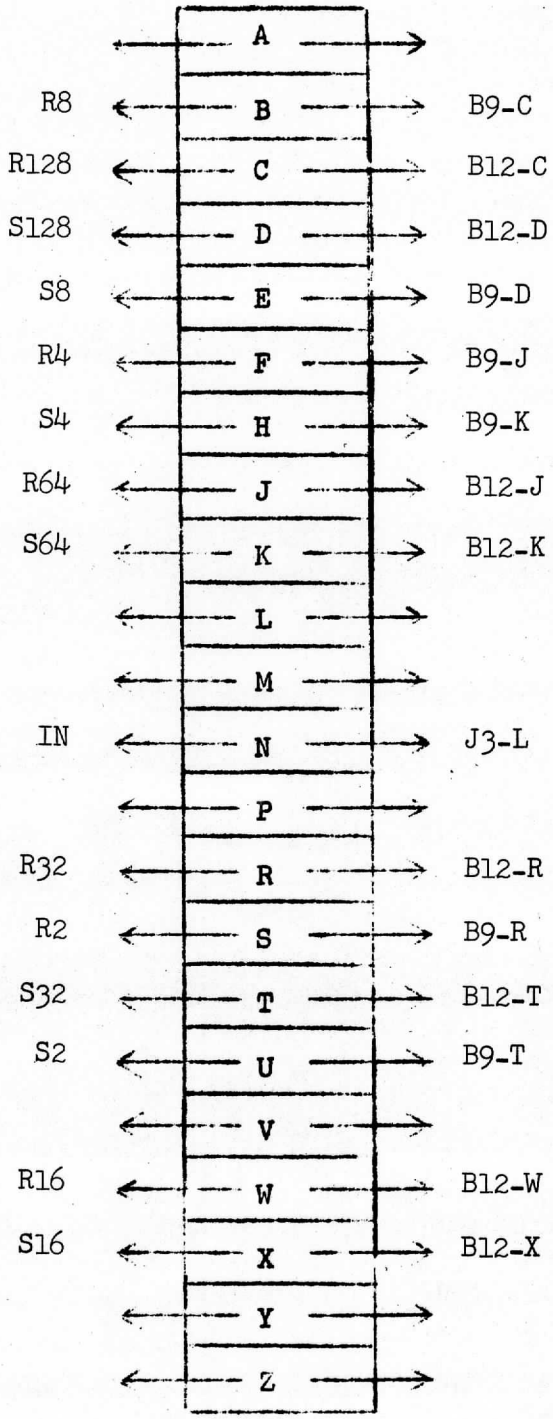
CARD TYPE 4XG CARD NO. B6



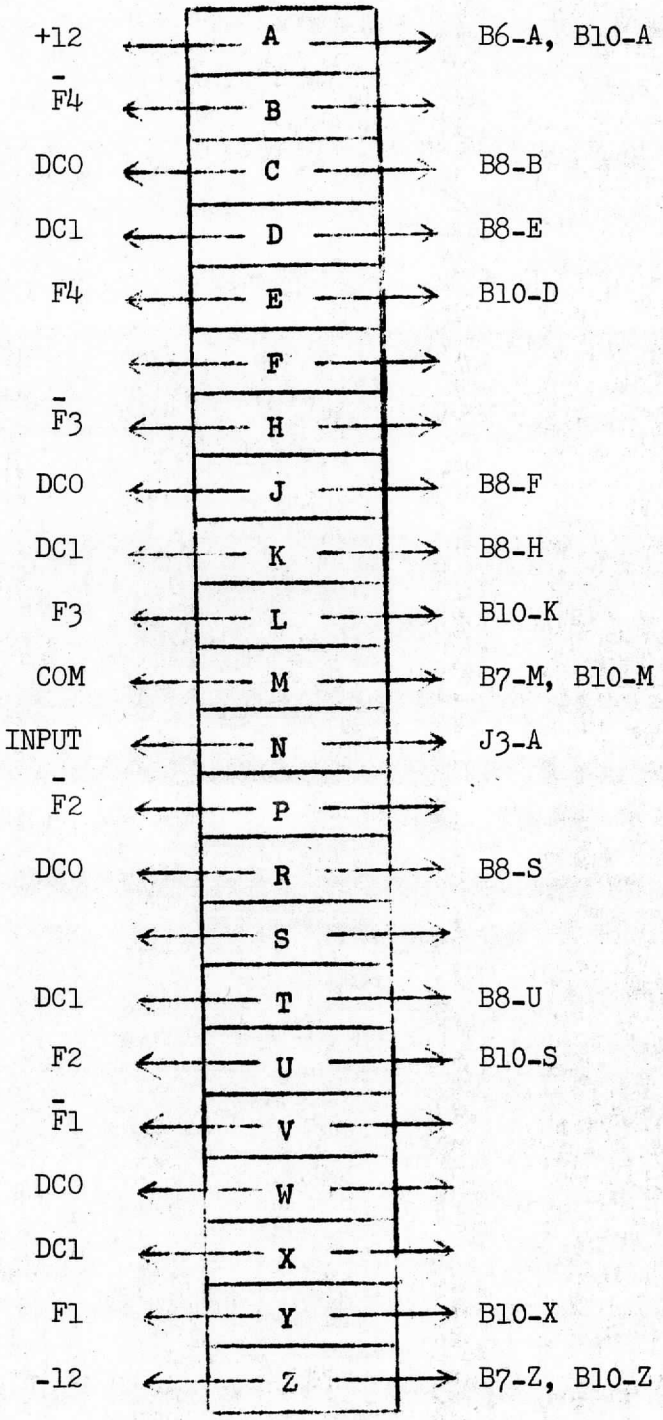
CARD TYPE MNO CARD NO. B7



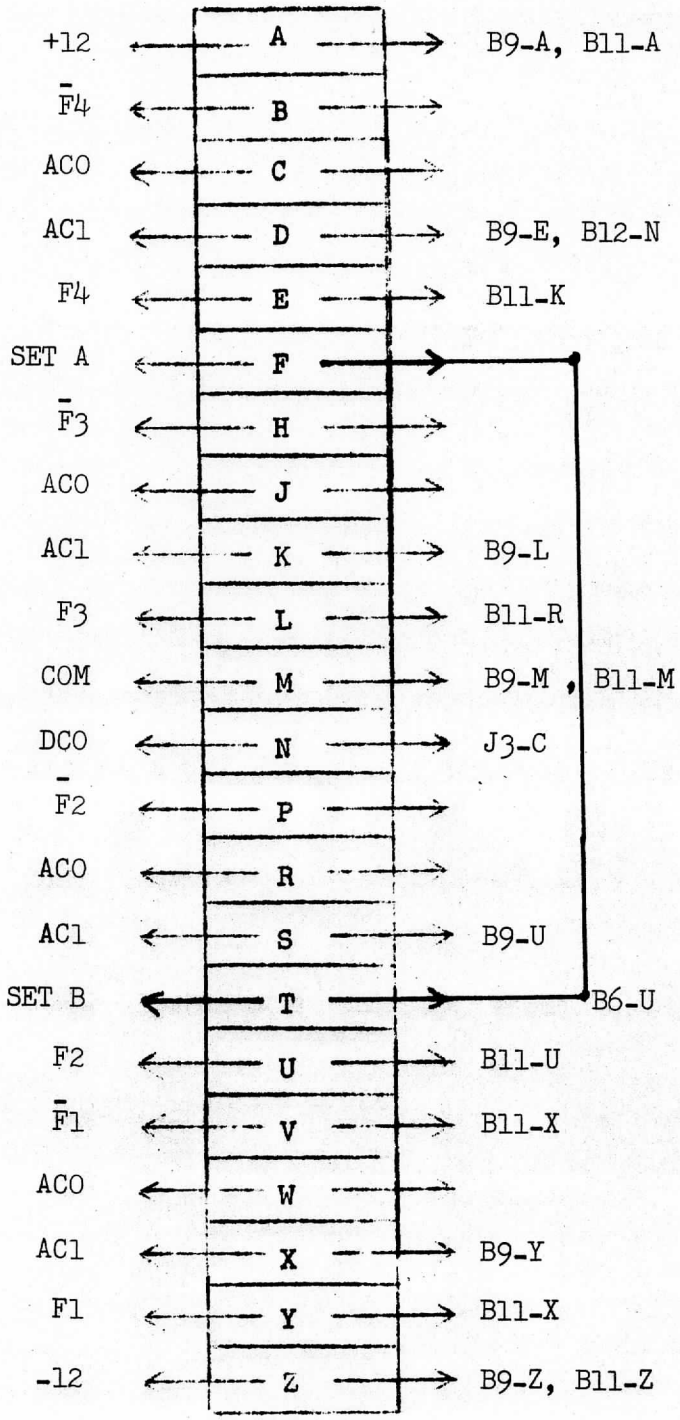
CARD TYPE PRS CARD NO. B8



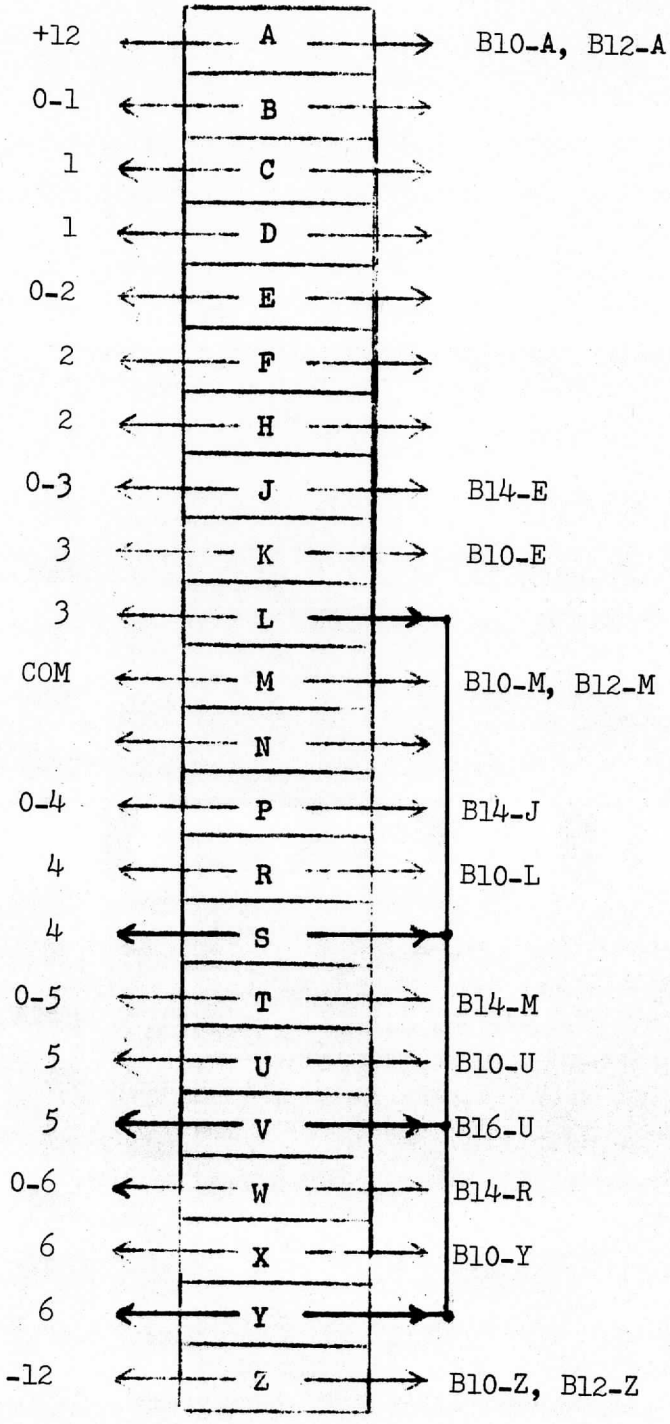
CARD TYPE 4XH CARD NO. B9



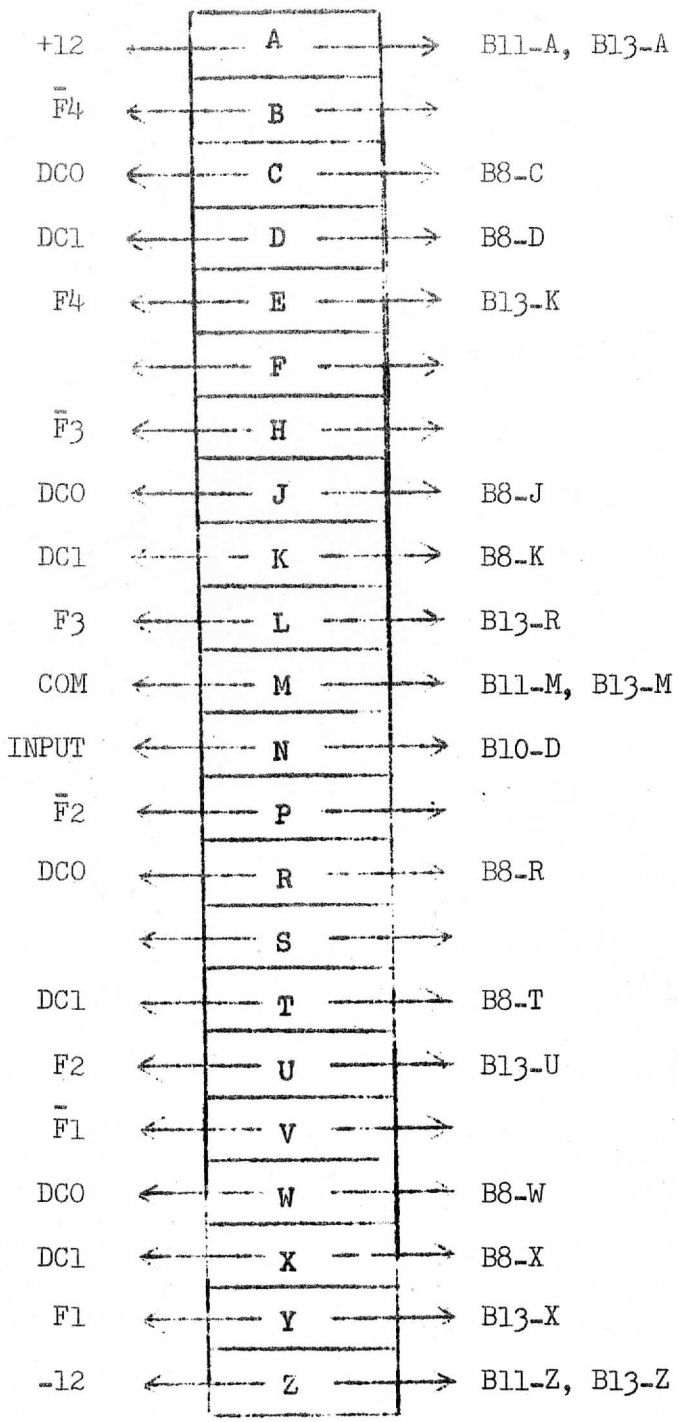
CARD TYPE 4XG CARD NO. B10



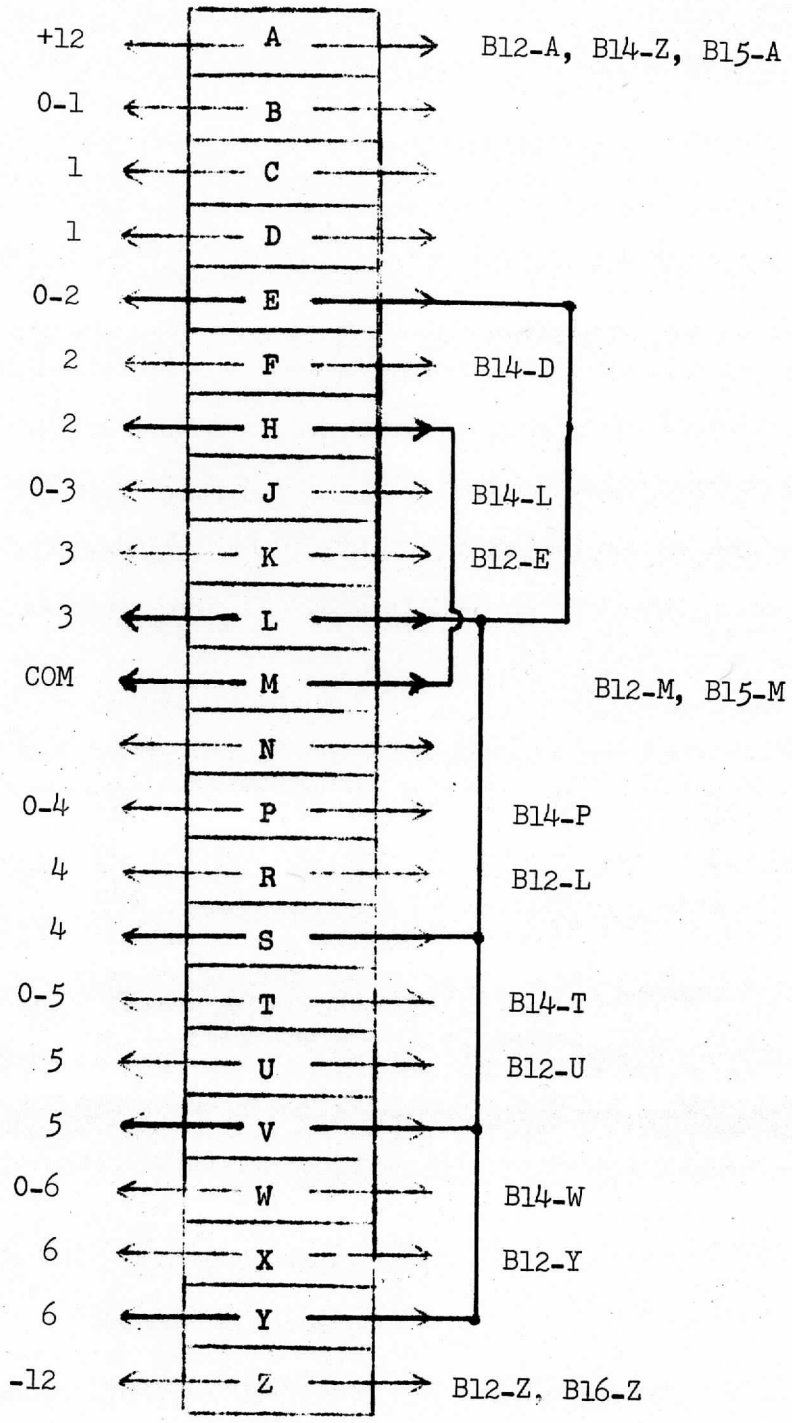
CARD TYPE N26 **CARD NO.** B11



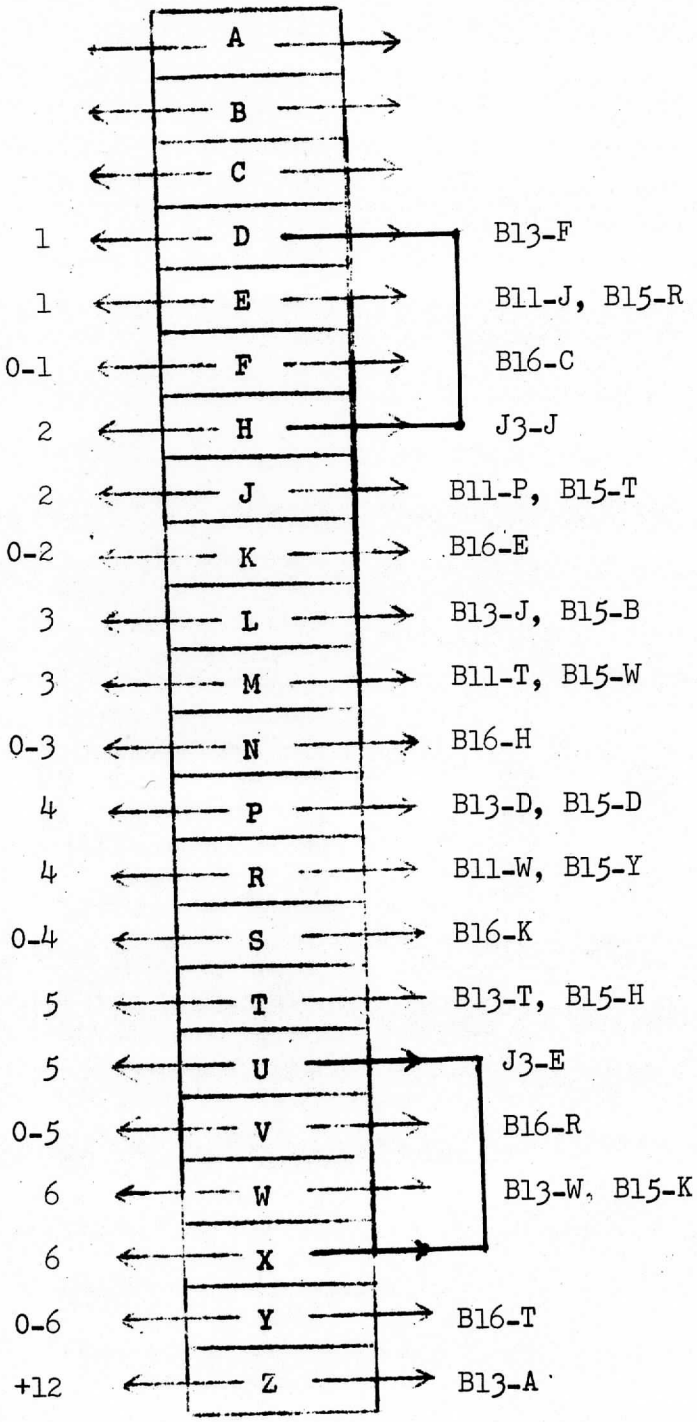
CARD TYPE 4XH CARD NO. B12



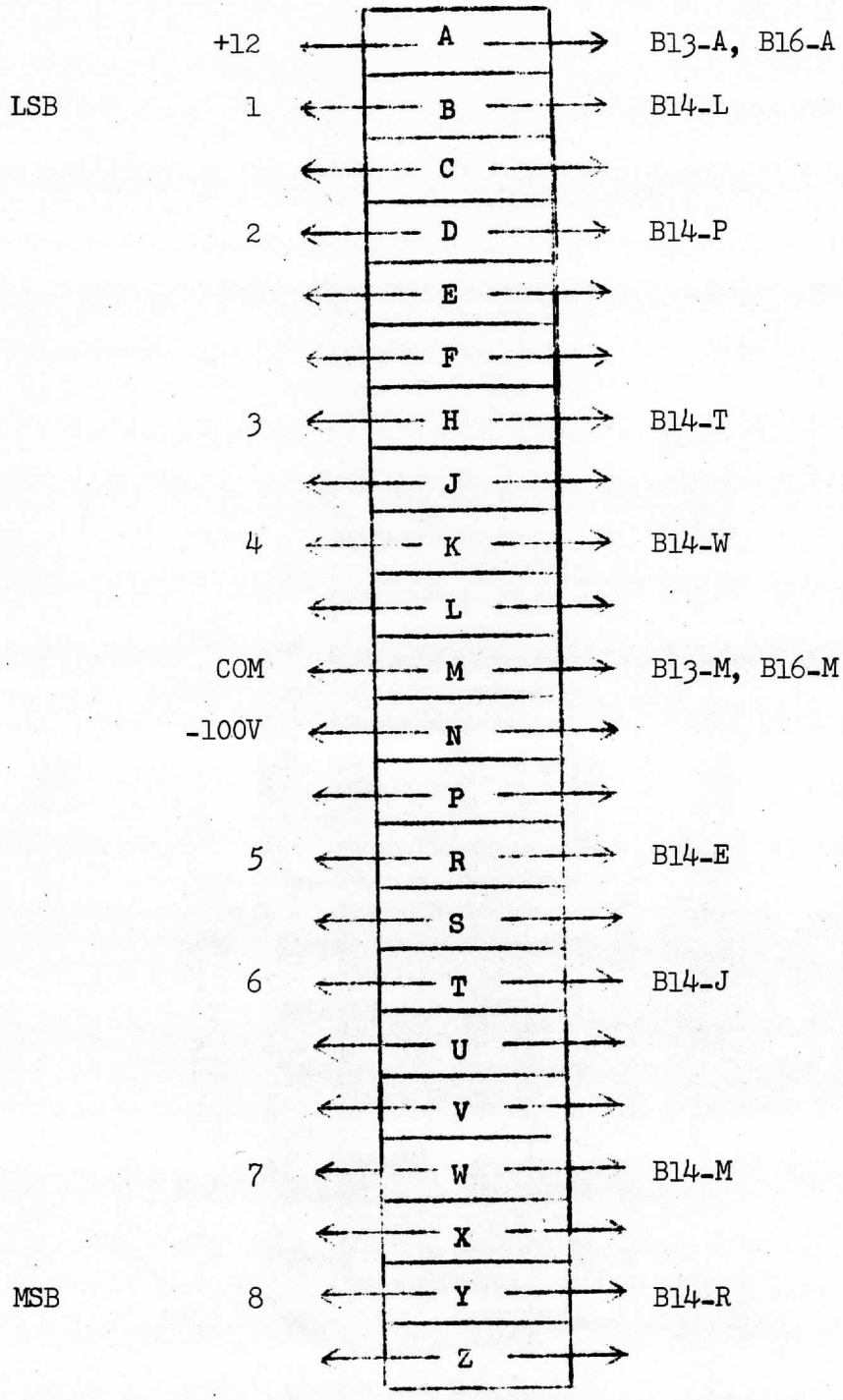
CARD TYPE N26 CARD NO. B13



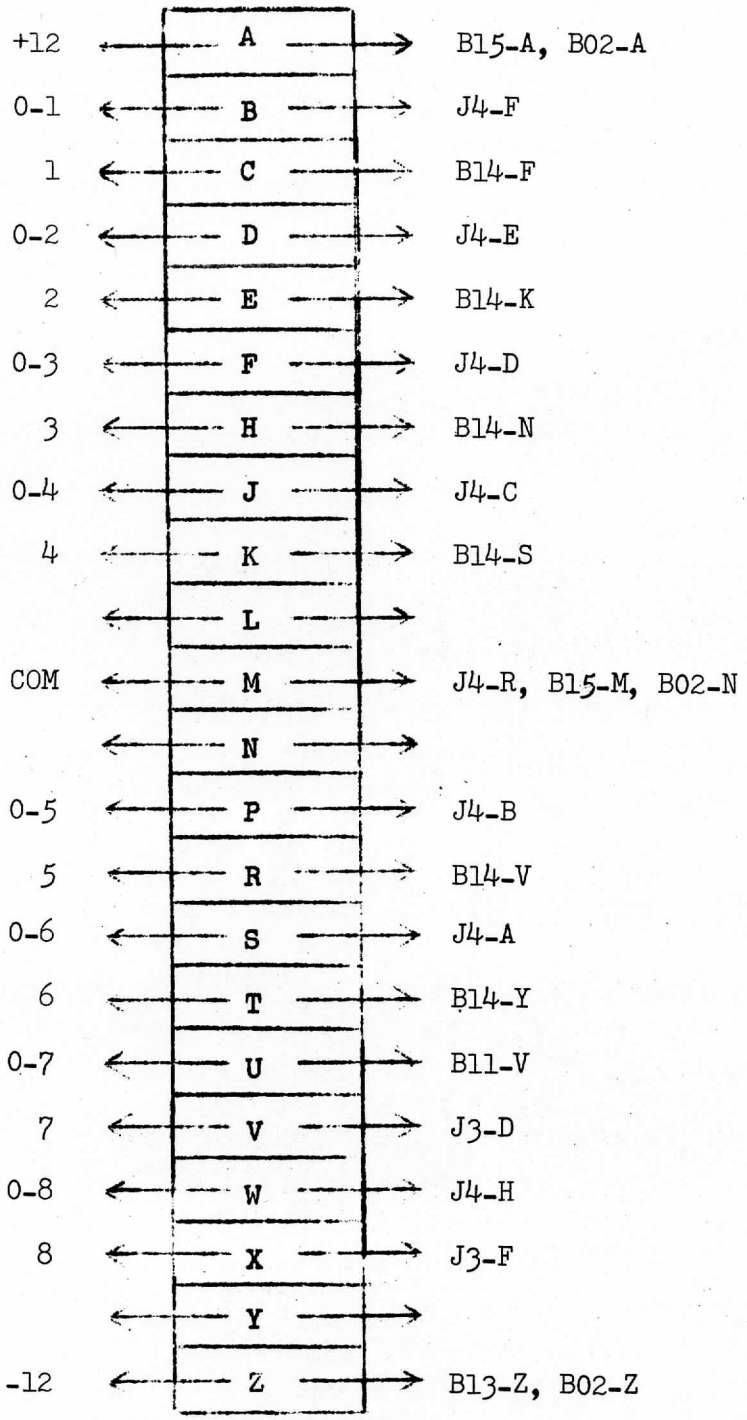
CARD TYPE 0-26 CARD NO. B14



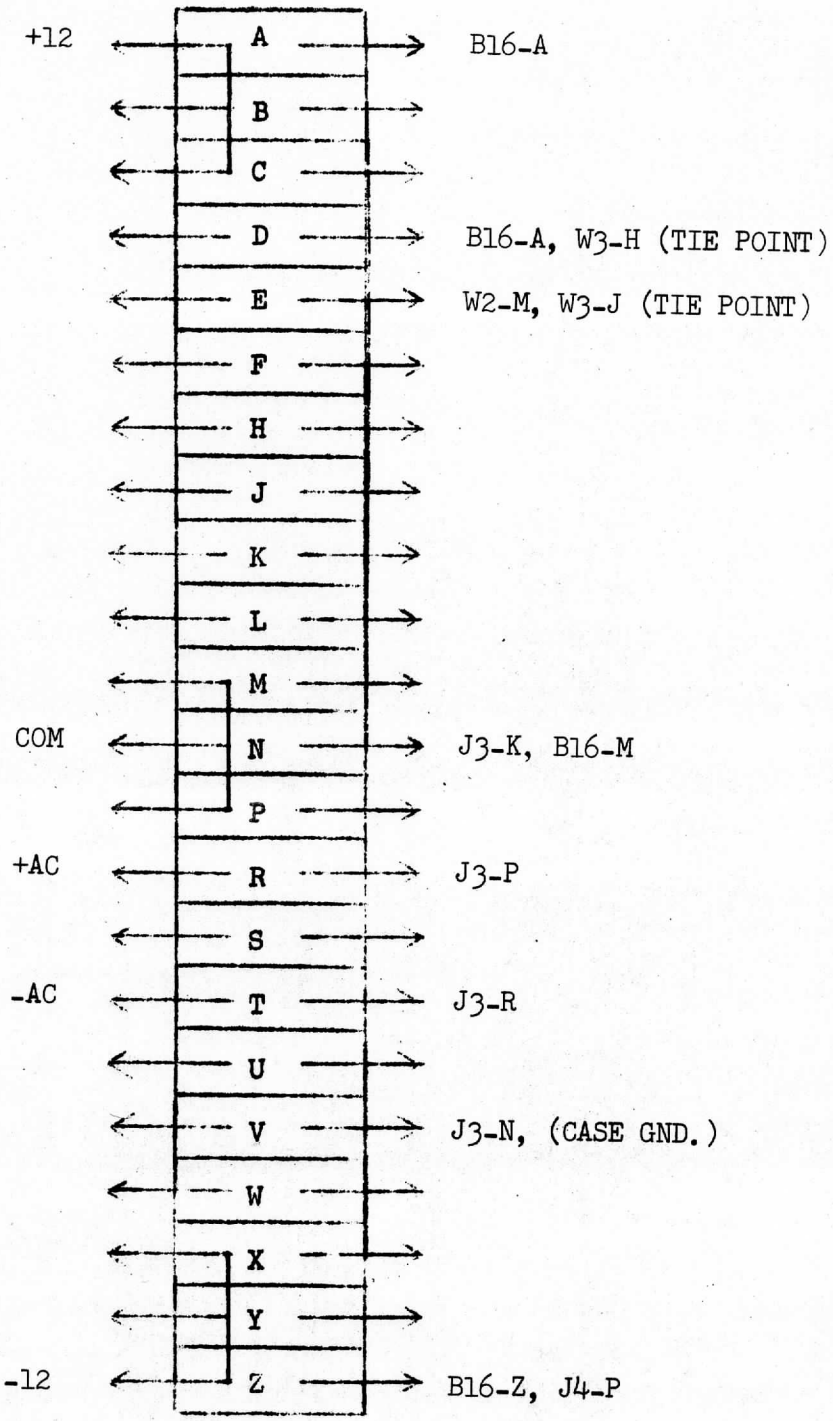
CARD TYPE NI-8 CARD NO. B15



CARD TYPE 8-SA **CARD NO.** B16



CARD TYPE Power Supply (+) **CARD NO.** B02



CARD TYPE Power Supply CARD NO. B01