Color Data Processor

— Technical Manual

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COLOR DATA PROCESSOR

TECHNICAL MANUAL

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FIGURES AND TABLES

1.0 EQUIPMENT DESCRIPTION

1.1 PURPOSE

The Color Data Processor formats and combines video, digital data-logging information, and timing signals, supplied from the ATS-3 MSSCC Experiment Ground Equipment, for analog recording by the Ampex SK-1600B Video Weather Data Accumulator. In addition, the Processor supplies two control signals required for proper speed and phasing of the SK-1600B transport.

1.2 FUNCTIONAL DESCRIPTION

1.21 Channel Video Outputs

The Color Data Processor supplies three video output channels to the record electronics input of the SK-1600B recorder. These outputs are a linear sum of 1) input video data, 2) two low-level reference frequency sinusoids, and 3) a two-level code (NRZ) containing line signature data.

In normal MSSCC camera operation, where the camera is stepped once per scan, the green, red, and blue camera signals appear at the channel A, B, and C outputs, respectively, and are recorded simultaneously. In either three sweep per line or ATS-B operation, the Photofax Analog video is supplied to Channel A, and only that channel is recorded. The video input to Channel A is automatically selected on the basis of the telemetry data inputs indicating which spacecraft camera is being operated (B or C) and the number of sweeps per line (1 or 3). A front

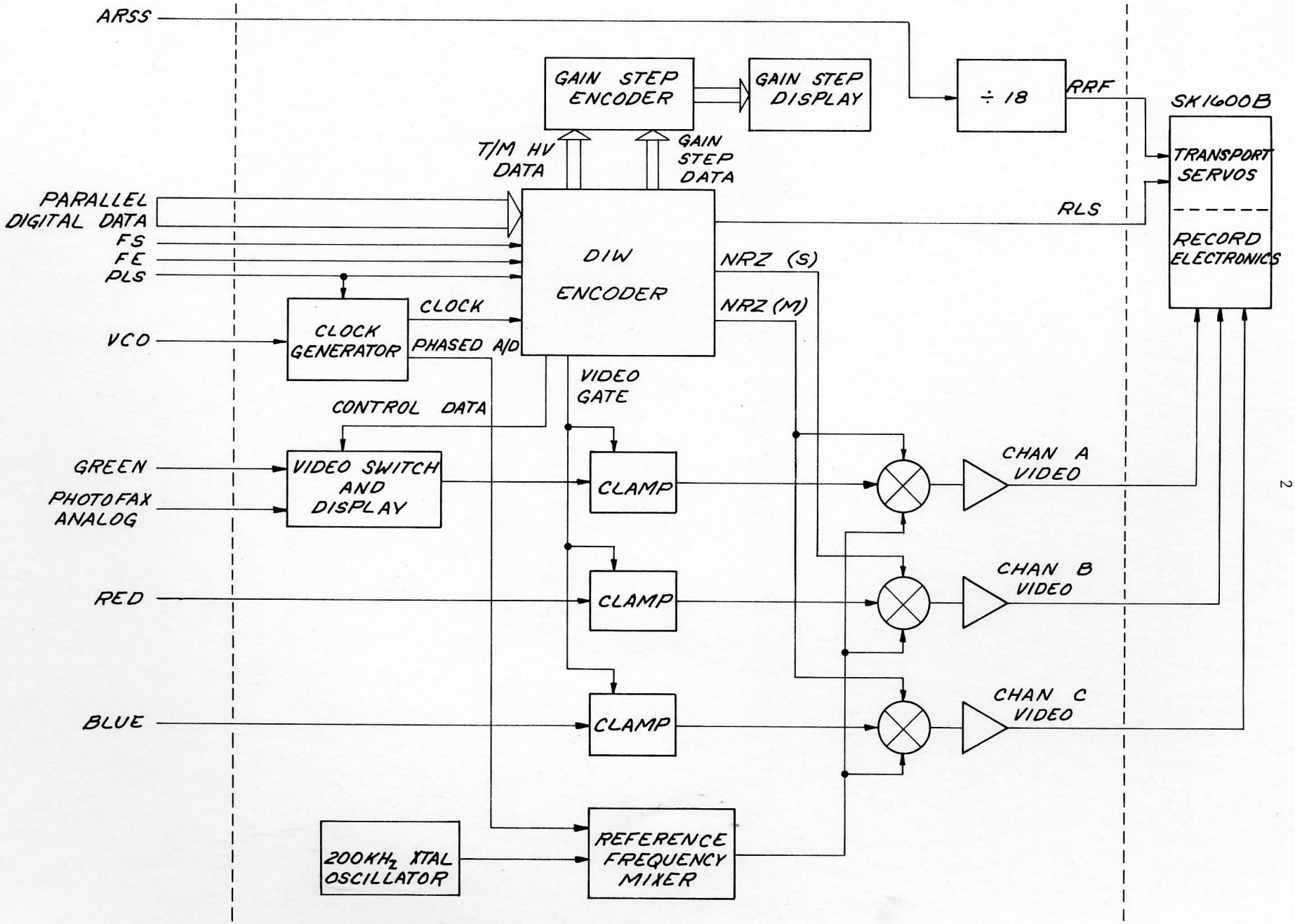


FIG. 1-1 COLOR DATA PROCESSOR FUNCTIONAL BLOCK DIAGRAM

panel toggle switch allows manual override of the automatic selection, and indicator lamps display which channel a video input is in use. Nominal video levels for all channel outputs are 0 to +1.5 v. peak.

1.22 Data Reference Frequencies

Two reference frequencies, appearing as 70 mv. peak-to-peak sinusoids, are always present in the three channel video outputs: a fixed 200 kHz. tape speed reference frequency and the A/D sampling frequency (245.76 kHz. at 100 rpm spin rate). Data are recorded at a tape speed which is proportional to the spacecraft spin rate. When reproduced at a fixed speed, the scan duration and A/D frequency are constants, and the tasks of photographic display or conversion to digital records are therefore simplified. The A/D reference frequency permits data to be positioned or sampled with a high degree of accuracy and repeatability. Since the SK-1600B utilizes a wideband FM record/reproduce system, the DC level and amplitude of the reproduced data depends on the recording speed. The 200 kHz. tape speed reference frequency supplies the recording speed information so proper compensation for gain and DC level change in the reproduced data may be made.

1.23 Data Identification Word

A 96-bit Data Identification Word (DIW) is generated in the 96 Picture Element intervals before the occurrence of the Blue Line Start pulse. Telemetry inputs supplying time and experiment status information are encoded into a serial, two-level (binary) code

analogous to the NRZ codings used in digital recording. The levels appearing on the channel outputs are nominally 0 and +1 v. and the video inputs are clamped to zero volts while the DIW is generated. NRZ(M) coding (where a data "1" is represented by a transition between levels and a data "0" by no transition) is supplied to Channels A and C, and NRZ(S) coding [opposite of NRZ(M)] is supplied to Channel B. The data contained in the DIW are listed in Table 1-1.

A 50 microsecond Data Line Start pulse is generated 32 Picture Element pulses before the start of the DIW.

1.24 Gain Step Encoder

The Gain Step Encoder supplies six binary data outputs to the DIW Encoder (two per color channel) indicating the nominal high voltage outputs, or Gain Steps, of each MSSCC camera photomultiplier supply. An additional one-of-four line output for each color drives front panel indicator lamps, which are used to confirm that the Gain Step data encoded in the DIW is correct.

1.25 Recorder Control Outputs

A Recorder Line Start (RLS) output pulse is generated 64 Picture Element pulses after the occurrence of the Pre-line Start pulse. The RLS turns on the SK-1600B record electronics and provides a phasing reference for the rotating scanning drum.

The Recorder Reference Frequency (RRF) supplies 2^{13} pulses for each RLS pulse. The rotation of the SK-1600B drum and capstans is accurately controlled by servos which maintain phase lock between the outputs of 2^{12} bit optical encoders, on the drum and capstan shafts,

and the RRF. The drum will advance through exactly four revolutions for each 2^{13} RRF pulses received, so once the initial phasing of the drum position with the RLS has been established, no further phase corrections are required.

1.26 Data and Control Signal Timing

The time duration and sequence of control signals and data is shown in Figure 1-2. All system timing is derived from the PLS and VCO inputs to the Color Data Processor, and time events on the figure are therefore given in terms of Picture Element intervals, measured from the occurrence of the Green Line Start pulse.

1.3 PHYSICAL DESCRIPTION

The Color Data Processor consists of two separate rack mounting units, designated Color Data Processor and Processor Power Supply. Physical dimensions of each unit, excluding front and rear panel projections, are:

Processor: 19 in. w. x 5 1/4 in. h. x 18.5 in. d.

Power Supply: 19 in. w. x 8 3/4 in. h. x 5 1/4 in. d.

The Processor unit is mounted upon chassis slides for convenient access to circuit modules for test or adjustment. Processor circuitry is built on 4 1/2 in. x 3 1/4 in. glass-epoxy module cards, which mate with standard configuration 44-pin connectors. Modules are contained in two 28-slot card files which occupy the center and rear locations of the card drawer.

All inter-unit and external interfacing connections are made at the rear connector panels of both units.

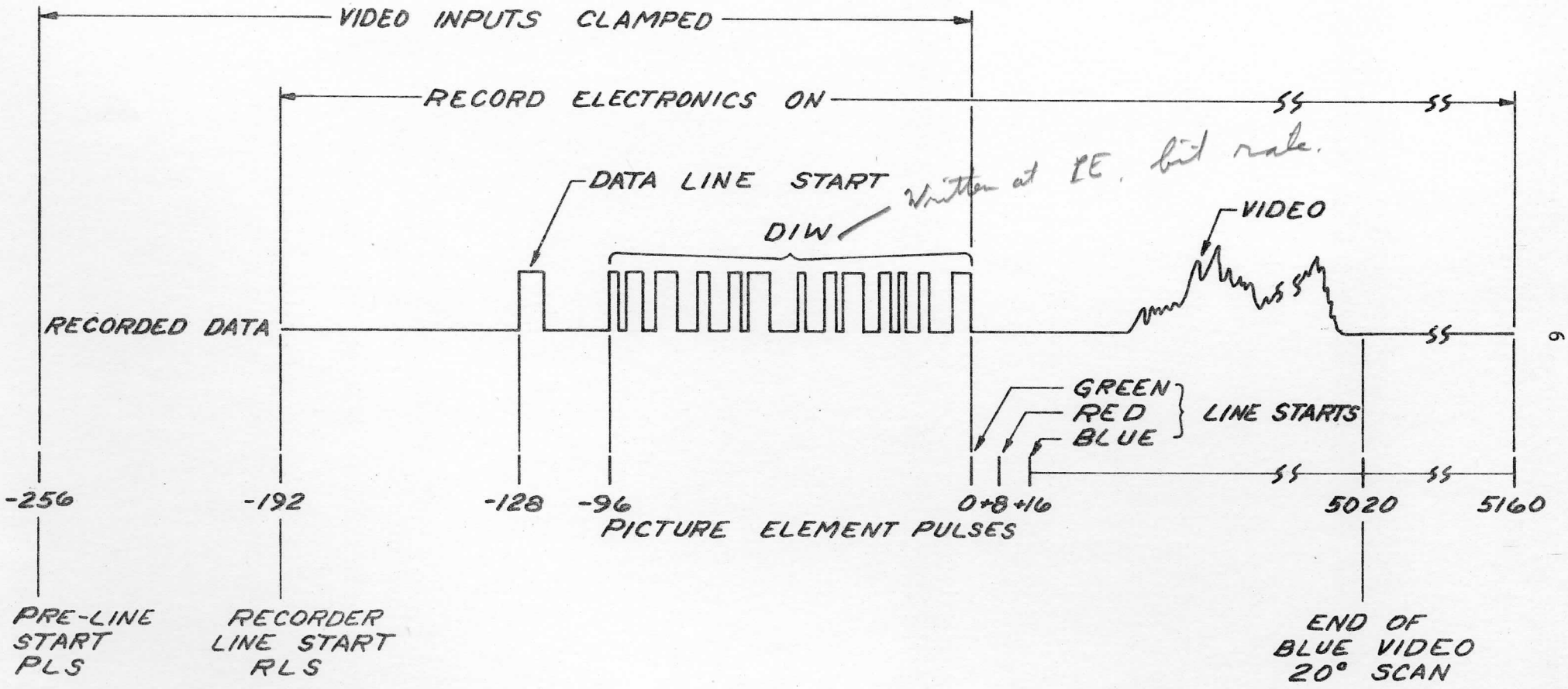


FIG. 1-2 DATA TIMING DIAGRAM

1.4 ELECTRICAL SPECIFICATIONS

Video Input Impedance: 75Ω

Video Input Level: 0 to 0.5 v. (minimum)

Video Frequency Response: DC to 200 kHz. (3 db point)

Maximum Video Gain: 3

Channel Output Impedance: 75Ω

Channel Output Level: 0 to 3 v. (maximum)

Logic Input Impedance: 75Ω (minimum)

Logic Levels and Drive Capabilities: See Wyle Specification Sheets, Section 4

Power: 115 v., 60 Hz., 1 Phase, 0.5 amp.

1.5 EQUIPMENT SUPPLIED

Color Data Processor and Power Supply with line cord and interconnection cable;

Data Input Simulator (T/M High Voltage);

Technical Manual (2 copies);

Spare Circuit Modules, one each of following:

Wyle	SSEC
MDS-4	Video Amplifier 1306-3A
MPG-8	D/A Converter, 1306-1A
MNG-12	
MSR-8	
MCO-1	
MBD-1	
MOF-4	
MUF-5	
MEC-44 (Extender Module)	

Spare Components, one each except as noted:

Description	Manuf. and Ref. No.
Integrated Circuit, Comparator, μA710C	Fairchild U5B771039X
Integrated Circuit, Operational Amp.,LM201	National Semiconductor LM201
Transistor, 2N3644	Fairchild
Transistor, 2N3643	Fairchild
Transistor, 2N4222	Motorola
Lens,Cartridge Indicator Lamp, White	Sylvania 301460
Lens,Cartridge Indicator Lamp, Red	Sylvania 301470
Lens, Cartridge Indicator Lamp, Blue	Sylvania 301480
Lens, Cartridge Indicator Lamp, Green	Sylvania 301490
Lamp, Indicator, Type 328	Tung-Sol
Fuse, 1/2 amp., Slo-Blo (2 supplied)	Littelfuse 3AG 1/2 S

Data Identification Word Format

Bit Position	Data Code	Data Description
1	1	Marker Pattern
2	1	
3	1	
4	0	
5	1	
6	0	
7	0	
8	1	
9	1	
10	0	
11	1	
12	FS	Frame Start
13	FE	Frame End
14	SCOP	B or C Spacecraft; 0 = B, 1 = C
15	GCLR	Line Color - Green
16	RCLR	Line Color - Red
17	BCLR	Line Color - Blue
18	FIT4	Frame Indentifier Tens (BCD)
19	FIT2	
20	FIT1	
21	FIU8	Frame Identifier Units (BCD)
22	FIU4	
23	FIU2	
24	FIU1	
25	AVG4	Channel A (Green or ATS-B) Video Gain DB/2 (BCD)
26	AVG2	
27	AVG1	
28	BVG4	Channel B (Red) Video Gain DB/2 (BCD)
29	BVG2	
30	BVG1	
31	CGV4	Channel C (Blue) Video Gain DB/2 (BCD)
32	CVG2	
33	CVG1	
34	0	
35	MVC2	Thousands Vertical Line Count (BCD)
36	MVC1	
37	CVC8	Hundreds Vertical Line Count (BCD)
38	CVC4	
39	CVC2	
40	CVC1	
41	XVC8	Tens Vertical Line Count (BCD)
42	XVC4	
43	XVC2	
44	XVC1	
45	UVC8	Units Vertical Line Count (BCD)
46	UVC4	
47	UVC2	
48	UVC1	
49	0	
50	0	
51	XHR2	Tens Hours (BCD)

Table 1-1

Bit Position	Data Code	Data Description
52	XHR1	
53	UHR8	Units Hours (BCD)
54	UHR4	
55	UHR2	
56	UHR1	
57	SVGN	Satellite Video Gain, ATS-B; 0 - Normal, 1 = High
58	XMN4	Tens Minutes (BCD)
59	XMN2	
60	XMN1	
61	UMN8	Units Minutes (BCD)
62	UMN4	
63	UMN2	
64	UMN1	
65	SWPL	Sweeps per line; 0 = 1 swp/in, 1 = 3 swp/in
66	XSC4	Tens Seconds (BCD)
67	XSC2	
68	XSC1	
69	USC8	Units Seconds (BCD)
70	USC4	
71	USC2	
72	USC1	
73	SCDR	Scan Direction; 0 = N-S, 1 = S-N
74	MODE	Scan Mode; 0 = Back-to-back, 1 = Normal
75	AGS1	Gain Step, Green
76	AGS2	
77	BGS1	Gain Step, Red
78	BGS2	
79	CGS1	Gain Step, Blue
80	CGS2	
81	AHV5	T/M High Voltage, Green
82	AHV4	
83	AHV3	
84	AHV2	
85	AHV1	
86	BHV5	T/M High Voltage, Red
87	BHV4	
88	BHV3	
89	BHV2	
90	BHV1	
91	CHV5	T/M High Voltage, Blue
92	CHV4	
93	CHV3	
94	CHV2	
95	CHV1	
96	Parity	Zero Reset

2.0 PRINCIPLES OF OPERATION

2.1 DIW ENCODER (Figure 2-1)

The Data Identification Word Encoder generates the 96-bit NRZ(M) and NRZ(S) characters, each preceded by a Data Line Start pulse, as illustrated in Figure 1-2.

The Digital Clock supplies a two-phase clock signal at the Picture Element frequency to the encoder logic and an A/D frequency output to the Reference Frequency Mixer. These outputs are derived from the VCO input from the Synchronizer and are initially phased by the Pre-line Start (PLS) input pulse.

Gating and control signals determining operating sequence are obtained from the outputs of an 8-bit (256 state) Control Counter. A single counting sequence is begun with the arrival of each PLS input pulse.

Parallel digital data inputs are scanned, eight bits at a time, by binary decoder outputs and transferred to shift register parallel data inputs. A new group of 8 data bits is scanned every 8 Picture Element pulses.

Data groups are alternately loaded into and shifted from dual 8-bit shift registers to the NRZ Generator input.

The NRZ generator translates the shift register output, in which data "ones" and "zeros" are represented by logic level "ones" and "zeros," to the NRZ(M) or NRZ(S) coding described above.

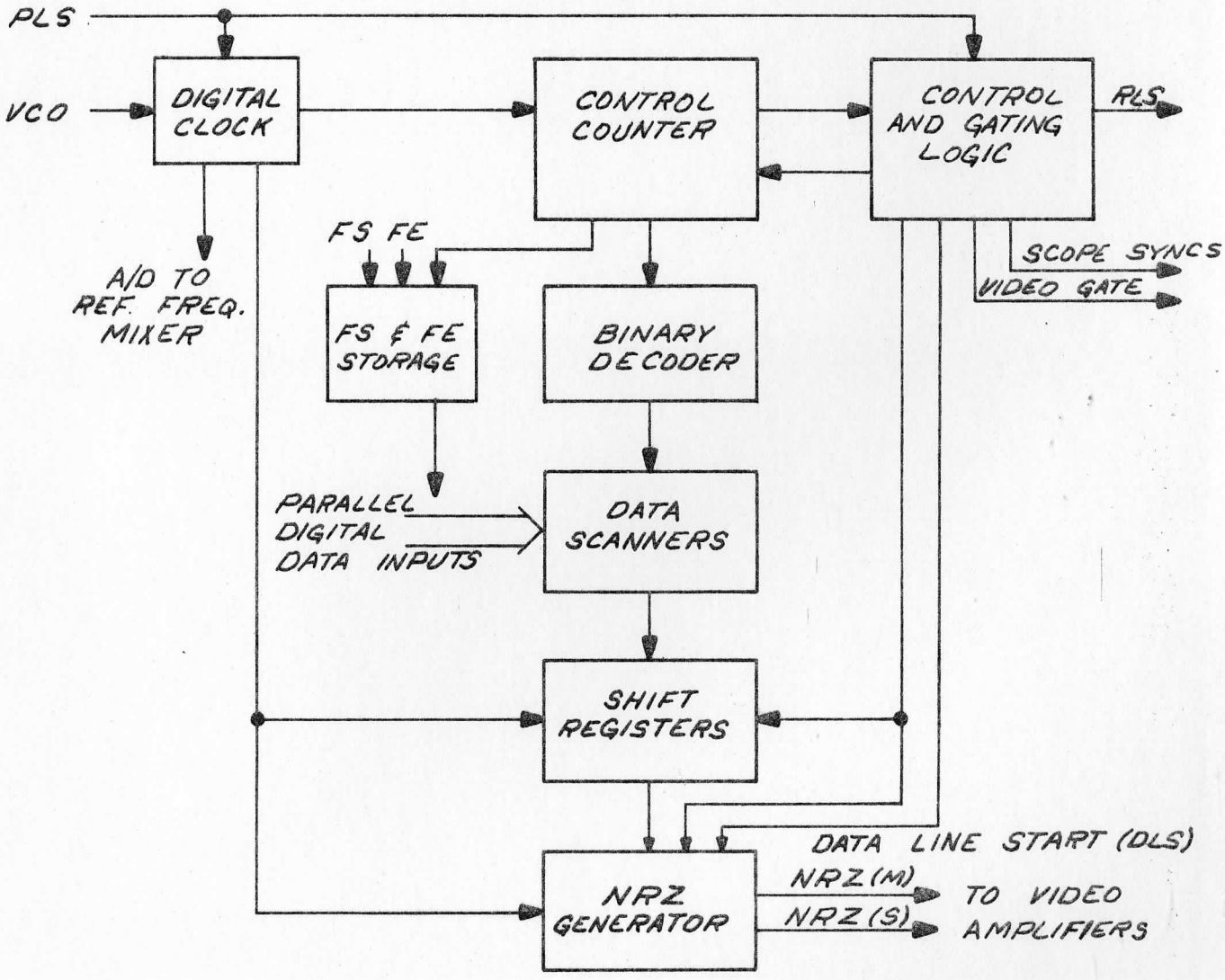


FIG. 2-1 DIW ENCODER BLOCK DIAGRAM

Frame Start and Frame End pulses are temporarily stored and appear as data "ones" in the next DIW character generated after their occurrence.

In addition to providing the control signals necessary for encoder operation, the Control and Gating Logic supplies 1) a Video Gate signal which actuates the video input clamping circuits, 2) three Sync outputs, which provide positive-going pulse one-half clock cycle before the occurence of the first, 33rd, and 65th data bits of the DIW character for convenience in monitoring the data content, 3) a Recorder Line Start pulse output, which turns on the SK-1600B record electronics and provides a phasing signal for the recorder scanning drum, and 4) the 50-microsecond Data Line Start pulse, which appears on both the NRZ(M) and NRZ(S) outputs.

2.2 GAIN STEP ENCODER

The Gain Step Encoder consists of three identical encoding channels. Each channel translates T/M High Voltage data inputs, which indicate camera photomultiplier supply gain step setting, to a display and a two-line coded output. A block diagram of one of these channels is given in Figure 2-2.

The five most significant bits of the T/M High Voltage data information are first converted to an analog voltage, directly proportional to the numerical value represented by the binary data inputs. This voltage output will normally assume one of four nominal values corresponding to the nominal digital values obtained in the telemetry system for each of the four gain steps.

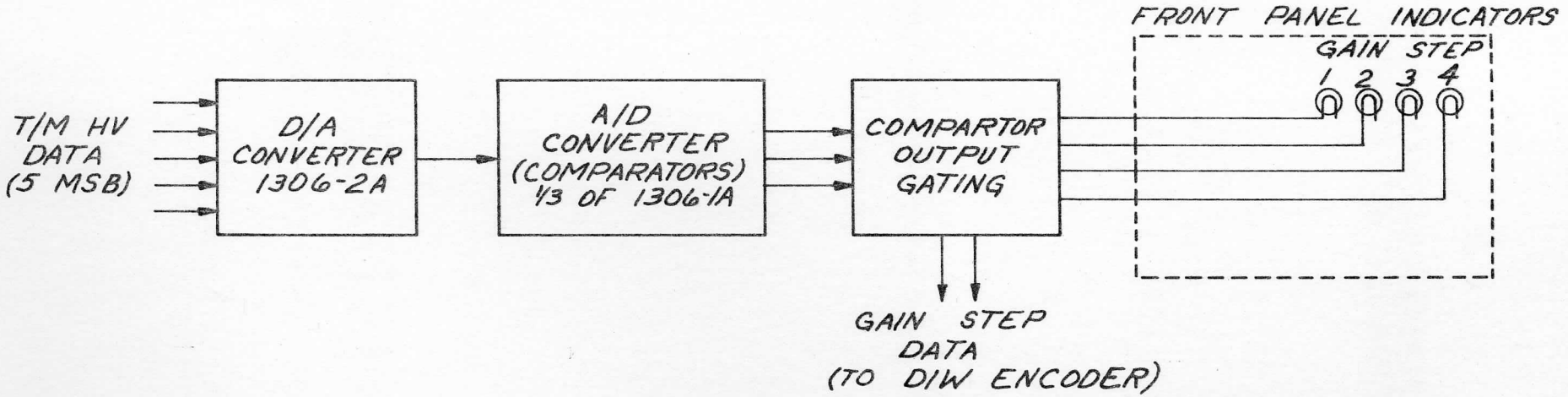


FIGURE 2-2
GAIN STEP ENCODER CHANNEL BLOCK DIAGRAM

This analog voltage is applied to the inputs of three comparators. The switching thresholds of these comparators are set to voltage levels between adjacent pairs of the nominal input voltage levels, as shown in Figure 2-3.

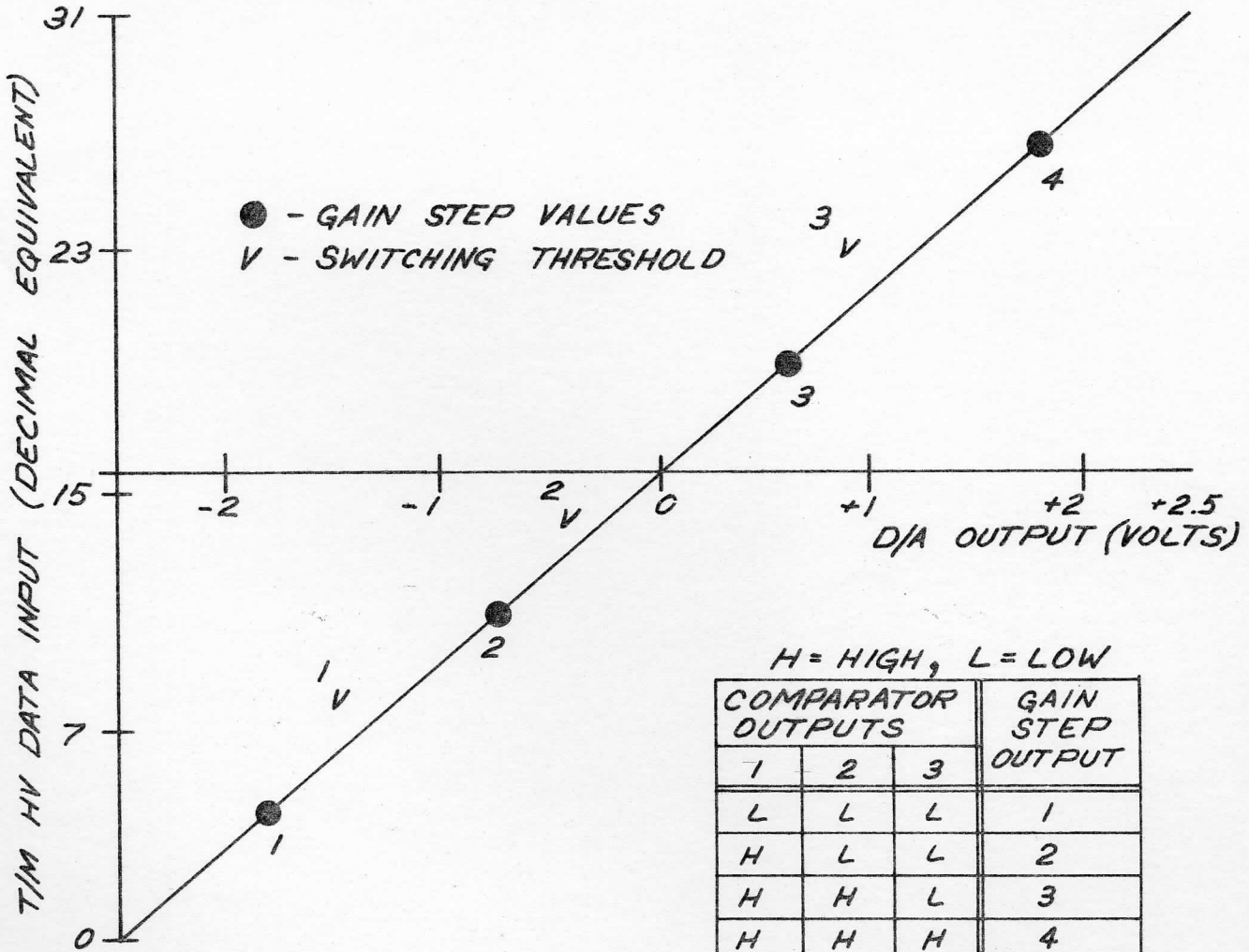
Comparator outputs are then encoded in the Comparator Output Gating logic to supply the required outputs for display and DIW coding.

2.3 DIVIDE-BY-18 COUNTER (Drawing 1306A014A)

The Analog Recorder Sync Signal (ARSS) input from the Synchronizer is a pulse train of 9×2^{14} pulses per Pre-line Start, or 18 times the number required by the SK-1600B transport. The necessary division by 18 is performed by a five-stage feedback ripple counter.

2.4 REFERENCE FREQUENCY MIXER (Drawing 1306A004A)

Two square-wave digital inputs, at 200 kHz. and the A/D sampling frequency, supplied from the MCO-1 Crystal Oscillator and the DIW Encoder Digital Clock respectively, are applied to the Reference Frequency Mixer inputs. Input drivers provide a voltage source input to following low-pass Tschebyscheff filters, which essentially pass only the fundamental component of the square-wave inputs. Filter outputs are applied to the output amplifier through level setting potentiometers.



H = HIGH, L = LOW

COMPARATOR OUTPUTS			GAIN STEP OUTPUT
1	2	3	
L	L	L	1
H	L	L	2
H	H	L	3
H	H	H	4

FIGURE 2-3 COMPARATOR THRESHOLD SETTING AND OUTPUT LOGIC TABLE

2.5 VIDEO AMPLIFIERS (Drawing 1306A002A)

The basic video amplifier consists of an operational amplifier (A301) and a complementary emitter follower output driver. Amplifier feedback is supplied through R316 from the driver output. Balance control R317 adjusts a compensating current for amplifier offset correction.

The video input signal is set to the proper level by potentiometer R308 and is normally applied through R309 to the amplifier non-inverting input while the Video Gate input remains at +4 v. level. When the Video Gate input is switched to the zero volt level, transistor Q304 supplies the current required to change the FET (Q303) gate voltage from -10 to 0 v. This turns on the FET and reduces the video level at the amplifier input by 30 db.

The NRZ input is referenced to ground and inverted in polarity by the input level shifter (Q301, Q302). The NRZ level is set by potentiometer R304 and summed with the Reference Frequency input at the amplifier noninverting input.

TABLE 2-1

PANEL TO MODULE CONNECTION LIST

J101-J113, J115

Connector Reference	To Module Pin	Signal Designation
J101	B24-14	A VID
J102	B21-14	VID GRN
J103	A10-18	PLS
J104	B12-5	VCO
J105	A11-13	RLS
J106	B26-14	B VID
J107	B21-15	VID PA
J108	B26-18	VID RED
J109	B12-18	FS
J110	B10-5	ARSS
J111	B28-14	C VID
J112	B28-18	VID BLU
J113	B12-19	FE
J115	B10-X	RRF

CONNECTOR PIN	TO MODULE PIN	SIGNAL DESIGNATION
1		
2		
3		
4		
5		
6		
7		
8	B3-F	FIU1
9	B3-J	FIU2
10	B3-U	FIU4
11	B3-V	FIU8
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28	B5-F	FIT1
29	B5-J	FIT2
30	B5-U	FIT4
31		
32		
33		
34		
35		
36		
37		

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TITLE
PANEL TO MODULE
CONNECTION LIST - J-116

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	GW	5-2-68				

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	A	1 OF 1	1306A020A

CONNECTOR PIN	TO MODULE PIN	SIGNAL DESIGNATION
1		
2	B5-5	XHR1
3	B5-3	XHR2
4	B3-5	UHR1
5	B3-3	UHR2
6	B3-22	UHR4
7	B3-21	UHR8
8	B9-5	XMN1
9	B9-3	XMN2
10	B9-22	XMN4
11	B7-5	UMN1
12	B7-3	UMN2
13	B7-22	UMN4
14	B7-21	UMN8
15	B4-7	XSC1
16	B4-8	XSC2
17	B4-19	XSC4
18	B2-7	USC1
19		
20		
21	B2-8	USC2
22	B2-19	USC4
23	B2-20	USC8
24	B5-E	MVC1
25	B5-C	MVC2
26	B3-E	CVC1
27	B3-C	CVC2
28	B3-Z	CVC4
29	B3-Y	CVC8
30	B9-E	XVC1
31	B9-C	XVC2
32	B9-Z	XVC4
33	B9-Y	XVC8
34	B7-E	UVC1
35	B7-C	UVC2
36	B7-Z	UVC4
37	B7-Y	UVC8

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TITLE
PANEL TO MODULE
CONNECTION LIST – J-117

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	GW	5-2-68				

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	A	1 OF 1	1306A021A

CONNECTOR PIN	TO MODULE PIN	SIGNAL DESIGNATION
1		
2	B8-20	SCDR
3	B8-19	MODE
4	B9-21	SVGN
5	B5-Y	CVG1
6	B7-F	CVG2
7	B7-J	CVG4
8	B9-J	AVG1
9	B9-U	AVG2
10	B9-V	AVG4
11	B7-U	BVG1
12	B7-V	BVG2
13	B9-F	BVG4
14	B7-19	SCOP
15	B4-20	SWPL
16	B7-8	GCLR
17	B7-7	RCLR
18	B5-V	BCLR
19		
20		
21	N.C.	B&W
22	B8-U	BHV1
23	B8-V	BHV2
24	B2-F	BHV3
25	B2-J	BHV4
26	B2-U	BHV5
27	B6-J	CHV1
28	B6-U	CHV2
29	B6-V	CHV3
30	B8-F	CHV4
31	B8-J	CHV5
32	B2-V	AHV1
33	B4-F	AHV2
34	B4-J	AHV3
35	B4-U	AHV4
36	B4-V	AHV5
37	⏚	GRND.

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TITLE
PANEL TO MODULE
CONNECTION LIST - J-118

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	MW	5-2-68				

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	A	1 OF 1	1306A022A

3.0 MAINTENANCE

3.1 GENERAL

The module card arrangement of circuitry in the Color Data Processor allows complete and convenient access to all components and test points for trouble-shooting and component replacement.

Circuit modules are contained in two card files, located in the center and rear of the card drawer. The center file is designated "A" and the rear file "B." Module card locations within each file are numbered 1 through 28 on the card file top rails. The module card types assigned to each location are listed in Table 3-2

Circuits diagrammed in the schematics are labeled with a letter-number combination denoting file and module slot locations. Inputs and outputs are labeled with the appropriate module connector pin designation. All location, pin, and connector designations are lettered vertically. All other labels are slant lettered to avoid ambiguities.

The block diagrams, logic sequence diagram (Figure 4-1), and Wyle module performance sheets provide additional information required for trouble-shooting.

3.2 CALIBRATION AND ADJUSTMENT

Readjustment of controls is not normally necessary, but should be performed if changes in the calibrated video input levels or T/M High Voltage data nominal values should occur. Control settings should also be checked, in the circuits related, after corrective maintanance is performed.

Locations of adjustment controls are shown in Figure 3-1.

An accurately calibrated oscilloscope is the only test equipment required for the entire calibration procedure. It is used to observe the video amplifier outputs, available on the test panel located immediately above the Processor at the BNC jacks labeled RECORDER INPUT, A, B, C.

The Westinghouse Synchronizer must be operated in the SIMULATE mode to perform video amplifier adjustments.

3.21 Video Amplifier Adjustment Procedure

1. Pull out the Processor card drawer until card file B is fully accessible from above. Place front panel switch S2 to select GREEN input.

2. Turn off power supply, and extract the MCO-1 module in location B1 and move switch S1 to the 200 kHz position. Turn on power supply. This procedure removes the Reference Frequency Signal input to all video amplifiers.

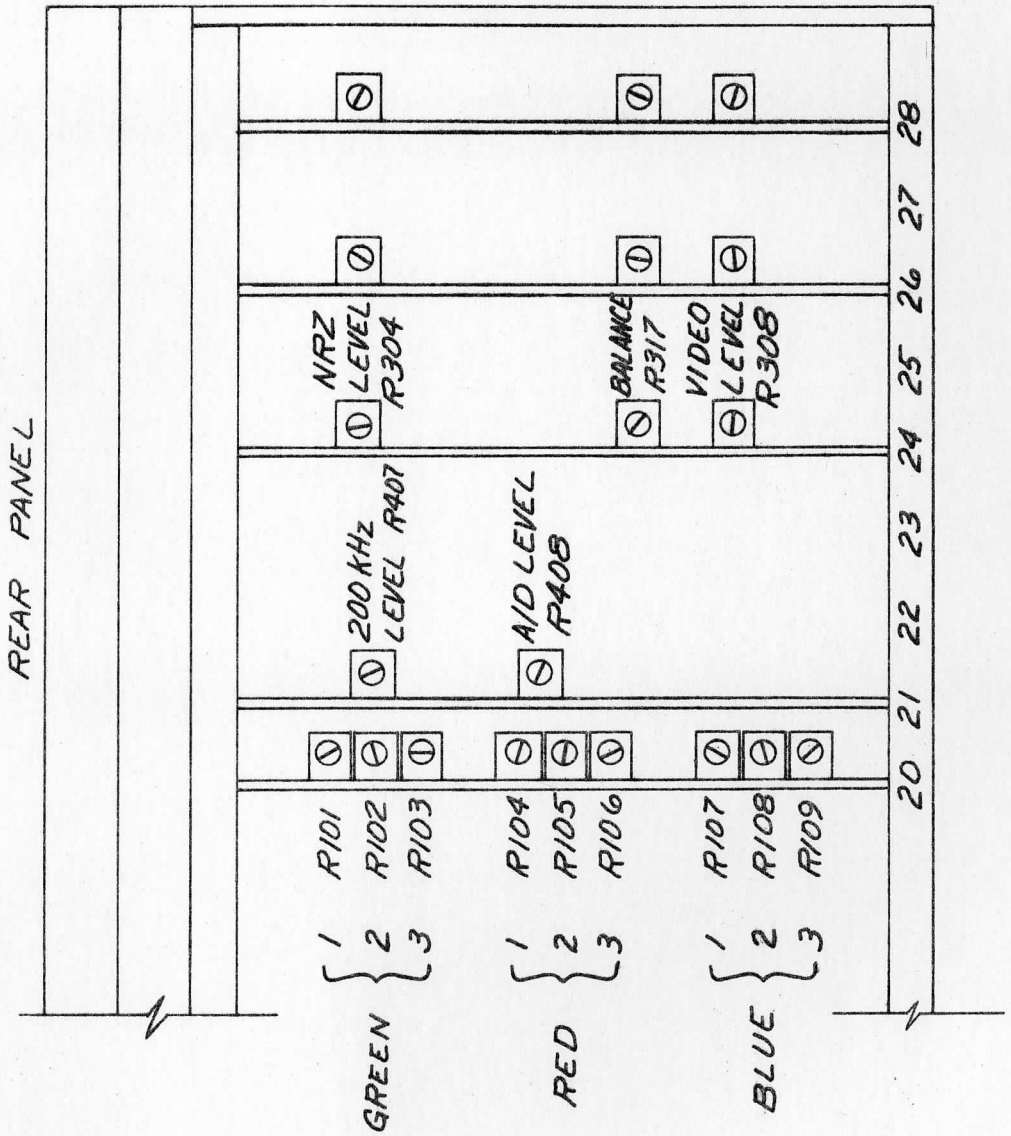
3. Disconnect the video input cable for the amplifier being adjusted at the Processor rear panel. Video input connectors are:

Channel A - J102

Channel B - J108

Channel C - J112

4. Observe the video amplifier output with an oscilloscope with DC coupled input and a sensitivity of 10 mv./cm. Externally synchronize the oscilloscope, using the SYNC 1 output on the Processor front panel, and set the time base to 20 ms./cm.



CARD FILE B

B20	COMPARATOR
B21	REFERENCE FREQ. MIXER
B24	VID. AMP. CHAN. A
B26	VID. AMP. CHAN. B
B28	VID. AMP. CHAN. C

FIG. 3-1 LOCATION OF CONTROLS

5. Ignoring the NRZ signal observed at the start of each trace, adjust the output level to 0 ± 1 mv. with BALANCE control R317.

6. Change the oscilloscope sensitivity to 0.5 v./cm. and time base to 100 μs./cm., and adjust the amplitude of the NRZ signal to 1.0 v. with NRZ LEVEL control R304.

7. Change the oscilloscope time base to approximately 50 ms./cm. and reconnect the video input. Observe the simulated video square wave output and adjust the amplitude to 1.50 v. with VIDEO LEVEL control R308.

Note: System calibration procedures specify that the amplitude of the simulated square wave input supplied by the Westinghouse Video Processor be +1.50 v. from a zero volt baseline.

8. Repeat steps 3 through 7 for each video amplifier requiring calibration.

9. If the Reference Frequency Mixer output levels are to be adjusted, proceed directly to step 2 of that procedure. Otherwise, turn off power momentarily while replacing the MCO-1 module in location B1 and return switch S2 to the normal AUTO (center) position.

3.22 Reference Frequency Mixer Adjustment Procedure

1. Perform steps 1 and 2 of the Video Amplifier Adjustment Procedure.

2. Discount the video input (Green) at J102.

3. Observe the Channel A video output at the RECORD INPUT A test jack on an oscilloscope externally synchronized to any SYNC output. Set the oscilloscope sensitivity to 20 mv./cm. and time base to 20 ms./cm.

4. Switch S1 to the A/D position and observe the high frequency signal which appears. Adjust the A/D LEVEL control, R408, until the peak-to-peak amplitude of this signal is 70 mv.

5. Turn off power momentarily to replace the MCO-1 module in location B1; then place switch S1 in the 200 kHz position.

6. Adjust the peak-to-peak amplitude of the observed high frequency waveform to 70 mv. with the 200 kHz LEVEL control, R407.

7. Replace the video input at J102, and place switches S1 and S2 to their normal center positions (BOTH and AUTO).

3.23 Comparator Adjustment Procedure

1. Determine the nominal telemetry High Voltage data reading for the four gain steps of the color channel requiring adjustment.

Example: Green channel telemetry data (in octal) readings for the four gain steps may be found to be:

Gain Step	Octal Data	5 MSB Binary	Decimal
1	064	00011	3
2	341	01110	14
3	427	10001	17
4	735	11101	29

2. Convert the octal form data to binary, retaining only the five most significant bits. Then convert these binary numbers to decimal, as shown in the above example.

3. Find an integer nearest the mean of each successive pair of decimal gain step values as shown below:

Example (continued):

Gain Step	Decimal	Mean
1	3	
		8
2	14	
		15
3	17	
		23
4	29	

4. Replace the normal input to J118 with the Data Input Simulator cable plug. Turn the rotary switch to the position indicating the color channel being adjusted, and set the toggle switches to simulate the first mean value. (The down position of each switch simulates a binary "0", the up position a binary "1".)

Example (continued): To simulate the first mean value of 8, the toggle switch labeled "8" should be placed in the up position; all others should be down.

5. The threshold level of the first comparator of the color channel being adjusted should be set to the position where slight back-and-forth movement of the control causes the Gain Step 1 and 2

indicator lamps to alternately turn on and off. Table 3-1 lists the controls to be adjusted and the indications of correct setting.

Example (continued): The first comparator of the green channel is adjusted by R101 to setting where the Green Gain Step indicator lamps 1 and 2 alternate on and off.

6. Complete the adjustments of the remaining comparators in a similar manner, referring to Table 3-1 and Figure 3-1 to determine the appropriate controls required for each adjustment and their locations.

7. Replace the normal input plug to the J118 receptacle.

	Control Adjusted			Indicates
	Green	Red	Blue	Alternating
First Mean Value	R101	R104	R107	1 and 2
Second Mean Value	R102	R105	R108	2 and 3
Third Mean Value	R103	R106	R109	3 and 4

Table 3-1. Comparator Adjustment List.

File and Location	Module Type
A1	Blank
A2	MPG-8
A3	MPG-8
A4	MAG-9
A5	MSR-8
A6	MNG-12
A7	MSR-8
A8	MBD-1
A9	MUF-5
A10	MUF-5
A11	MOF-4
A12	MAG-9
A13	MUF-5
A14	MNG-12
A15-28	Blank

File and Location	Module Type
B1	MCO-1
B2	MDS-4
B3	MDS-4
B4	MDS-4
B5	MDS-4
B6	MDS-4
B7	MDS-4
B8	MDS-4
B9	MDS-4
B10	MUF-5
B11	MNG-12
B12	MUF-5
B13-16	Blank
B17	D/A Conv. (1306-2A) Green HV
B18	D/A Conv. (1306-2A) Red HV
B19	D/A Conv. (1306-2A) Blue HV
B20	Comparator (1306-1A)
B21	Ref.Freq.Mixer (1306-4A)
B22-23	Blank
B24	Video Amp. (1306-3A) Chan.A
B25	Blank
B26	Video Amp. (1306-3A) Chan. B
B27	Blank
B28	Video Amp. (1306-3A) Chan. C

Table 3-2. Module Card Locations.

4.0 SCHEMATICS AND DIAGRAMS

DATA BIT 0 8 16 24 32 40 48 56 64 72 80 88 (0)

ONTROL CTR STATE 144 152 160 168 176 184 192 200 208 216 224 232 240 248 256

DECODER OUTPUT 0 1 2 3 4 5 6 7 8 9 10 11 12

SHIFT REG. GATE), SNC1

SNC 2

SNC 3

F9-Q

F8-Q

F7-Q

F6-Q

3 DEC (3 DECODE)

SRA RESET

SRB RESET

7 DEC (7 DECODE)

DX (SRA DATA XFR)

DX (SRB DATA XFR)

NGR

SRA CLOCK GATE

SRB CLOCK GATE

OUTPUT SELECT)

DECODER OUTPUT 0 1 2 3 4 5 6 7 8 9 10 11 12

OL CTR STATE 144 152 160 168 176 184 192 200 208 216 224 232 240 248 256

DATA BIT 0 8 16 24 32 40 48 56 64 72 80 88 (0)

FIGURE 4-1 LOGIC SEQUENCE DIAGRAM

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED

CPA 3 7
CPA 2 6
CPA 1 5
COMPARATOR "A" INPUT 3
CPB 3 15
CPB 2 14
CPB 1 13
COMPARATOR "B" INPUT 8
CPC 3 20
CPC 2 19
CPC 3 18
COMPARATOR "C" INPUT 16

A101 A102 A103 A104 A105 A106 A107 A108 A109

R101 20K R102 20K R103 20K
R104 20K R105 20K R106 20K
R107 20K R108 20K R109 20K

R110 4.3k
R111 4.3k
R112 47
R113 180
R115 220
R144 220

+12
A
B
-6

D102 IN4743
D101 IN4735
D104
D103 IN4742

C102 .047μf
C103 .047μf
C101 .047μf

1 +15
2 +12v. REF.
4 12 17 COM.
21 -12v. REF.
22 -15v.

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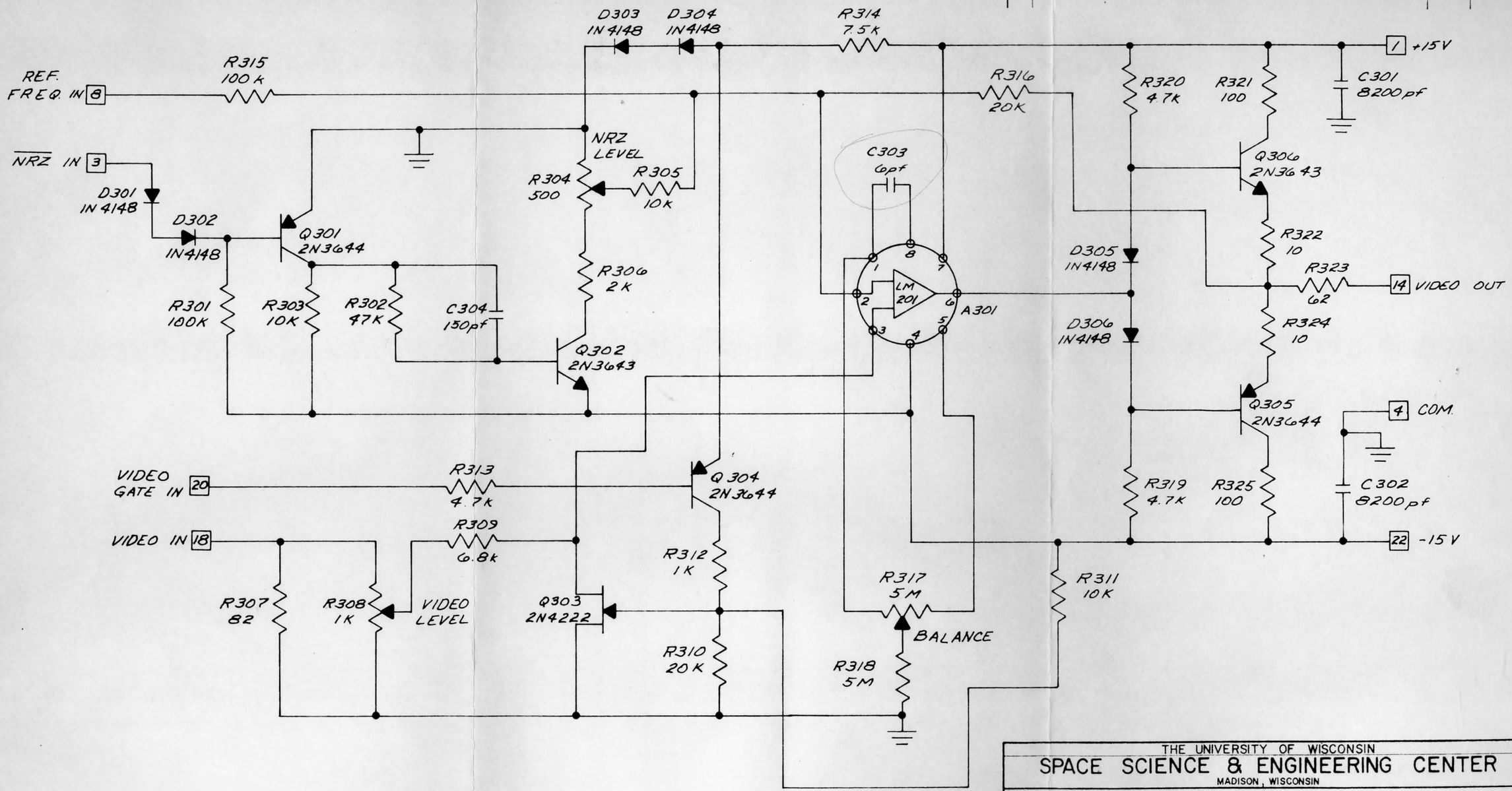
TITLE
A-D CONVERTER
1306-1A

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	GW	2-5-68			J.C.S.	2-23-68

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A001A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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MADISON, WISCONSIN

TITLE

VIDEO AMPLIFIER

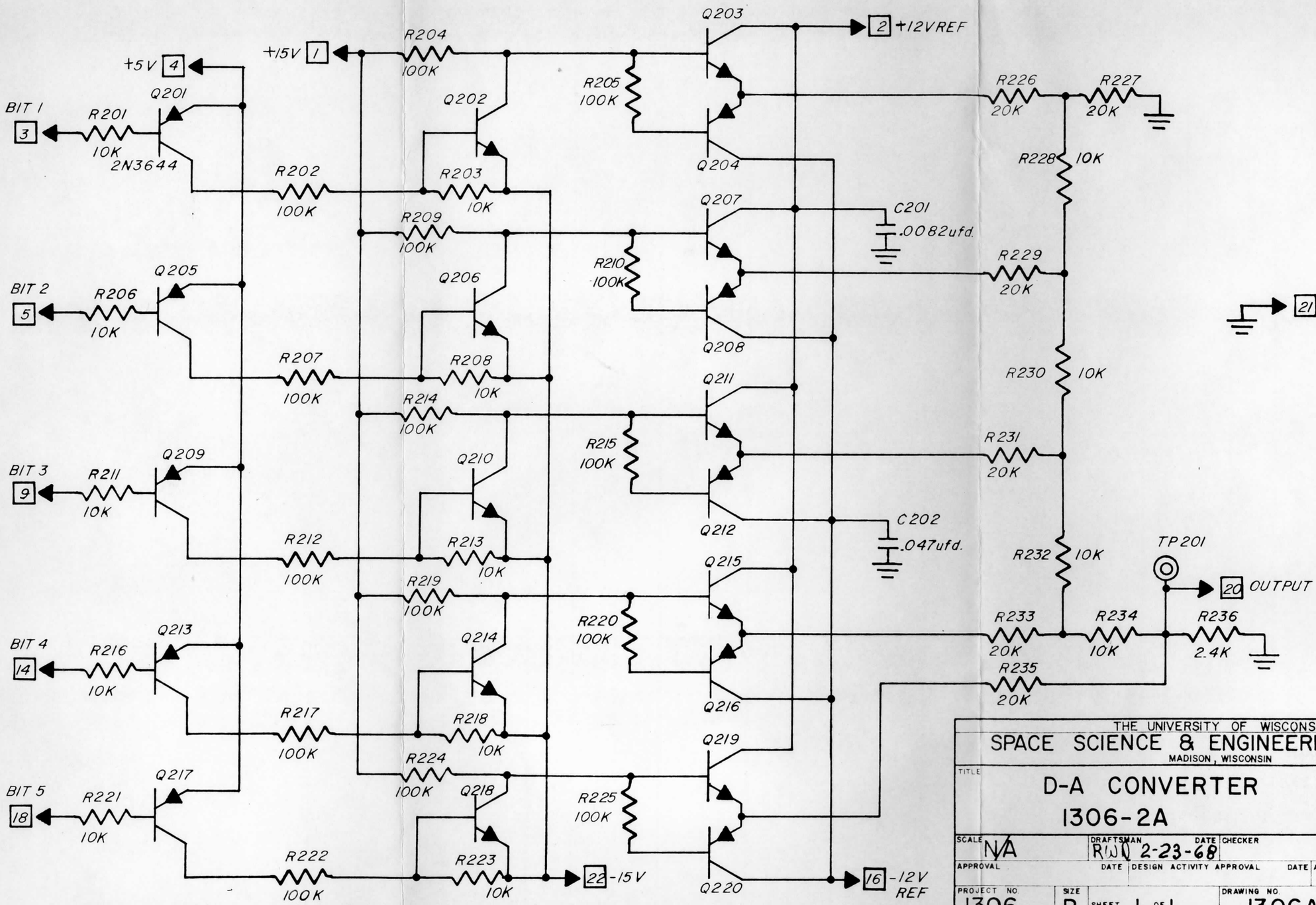
1306-3A

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A		1-24-68			J.C.S.	2-23-68

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A002A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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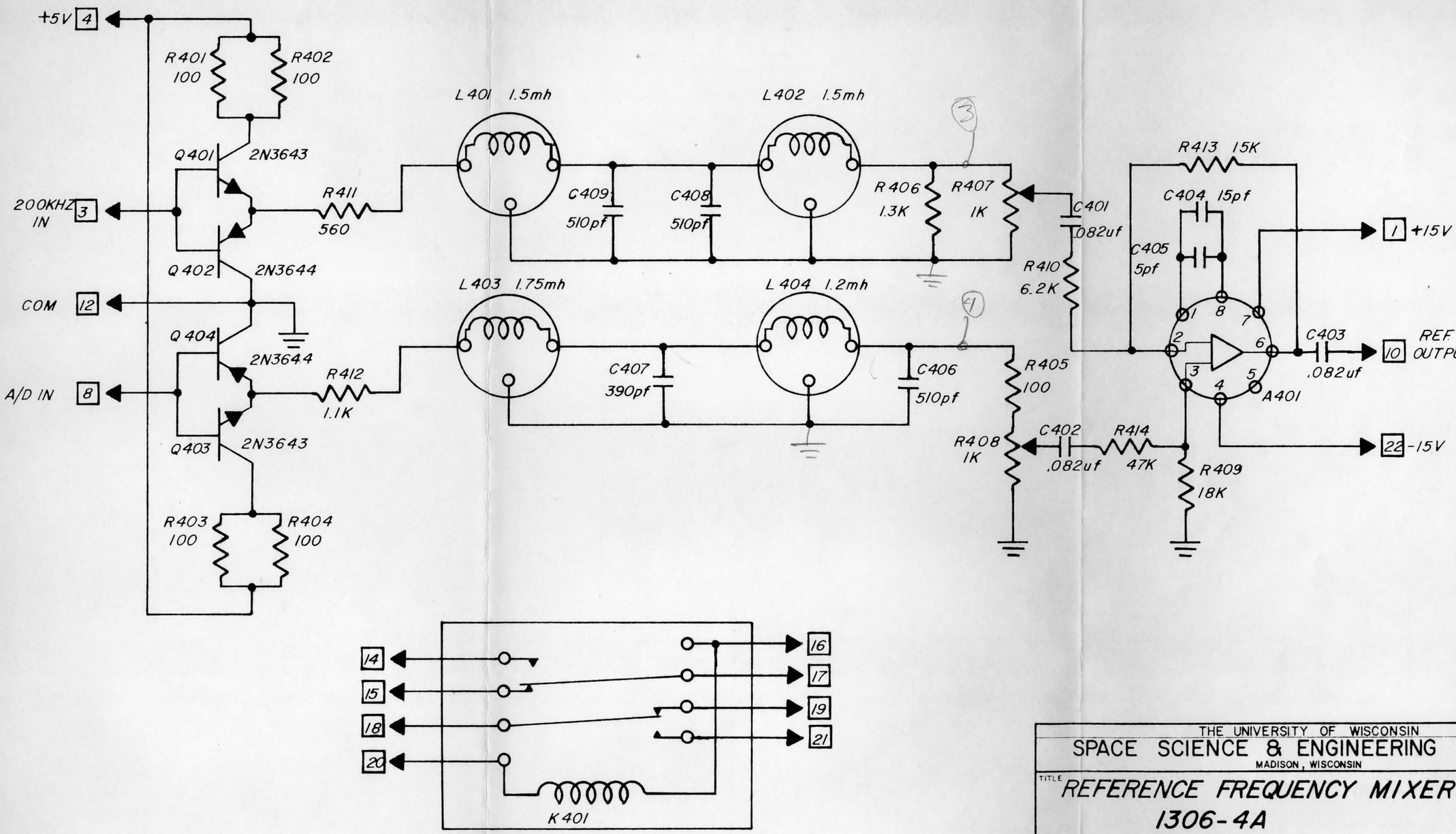
TITLE
D-A CONVERTER
1306-2A

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	RWQ	2-23-68			J.C.S	2-23-68
APPROVAL		DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A003A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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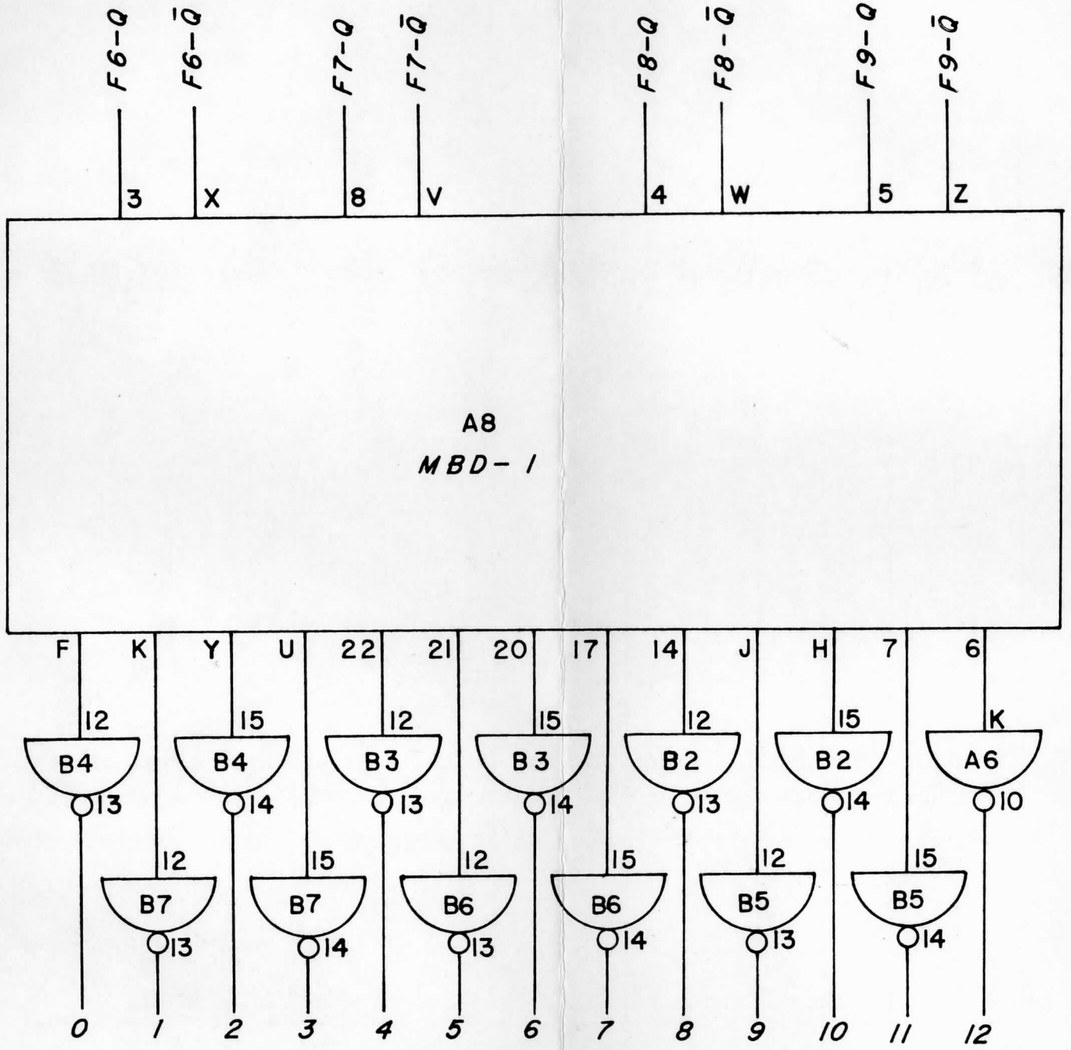
TITLE: REFERENCE FREQUENCY MIXER
1306-4A

SCALE	DRAFTSMAN / DATE	CHECKER / DATE	ENGINEER / DATE
N/A	RWR 2-24-68		J.C.J. 2-23-68

APPROVAL / DATE	DESIGN ACTIVITY APPROVAL / DATE	ADDITIONAL APPROVAL / DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A004A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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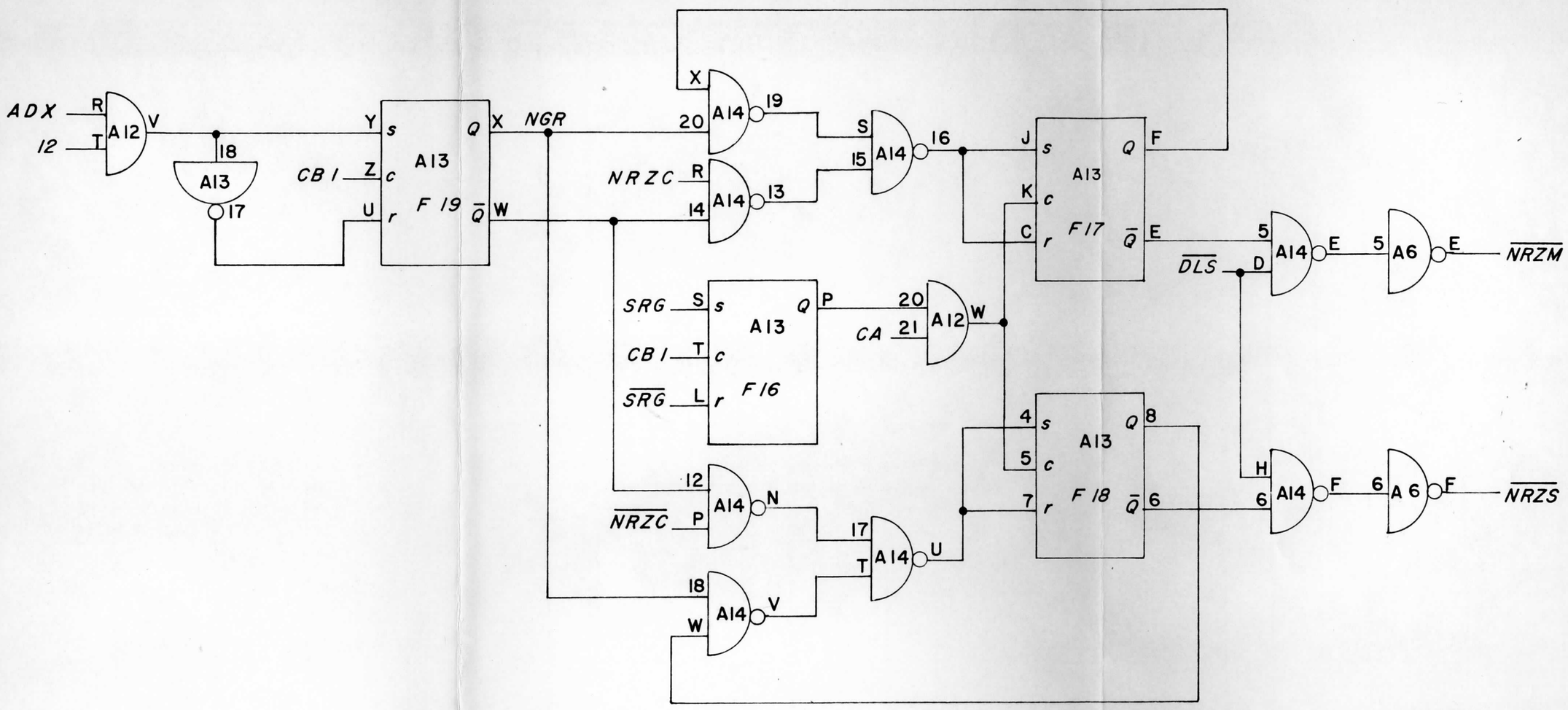
TITLE
BINARY DECODER

SCALE	DRAFTSMAN / DATE	CHECKER / DATE	ENGINEER / DATE
N/A	WQC 2/15/68		J.C.S. 2-23-68

APPROVAL / DATE	DESIGN ACTIVITY APPROVAL / DATE	ADDITIONAL APPROVAL / DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A005A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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TITLE

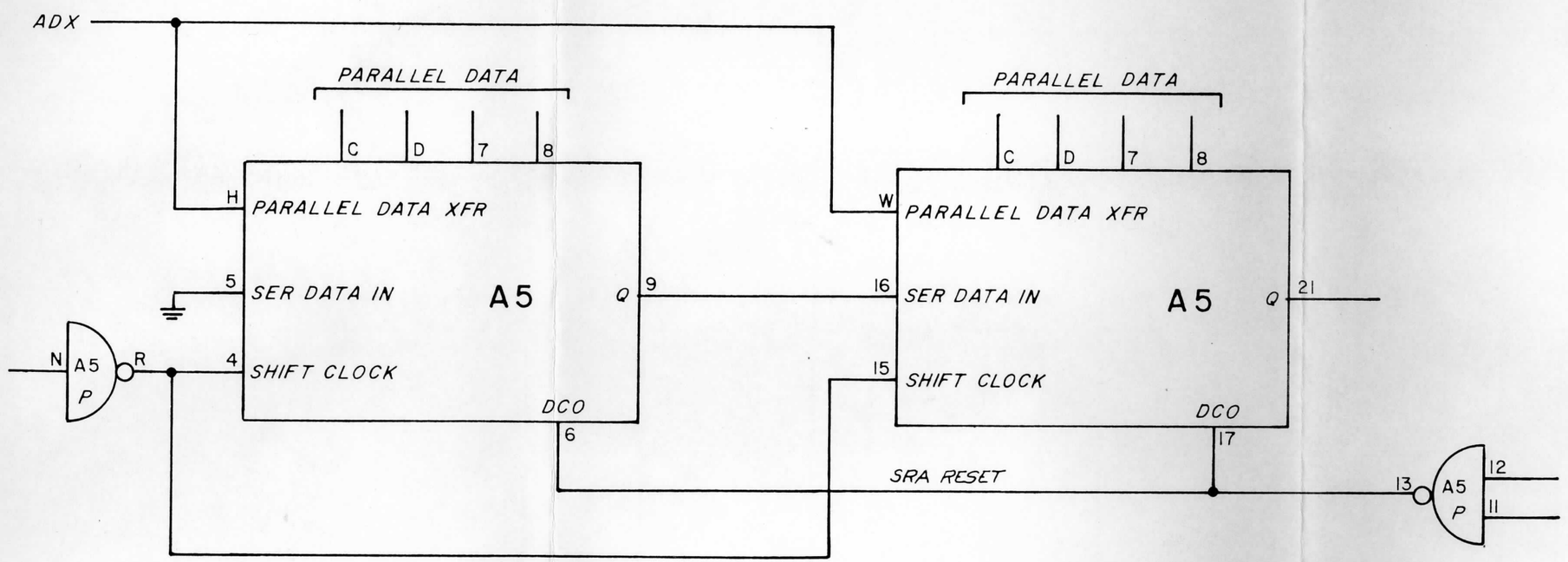
NRZ GENERATOR

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	LDQC	2/20/68			J.C.S.	2-23-68

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A006A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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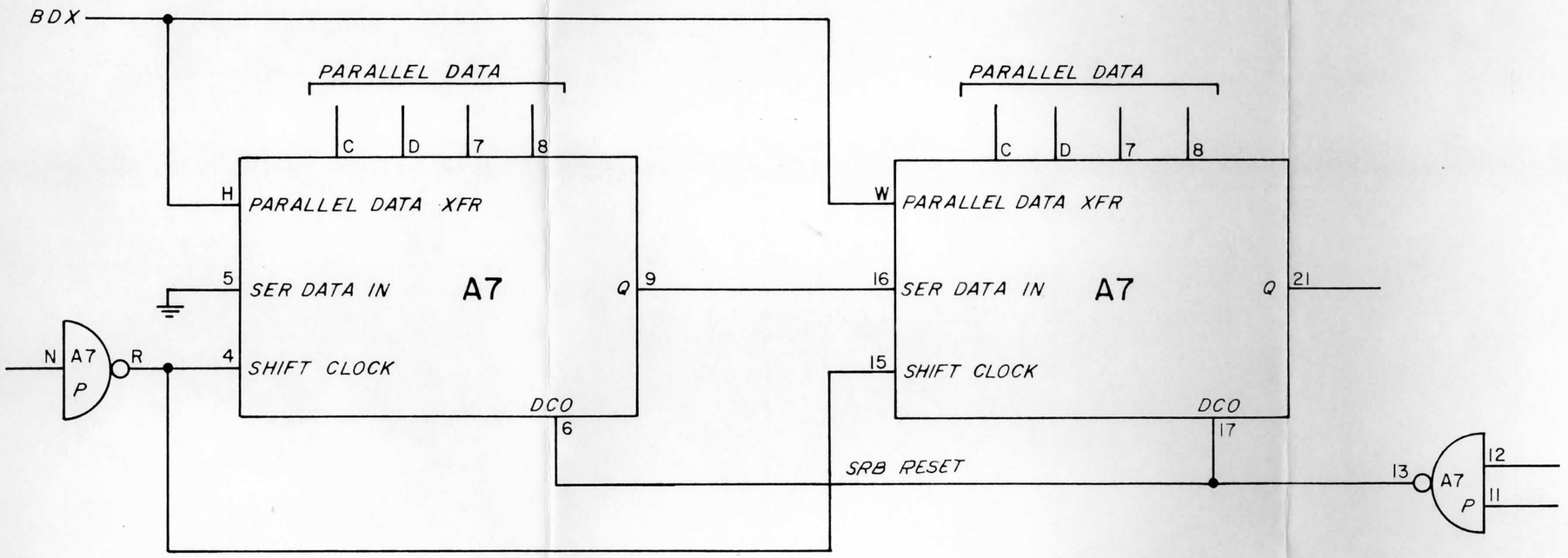
TITLE
SHIFT REGISTER A

SCALE	DRAFTSMAN DATE	CHECKER DATE	ENGINEER DATE
N/A	RWD 2-26-68		J.C.L. 2-23-68

APPROVAL DATE	DESIGN ACTIVITY APPROVAL DATE	ADDITIONAL APPROVAL DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A007A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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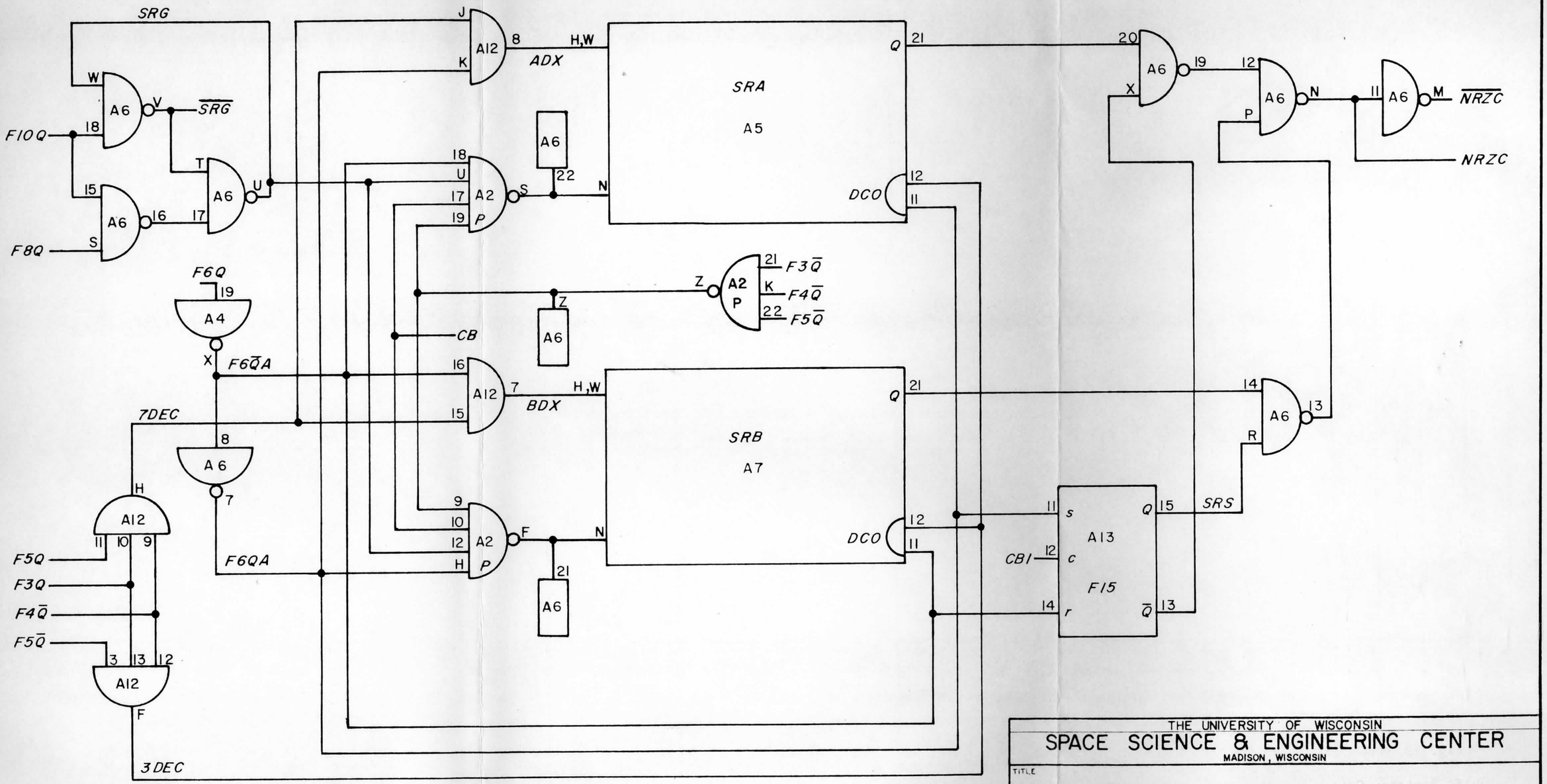
TITLE
SHIFT REGISTER B

SCALE	DRAFTSMAN DATE	CHECKER DATE	ENGINEER DATE
N/A	RWR 2-26-68		J.C.S 2-23-68

APPROVAL DATE	DESIGN ACTIVITY APPROVAL DATE	ADDITIONAL APPROVAL DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A008A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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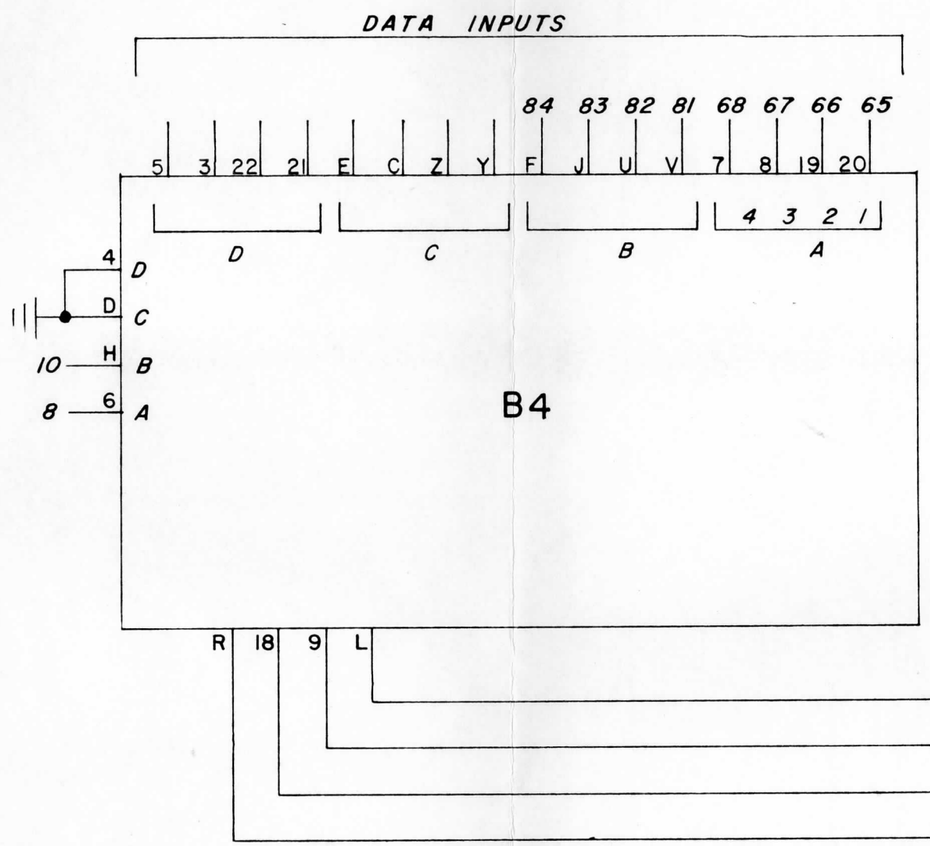
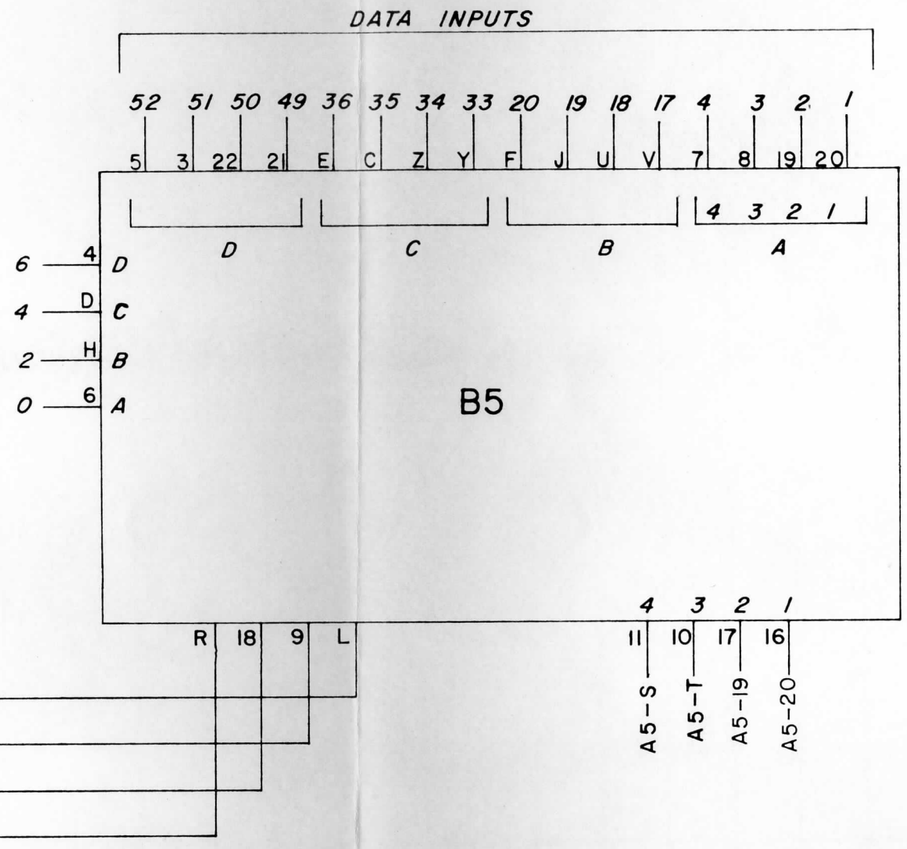
TITLE
SHIFT REGISTER GATING

SCALE	DRAFTSMAN / DATE	CHECKER / DATE	ENGINEER / DATE
N/A	RWJ 2-24-68		J.C.J. 2-23-68
APPROVAL / DATE	DESIGN ACTIVITY APPROVAL / DATE	ADDITIONAL APPROVAL / DATE	
PROJECT NO. 1306	SIZE B	SHEET 1 OF 1	DRAWING NO. 1306A009A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED





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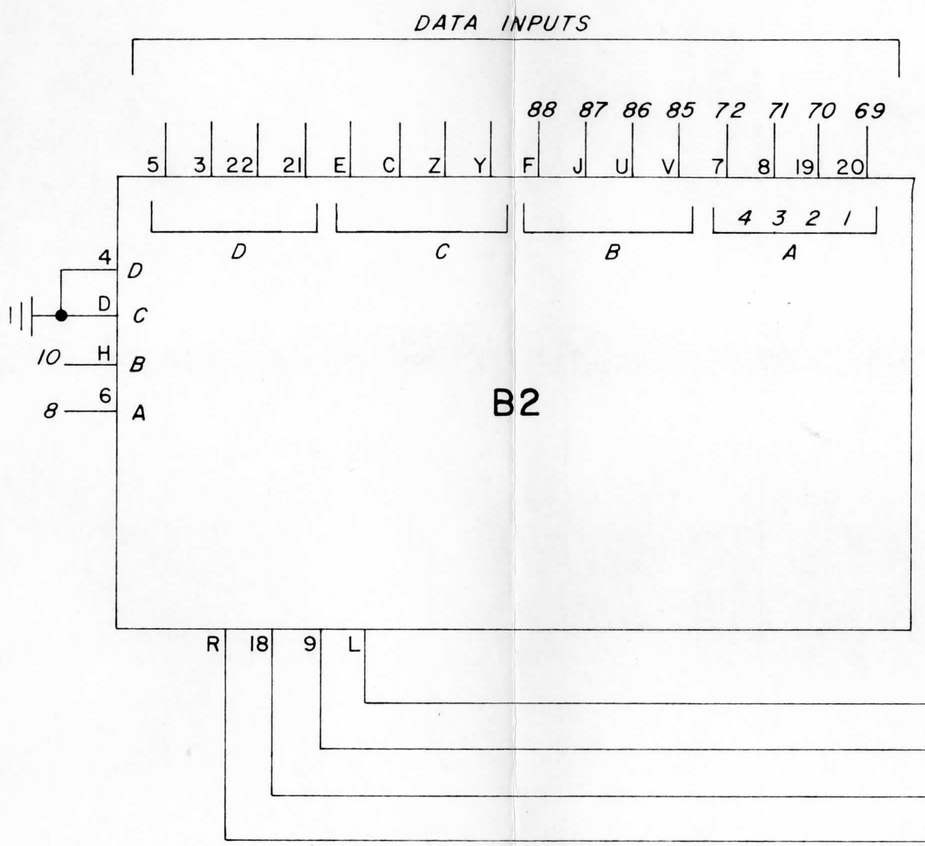
TITLE
DATA SCANNER, SRA, LSB

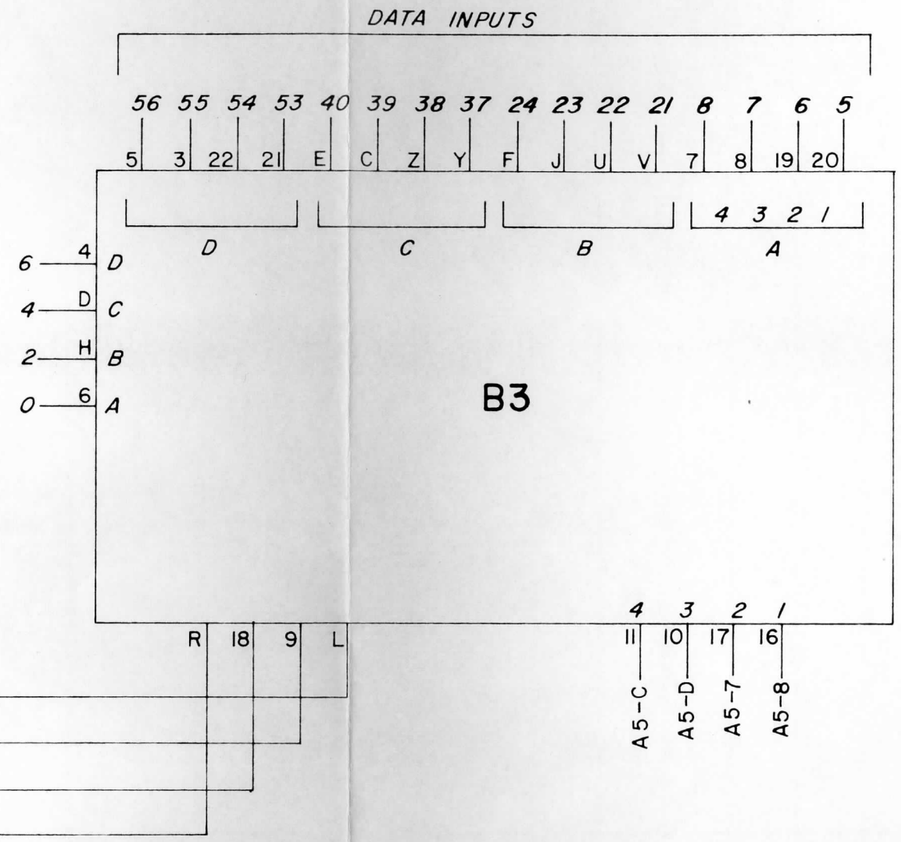
SCALE	DRAFTSMAN / DATE	CHECKER / DATE	ENGINEER / DATE
N/A	R.W.D. 2-16-68		J.C.S 2-23-68

APPROVAL / DATE	DESIGN ACTIVITY APPROVAL / DATE	ADDITIONAL APPROVAL / DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A010A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED





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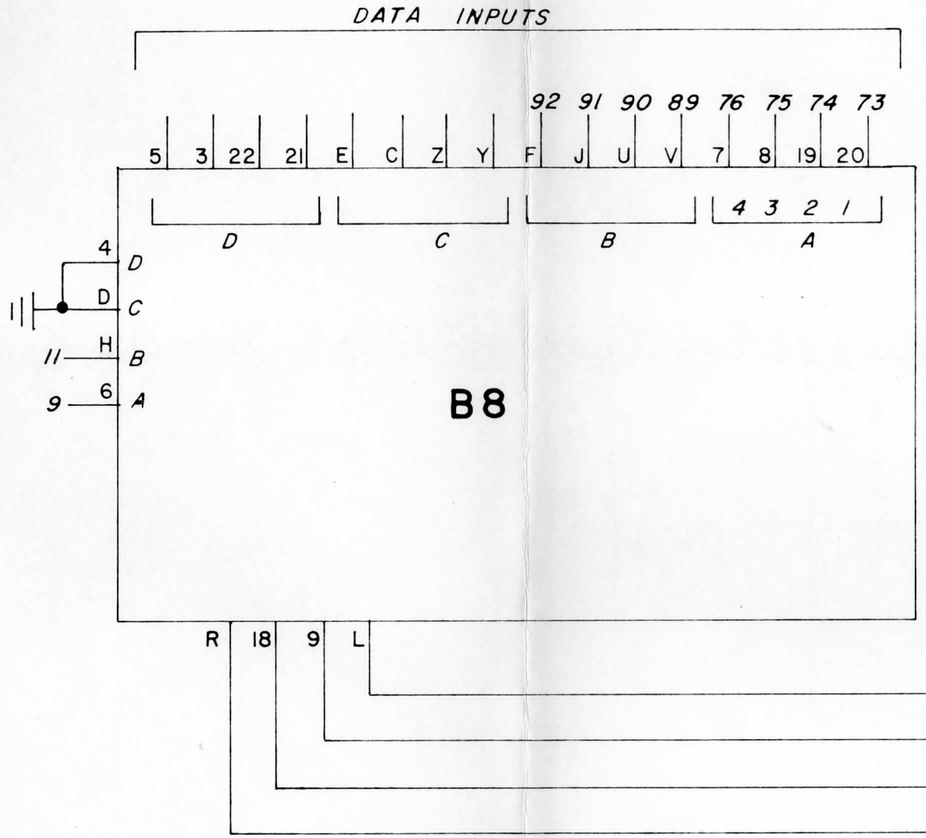
TITLE
DATA SCANNER, SRA, MSB

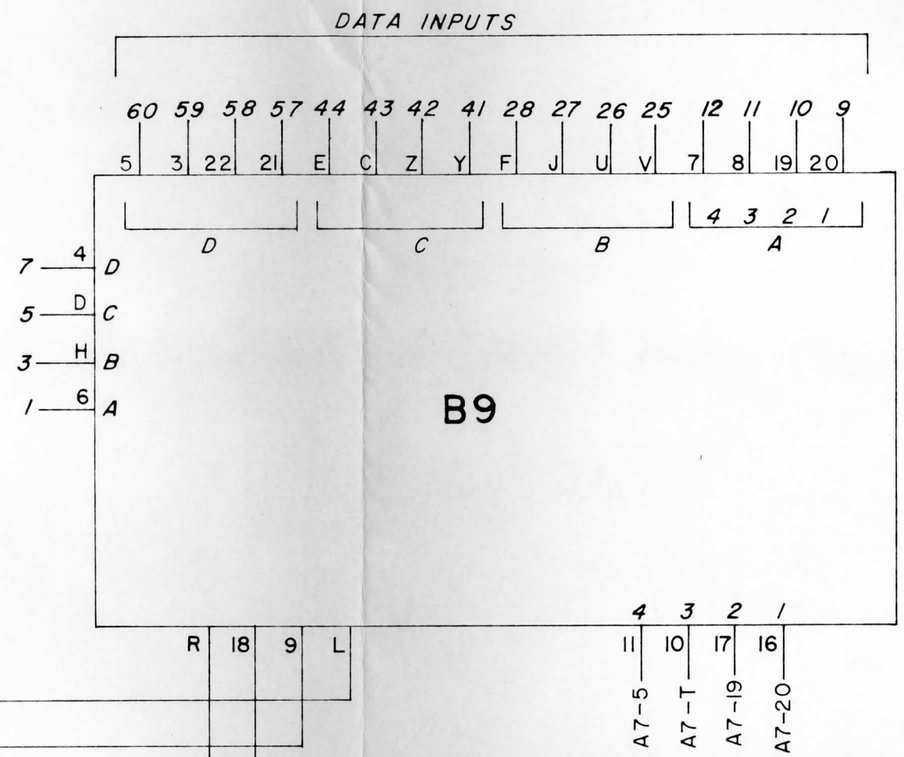
SCALE	DRAFTSMAN / DATE	CHECKER / DATE	ENGINEER / DATE
N/A	R.W.D. 2-16-68		J.C.S. 2-23-68

APPROVAL / DATE	DESIGN ACTIVITY APPROVAL / DATE	ADDITIONAL APPROVAL / DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A011A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED





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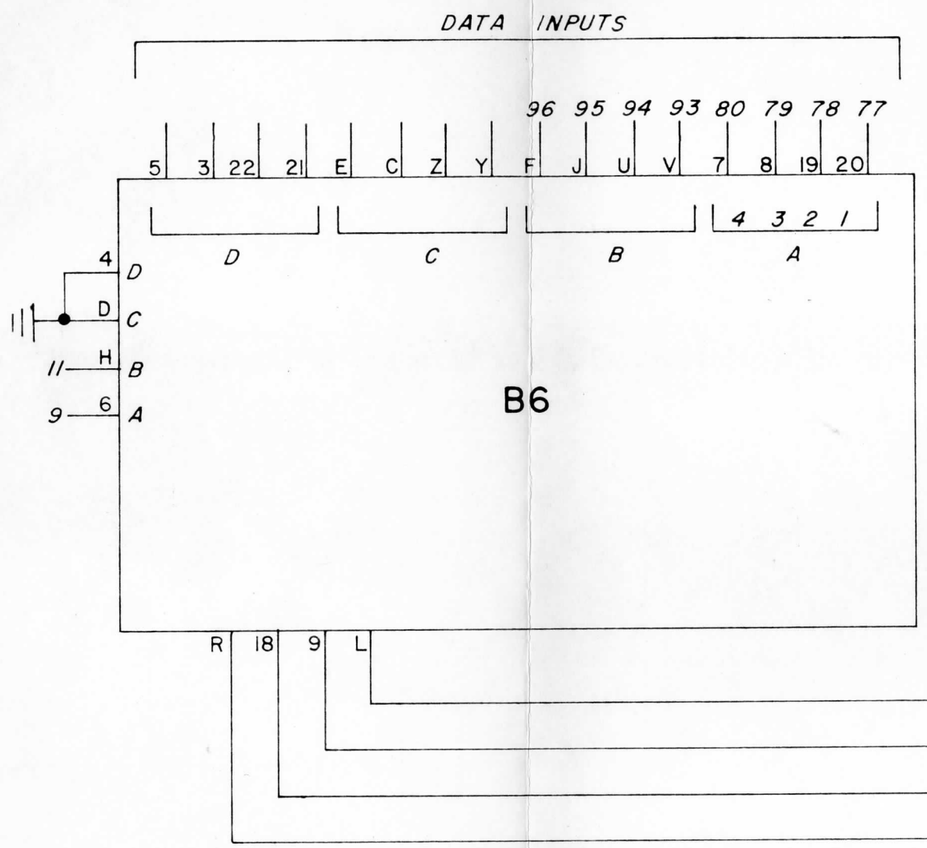
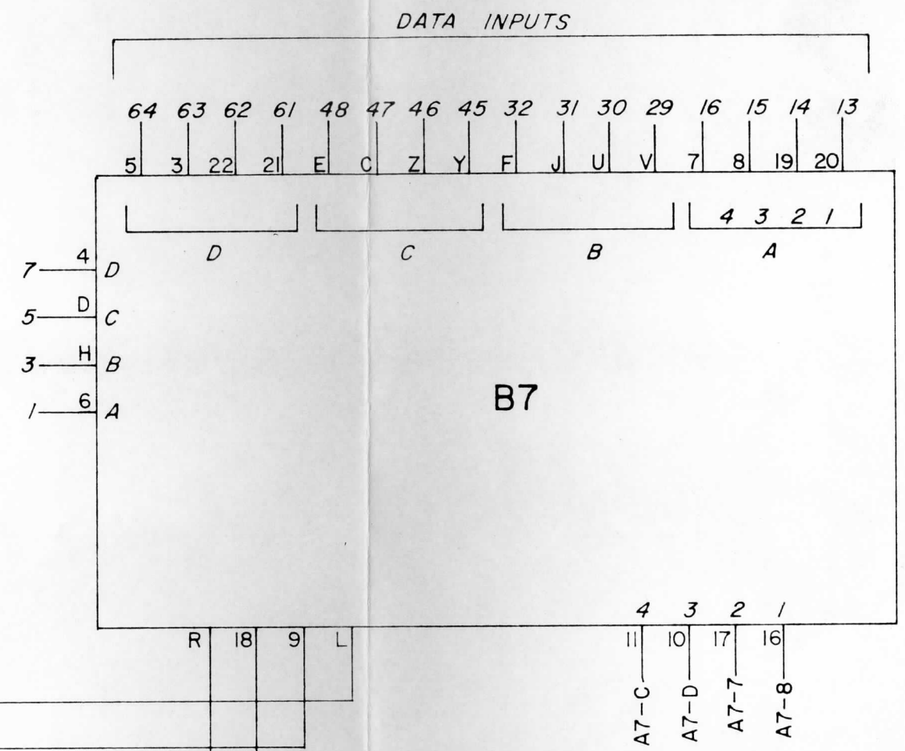
TITLE
DATA SCANNER, SRB, LSB

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	R.W.D.	2-16-68			J.C.S.	2-23-68
APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE	

PROJECT NO	SIZE	SHEET	OF	DRAWING NO.
1306	B	1	1	1306A012A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED





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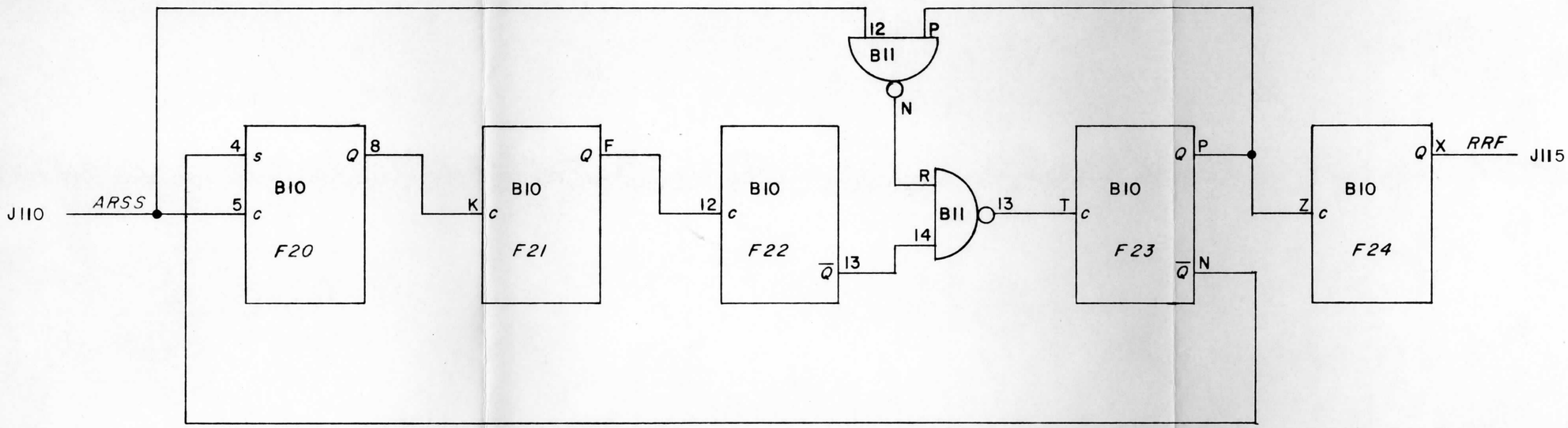
TITLE
DATA SCANNER, SRB, MSB

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	RWW	2-16-68			J.C.J.	2-23-68

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A013A

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED



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TITLE

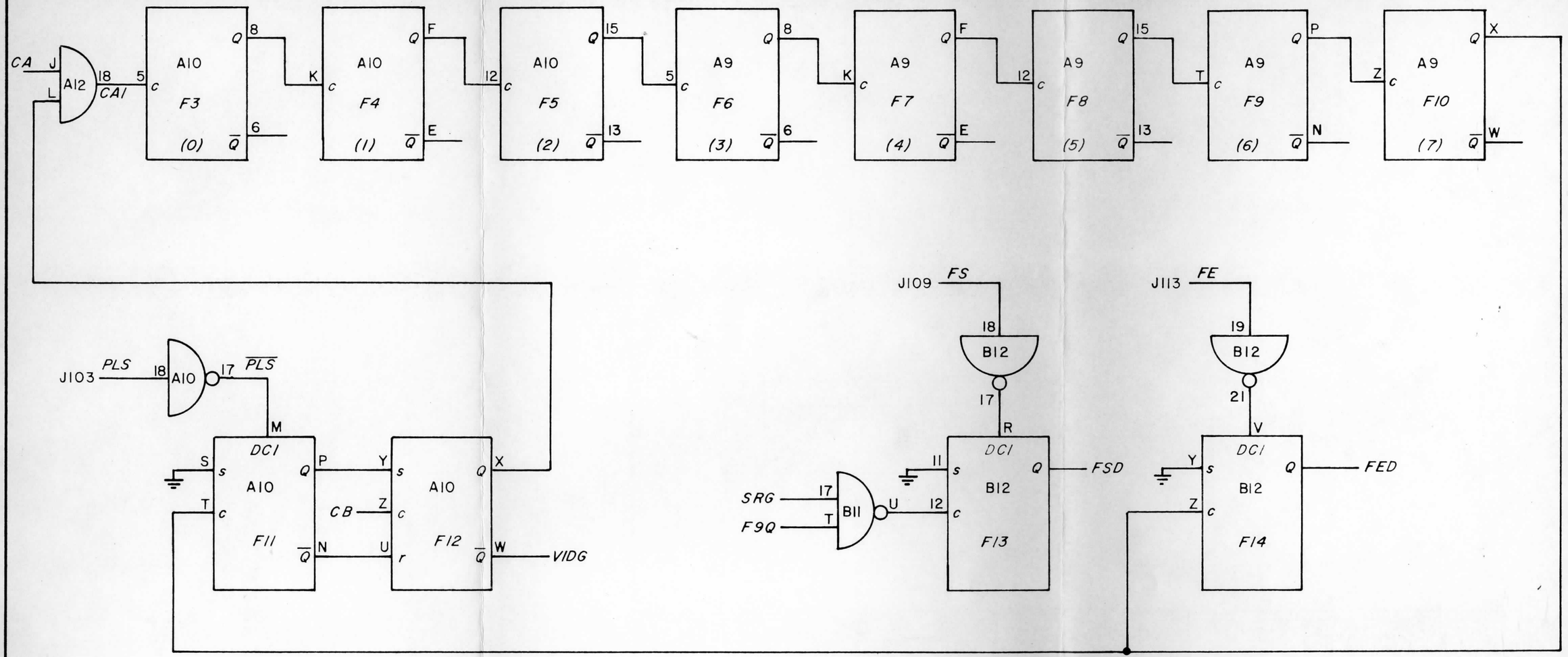
÷18 COUNTER

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	RD	2-13-68			J.C.L.	2-23-68

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO	SIZE	SHEET	DRAWING NO
1306	B	1 OF 1	1306A014A

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED



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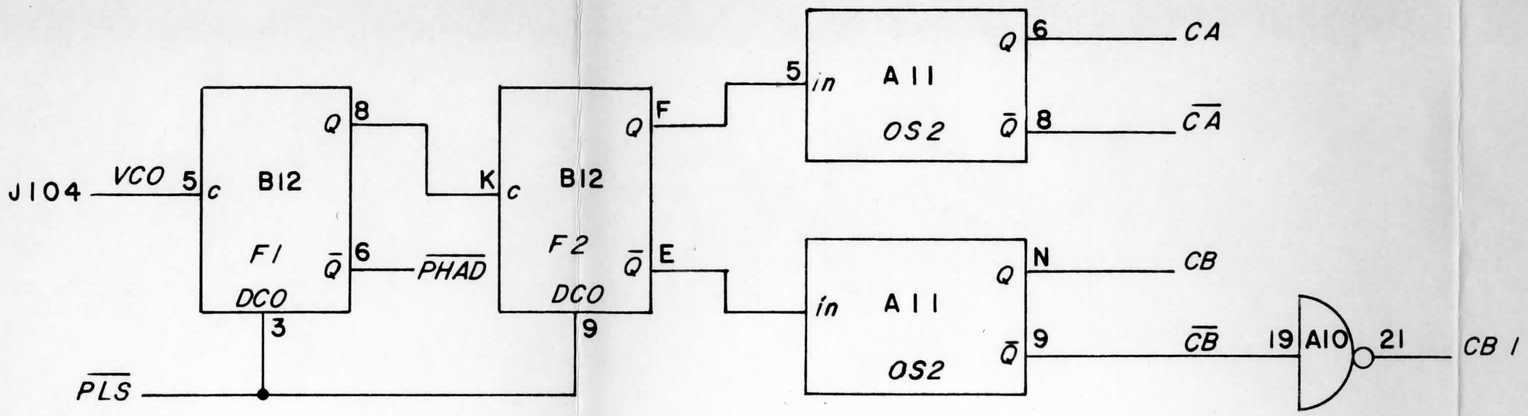
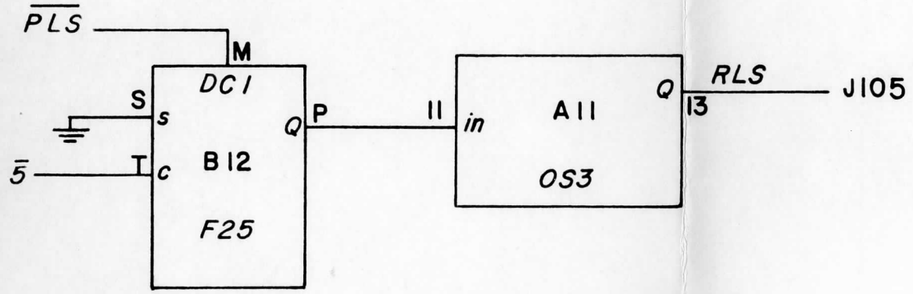
TITLE

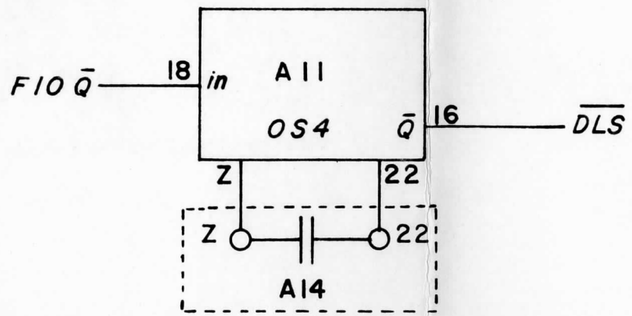
CONTROL COUNTER

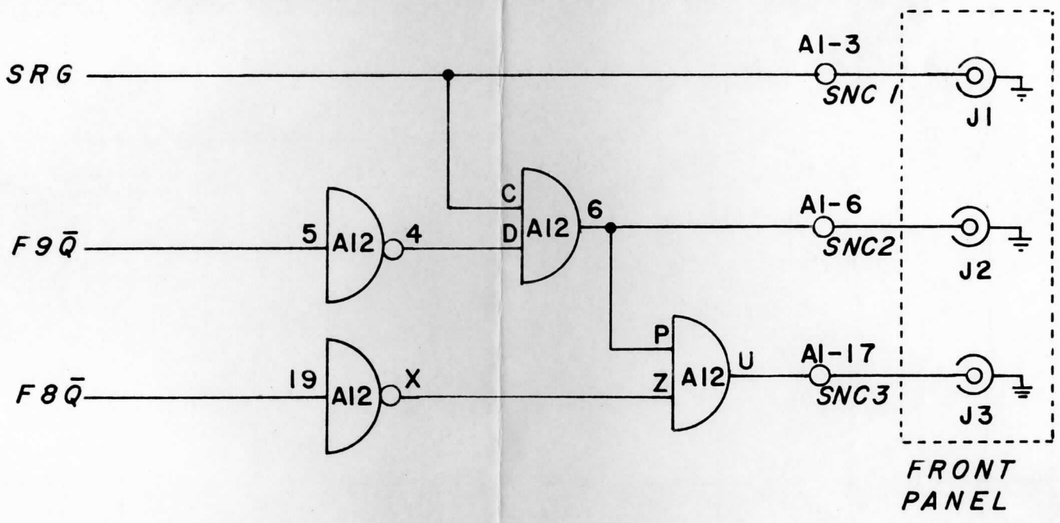
SCALE	DRAFTSMAN DATE	CHECKER DATE	ENGINEER DATE
N/A	RWD 2-26-68		J. C. S. 2-23-68
APPROVAL DATE	DESIGN ACTIVITY APPROVAL DATE	ADDITIONAL APPROVAL DATE	
PROJECT NO 1306	SIZE B	SHEET 1 OF 1	DRAWING NO 1306A015A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED









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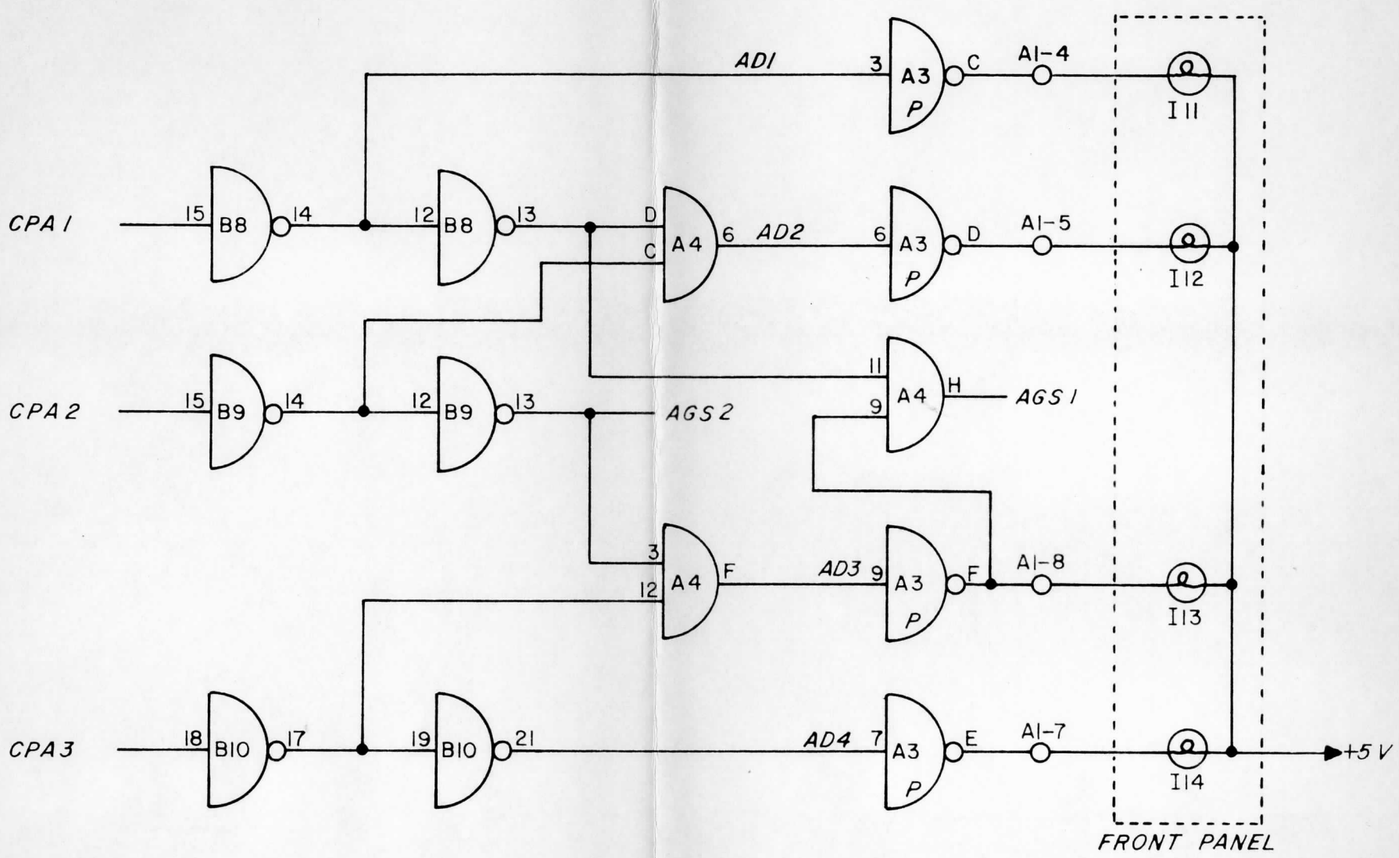
TITLE

CLOCK AND GATING

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	DQC	2/15/68			J.C.S.	2-23-68
APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE	

PROJECT NO.	SIZE	SHEET	DRAWING NO.
1306	B	1 OF 1	1306A016A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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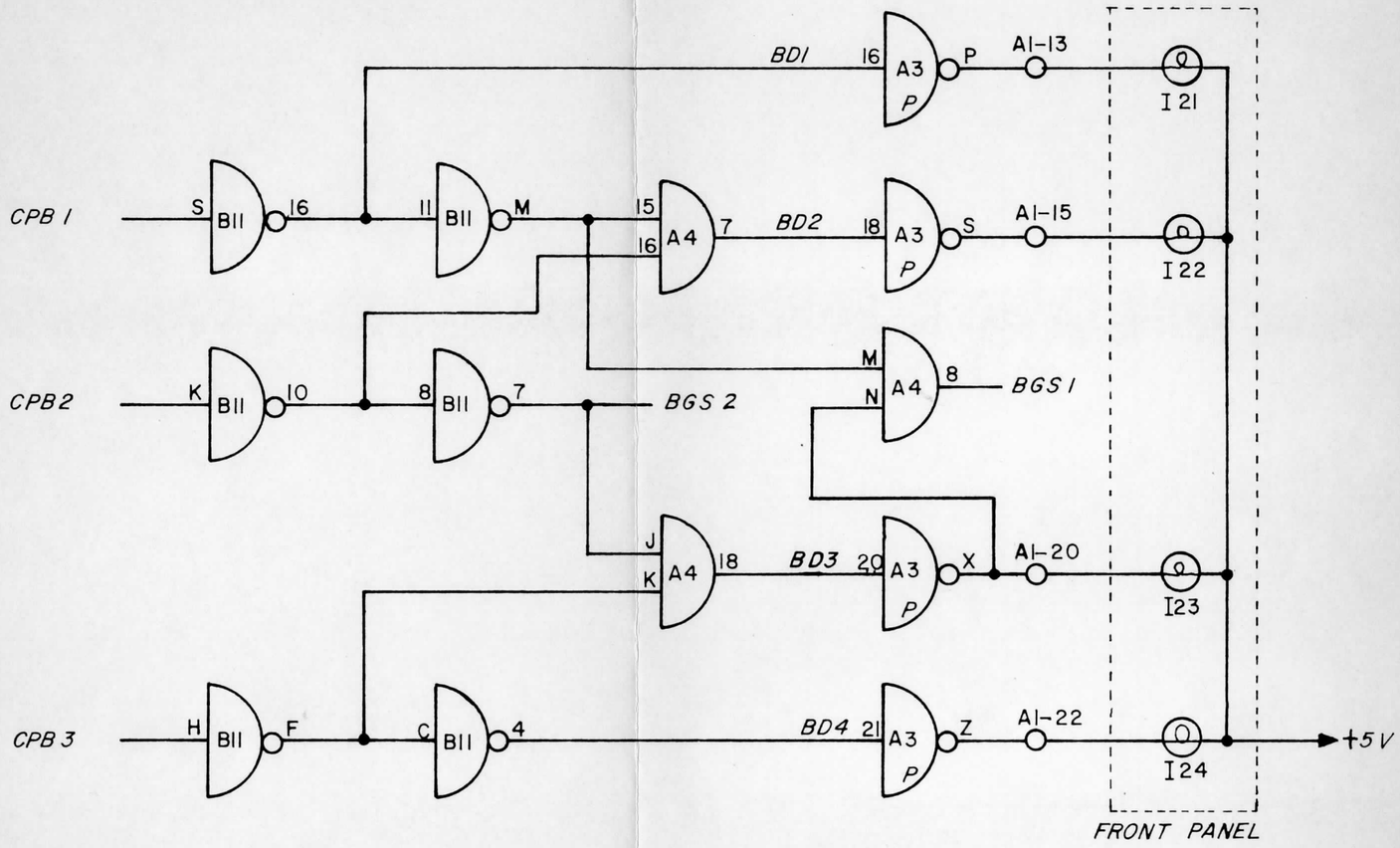
TITLE
COMPARATOR A OUTPUT GATING

SCALE	DRAFTSMAN / DATE	CHECKER / DATE	ENGINEER / DATE
N/A	RWN 2-26-68		J.C.S. 2-23-68
APPROVAL / DATE	DESIGN ACTIVITY APPROVAL / DATE	ADDITIONAL APPROVAL / DATE	
PROJECT NO 1306	SIZE B	SHEET 1 OF 1	DRAWING NO 1306A017A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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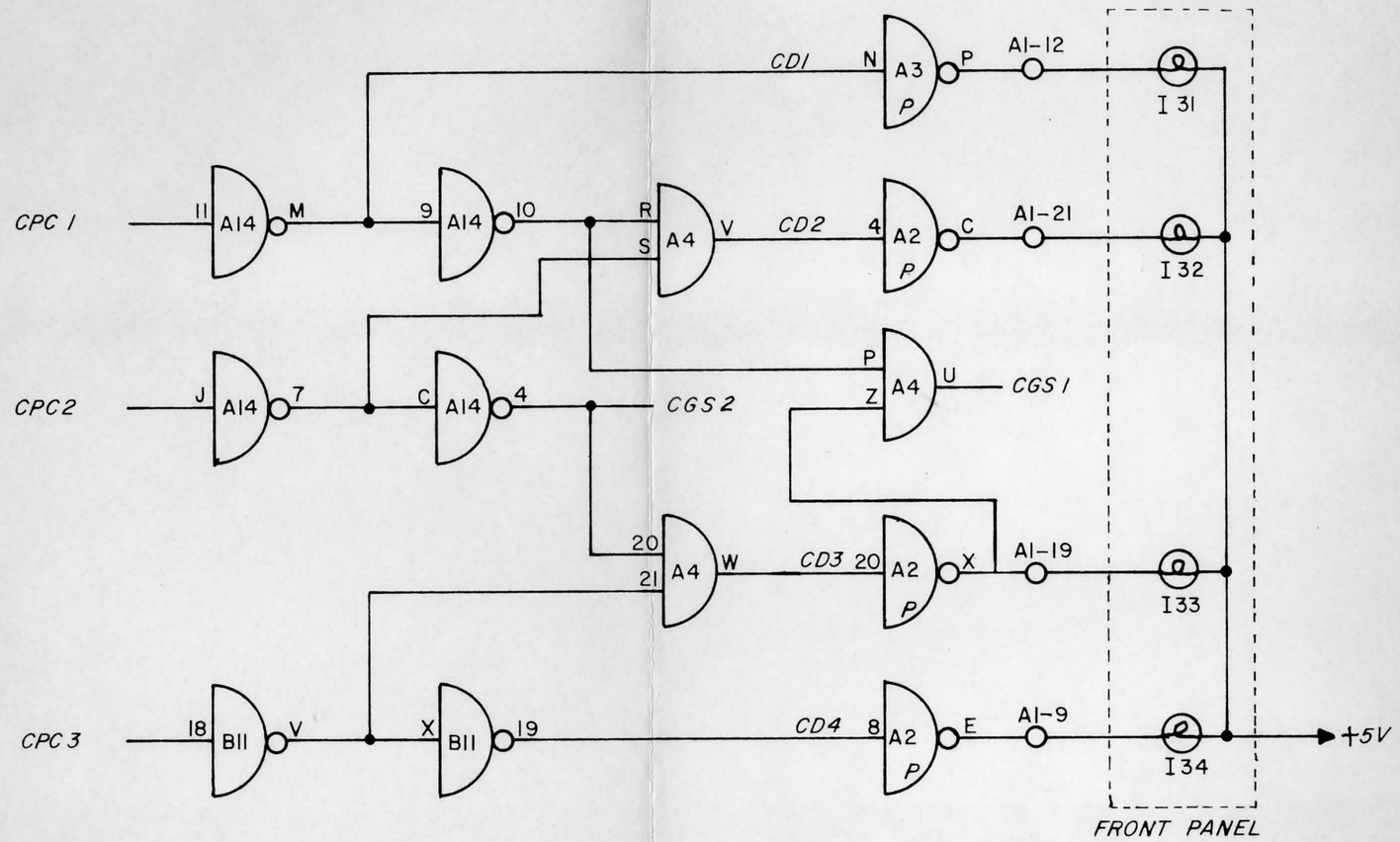
TITLE
COMPARATOR B OUTPUT GATING

SCALE	DRAFTSMAN / DATE	CHECKER / DATE	ENGINEER / DATE
N/A	RWR 2-26-68		J.C.S. 2-23-68
APPROVAL / DATE	DESIGN ACTIVITY APPROVAL / DATE	ADDITIONAL APPROVAL / DATE	
PROJECT NO. 1306	SIZE B	SHEET 1 OF 1	DRAWING NO. 1306A018A

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED



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TITLE

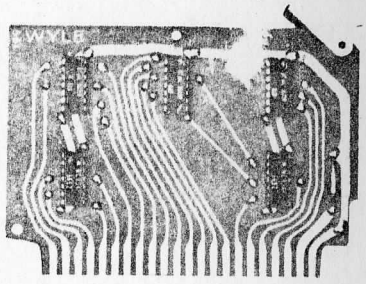
COMPARATOR C OUTPUT GATING

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
N/A	RWD	2-26-68			J.C.S.	2-23-68

APPROVAL	DATE	DESIGN ACTIVITY APPROVAL	DATE	ADDITIONAL APPROVAL	DATE

PROJECT NO	SIZE	SHEET	DRAWING NO.
1306		1 of 1	1306A019A

AND GATES



Nine 3-input AND gates
Two inverters

Application — General-purpose gating

Specifications (AND gates)

Frequency:	DC to 5 mc
Input loading:	1 unit load each input
Noise rejection:	750 millivolts, typical, at logic 0 1.5 volts, typical, at logic 1
Input/output levels:	
Logic 1:	+ 4 ± 1 volts
Logic 0:	+ 0.2 ± 0.2 volt
Propagation delay (see Note):	
Output positive-going:	28 ns, typical; 60 ns, maximum
Output negative-going:	46 ns, typical; 80 ns, maximum
Output drive capability:	8 unit loads
Power requirements:	+ 5 ± 0.5 volts at 70 milliamps, maximum
Operating temperature, ambient:	0°C. to + 70°C.
Storage temperature range:	-55°C. to + 125°C.
Circuit operation:	Output is logic 1 only if all inputs are logic 1. Output is logic 0 if one or more inputs are logic 0. Inputs left open simulate logic 1 states.

Note: Measured at 1.5 volts with output driving 8 unit loads and 40 picofarads. For decreased loads, turn-off (output positive-going) delay will increase. Minimum delay can be restored by addition of pull-up resistors.

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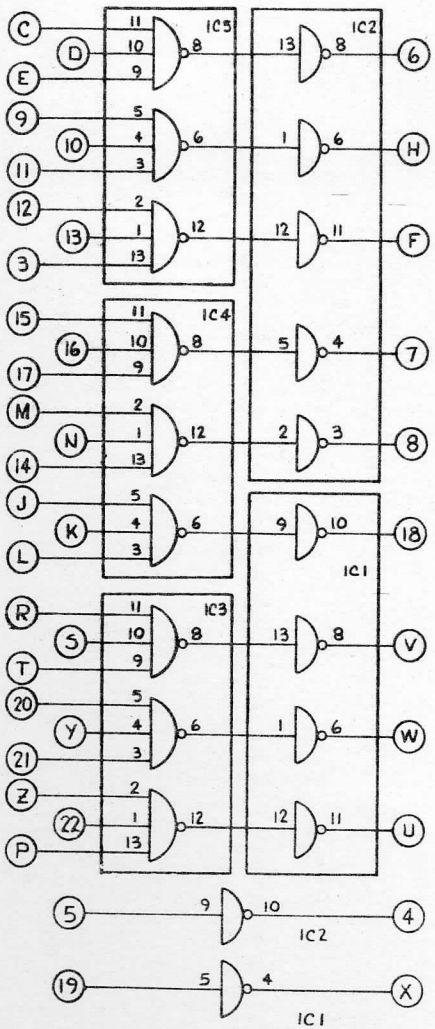
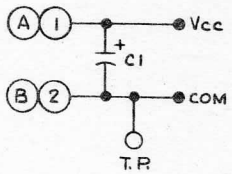
LOGIC DIAGRAM

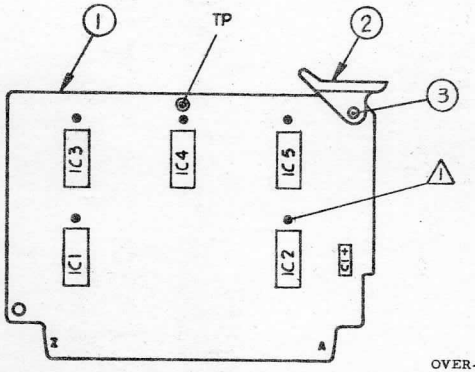




⚠1 INDICATES NOTCHED END OF IC MODULE

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LAYOUT



MECHANICAL SPECIFICATIONS

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED 44-PIN (.0156" CENTERS)

PARTS LIST

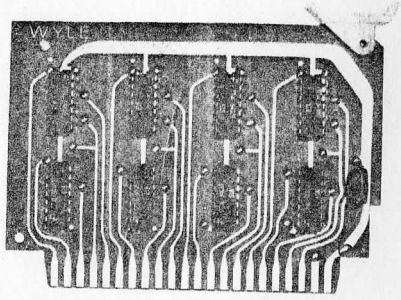
ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
6	2	A12099	IC MODULE, TYPE: WIC 711	IC1, IC2	AVL 165
5	3	A12010	IC MODULE, TYPE: WIC 706	IC3-IC5	AVL 109
4	1	69C108-105	CAPACITOR, 1 MFD., 35V	C1	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-42	EXTRACTOR-CARD		
1	1	B11961	PROCESS BOARD CODE 661		

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM.	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR = ±1/2° XX = ±.03 1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	"THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES."	SCALE 1/1	DRAWN BY NAME Sol Bunnett DATE 1-7-67	CHKD BY W. Larson 1-20-67	PROJ ENGR C.F. Muller 1-24-67
	WYLE LABORATORIES PRODUCTS DIVISION EL SEGUNDO, CALIF.	TITLE ASSY MAG-9 9-3 INPUT NAND GATES AND 2 INVERTERS	DRAWING NO. C12320	REV. A	

MAG-9

BINARY DECODER

One 4-bit binary decoder



Application — Conversion of 4-bit binary word to 1-out-of-16 lines code

Specifications

Frequency:	DC to 5 mc
Input loading (see Note 1):	8 unit loads each input
Input/output levels:	
Logic 1:	+ 4 ± 1 volts
Logic 0:	+0.2 ± 0.2 volt
Propagation delay (see Note 2):	
Output positive-going:	40 ns, typical; 50 ns, maximum
Output negative-going:	12 ns, typical; 30 ns, maximum
Output drive capability:	8 unit loads
Power requirements:	+ 5 ± 0.5 volts at 52 milliamps, maximum
Operating temperature, ambient:	0°C. to + 70°C.
Storage temperature range:	-55°C. to + 125°C.
Circuit operation:	Output line corresponding to binary input is at logic 0; remaining 15 outputs are at logic 1. Inputs left open simulate logic 1 states.

Note 1: True and false inputs are required for each bit of BCD data.

Note 2: Measured at 1.5 volts with output driving 8 unit loads and 40 picofarads. For decreased loads, turn-off (output positive-going) delay will increase. Minimum delay can be restored by addition of pull-up resistors.

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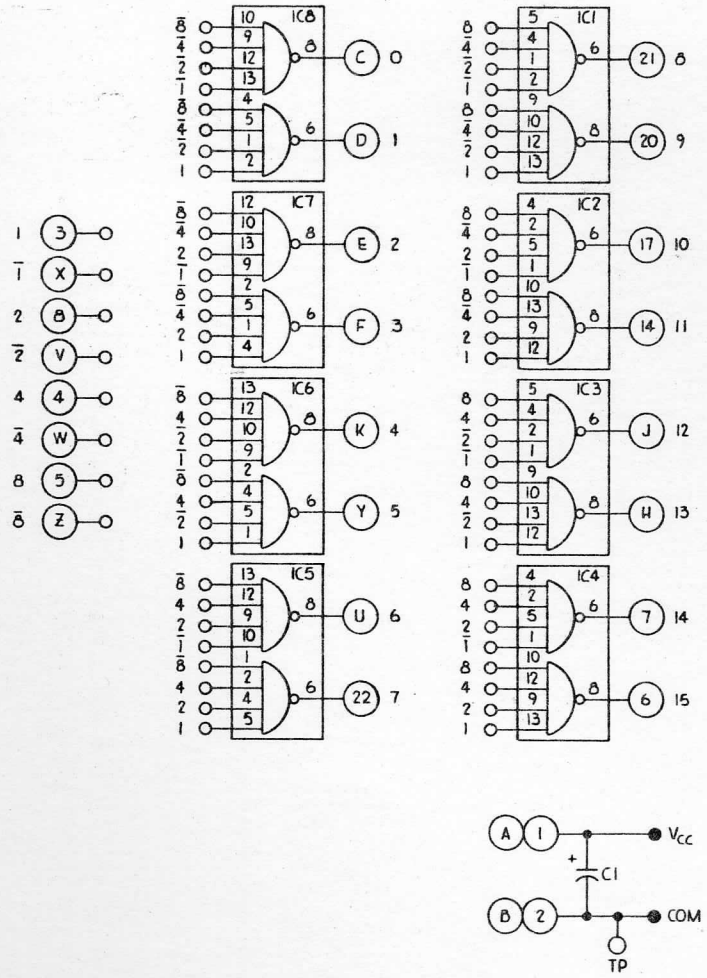
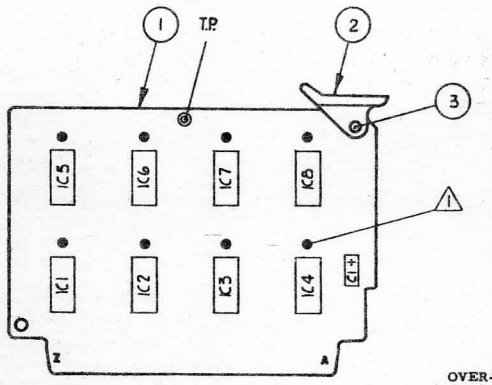
LOGIC DIAGRAM



PARTS LAYOUT



MECHANICAL SPECIFICATIONS

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED 44-PIN (.0156" CENTERS)

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
5	8	A12005	IC MODULE, TYPE: WIC 701	IC1 - IC8	AVL 104
4	1	69C108-105	CAPACITOR, 1 MFD, 35V	C1	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-59	EXTRACTOR-CARD		
1	1	B11957	PROCESS BOARD CODE 657		

PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM.	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.03	"THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES."	SCALE 1/1	DRAWN BY NAME Morrison DATE 6 Jan 67	CHKD BY Richmond 20 FEB 67	PROJ ENGR CR Muller 2-20-67

1. DO NOT SCALE THE DRAWING
2. ALL DIMENSIONS ARE IN INCHES
3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT
4. BREAK ALL SHARP EDGES .010 R. APPROX.

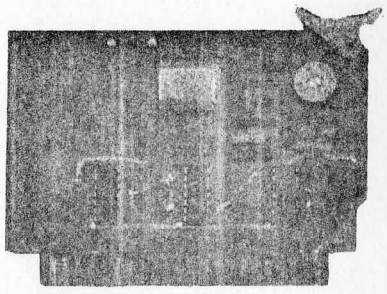
WYLE LABORATORIES
PRODUCTS DIVISION
EL SEGUNDO, CALIF.

TITLE: ASSY. MBD-1 4 BIT TO 16 LINE DECODER

DRAWING NO. C 12317 REV. A

MBD-1

⚠1 INDICATES NOTCHED END OF MODULE.
NOTES: UNLESS OTHERWISE SPECIFIED



CRYSTAL OSCILLATOR

One crystal-controlled oscillator circuit

Application — Precision clock source

Specifications

Frequency:	
Buffered (Pins 15, 21):	100 kc square wave (±0.001% at +25°C.)
Unbuffered (Pins 3, 4, 10):	200 kc square wave (±0.001% at +25°C.)
Stability:	±0.01% (0°C. to +70°C.)
Output levels:	
Logic 1:	+4 ±1 volts
Logic 0:	0.2 ±0.2 volt
Output drive capability:	
Pin 3:	8 unit loads
Pin 4:	7 unit loads
Pin 10:	5 unit loads
Pins 15, 21:	25 unit loads
Power requirements:	+5 volts ±0.5 volts at 35 milliamps, maximum
Operating temperature, ambient:	0°C. to +70°C.
Storage temperature range:	-55°C. to +125°C.
Circuit operation:	The crystal-controlled oscillator circuit is connected via NAND gates to a J-K flip-flop which divides the crystal frequency by two and generates a symmetrical square wave. The true and false outputs of the flip-flop are each connected to a 3-input buffer driver. The buffer drivers may be inhibited separately or simultaneously.

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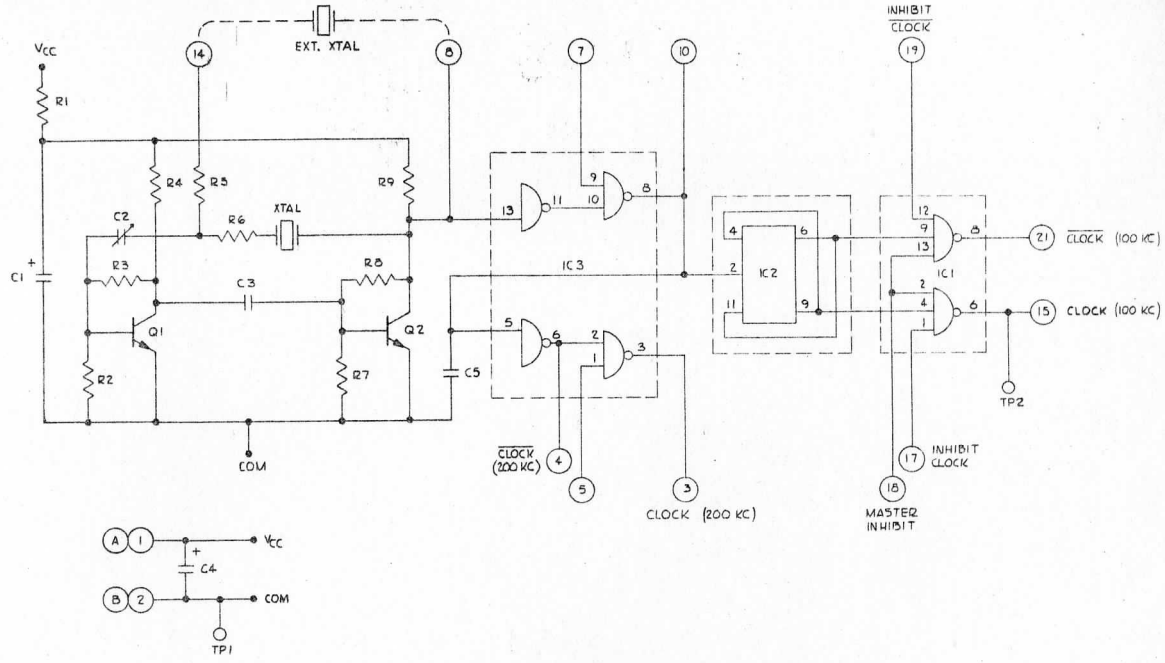
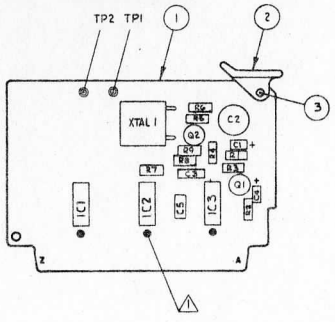
SCHEMATIC DIAGRAM



MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX – ±.010 ANGULAR ±1/2° XX – ±.03	"THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES."	SCALE	DRAWN BY	CHKD BY	PROJ ENGR
1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	WYLE LABORATORIES PRODUCTS DIVISION EL SEGUNDO, CALIF.	FULL NAME DATE 7-27-66	W. Carson 7-27-66	7-27-66	7/27/66
		TITLE ASSY. MCO-1 100 KC CRYSTAL OSCILLATOR		DRAWING NO. C11878 SH 1 OF 2	B REV

1.
NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LAYOUT



MECHANICAL SPECIFICATIONS

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED 44-PIN (.0156" CENTERS)

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION(S)	VENDOR CODE
16	1	69C100-330	CAPACITOR 33 PF	C5	AVL 110
15	1	76C108	CRYSTAL	XTAL	AVL 141
14	2	75A110	TRANSISTOR, 2N3646	Q1,2	AVL 115

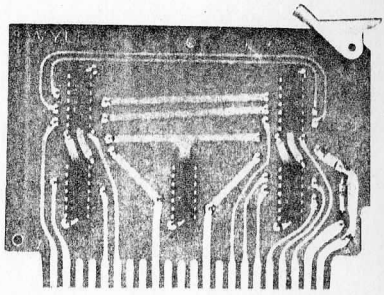
ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION(S)	VENDOR CODE
13	2	70C112-104	RESISTOR, 100 K 1/4 W, 5%	R2,7	AVL 186
12	2	70C112-473	RESISTOR, 47 K 1/4 W, 5%	R3,8	AVL 186
11	4	70C112-152	RESISTOR, 1.5K 1/4 W, 5 %	R4,5,6,9	AVL 186
10	1	70C112-101	RESISTOR, 100 OHM 1/4 W, 5 %	R1	AVL 186
9	1	A12008	IC MODULE, TYPE WIC 704	IC2	AVL 107
8	1	A12007	IC MODULE, TYPE WIC 703	IC 3	AVL 106
7	1	A12006	IC MODULE, TYPE WIC 702	IC 1	AVL 105
6	1	69C101-222	CAPACITOR, .0022 MFD	C 3	AVL 111
5	1	69C118	CAPACITOR - VARIABLE, 5-25 PF	C 2	AVL 140
4	2	69C108-105	CAPACITOR, 1 MFD, 35V	C1,4	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-21	EXTRACTOR-CARD		
1	1	B11939	PROCESS BOARD, CODE 639		

PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX – ±.010 ANGULAR ±1/2° XX – ±.03	"THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES."	SCALE	DRAWN BY	CHKD BY	PROJ ENGR
1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	WYLE LABORATORIES PRODUCTS DIVISION EL SEGUNDO, CALIF.	FULL NAME DATE 7-26-66	W. Carson 7-26-66		
		TITLE ASSY. MCO-1 100 KC CRYSTAL OSCILLATOR		DRAWING NO. C11878 SH 2 OF 2	B REV

⚠ INDICATES NOTCHED END OF IC MODULE.
NOTES: UNLESS OTHERWISE SPECIFIED

DIGITAL SCANNER



One 4-digit scanner
Two inverters

Applications — Multiplexing of four 4-bit data words

Specifications

Inverters:	See MIA-18 specification
Scanner:	
Frequency:	DC to 5 mc
Input loading:	
Data Input:	1 unit load
Data Transfer Input:	4 unit loads
Input/Output levels:	
Logic 1:	+ 4 ± 1 volts
Logic 0:	+ 0.2 ± 0.2 volt
Propagation delay (see Note 1):	
Output positive-going:	40 ns, typical; 45 ns, maximum
Output negative-going:	10 ns, typical; 20 ns, maximum
Data Transfer pulsewidth:	100 ns, minimum
Output drive dapability:	8 unit loads
Power requirements:	+ 5 ± 0.5 volts at 88 milliamps, maximum
Operating temperature, ambient:	0°C. to + 70°C.
Storage temperature range:	-55°C. to + 125°C.
Circuit operation:	The scanner acts as a four-pole, four-position switch. Four Data Transfer Inputs are provided as controls to select one out of four 4-bit inputs. Selected Transfer Input is made true; remaining Transfer Inputs must be false. Selected input word is reflected on output lines. Two cards can be interconnected for 8-digit scanning.

Note 1: Measured at 1.5 volts with output driving 8 unit loads and 40 picofarads. For decreased loads, turn-off (output positive-going) delay will increase. Minimum delay can be restored by addition of pull-up resistors.

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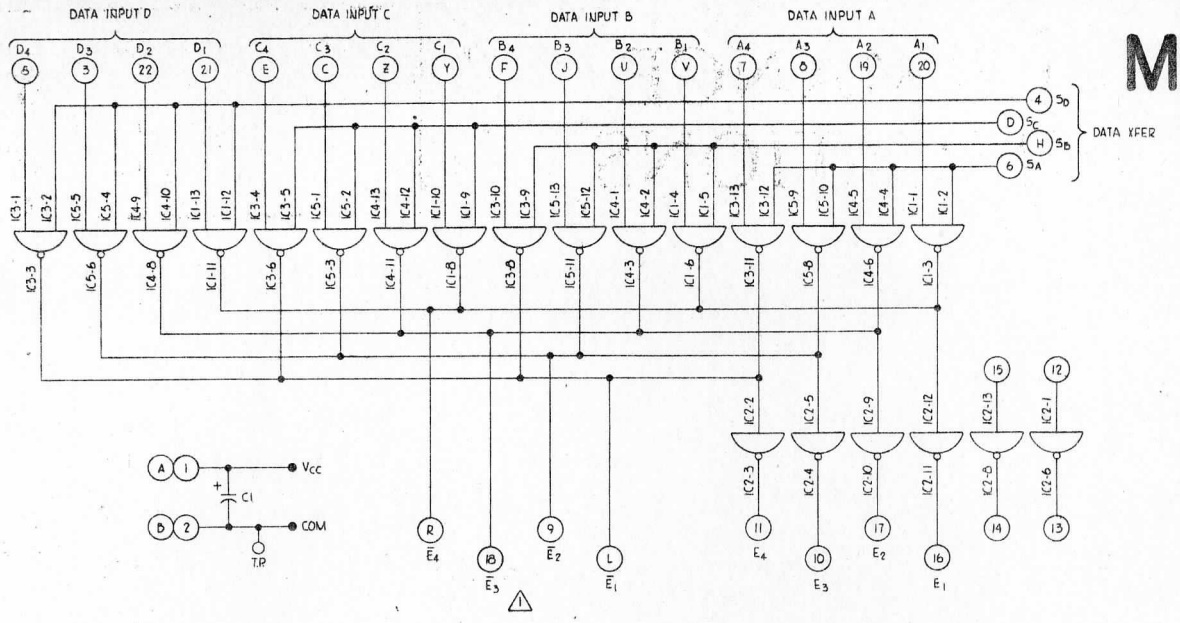

⚠1 8-DIGIT SCANNING IS ACCOMPLISHED BY CONNECTING THE $\bar{E}_1\bar{E}_2\bar{E}_3$ AND $\bar{E}_4$ OUTPUTS OF ONE MDS-4 CARD TO THE $\bar{E}_1\bar{E}_2\bar{E}_3$ AND $\bar{E}_4$ OUTPUTS, RESPECTIVELY, OF A SECOND MDS-4 CARD.

NOTES: UNLESS OTHERWISE SPECIFIED

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES ARE AS NOTED LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.03 1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	-THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES-	SCALE NONE NAME DATE	DRAWN BY Watson 3.16.67 CHKD BY	CHKD BY LK 4.5.67 PROJ ENGR R.M.Miller 4-5-67	

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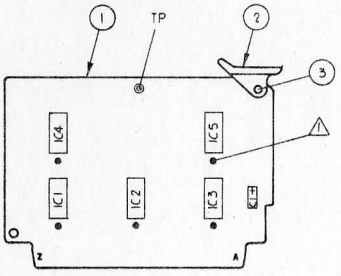
PRODUCTS DIVISION
EL SEGUNDO, CALIF.

TITLE: ASSY. MDS-4
4 DIGIT SCANNER

DRAWING NO. C 12294 REV. B
SH 1 of 2

PARTS LAYOUT



MECHANICAL SPECIFICATIONS

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED 44-PIN (.0156" CENTERS)

MC-834P
DTL 94L

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
6	1	A12099	IC MODULE, TYPE: WIC 711	IC2	AVL 165
5	4	A12007	IC MODULE, TYPE: WIC 703	IC1, IC3-IC5	AVL 106
4	1	69C108-105	CAPACITOR, 1 MFD, 35V	C1	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-51	EXTRACTOR-CARD		
1	1	B11952	PROCESS BOARD CODE 652		

PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES ARE AS NOTED LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.08 1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	-THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES-	SCALE 1/1 NAME DATE	DRAWN BY CHKD BY	CHKD BY PROJ ENGR	

WYLE LABORATORIES
PRODUCTS DIVISION
EL SEGUNDO, CALIF.

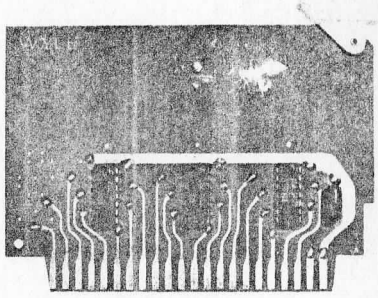
TITLE: ASSY. MDS-4
4 DIGIT SCANNER

DRAWING NO. C 12294 REV. A
SH 2 of 2

⚠ INDICATES NOTCHED END OF MODULE.

NOTES: UNLESS OTHERWISE SPECIFIED

NAND GATES



Twelve 2-input NAND gates

Applications — NAND gates, inverters, and DC flip-flops

Specifications

Frequency:	DC to 2 mc
Input loading:	1 unit load each input
Noise rejection:	750 millivolts, typical
Input/output levels:	
Logic 1:	+4 ±1 volts
Logic 0:	+0.2 ±0.2 volt
Propagation delay (see Note):	
Output negative-going:	40 ns, typical; 50 ns, maximum
Output negative-going:	12 ns, typical; 30 ns, maximum
Output drive capability:	8 unit loads
Power requirements:	+5 ±0.5 volts at 46 milliamps, maximum
Operating temperature, ambient:	0°C. to +70°C.
Storage temperature range:	-55° C. to 125° C.
Circuit operation:	Output is logic 1 if either or both inputs is logic 0. Output is logic 0 only if both inputs are logic 1. Inputs left disconnected simulate logic 1 states.

Note: Measured at 1.5 volts with output driving 8 unit loads and 40 picofarads. For decreased loads, turn-off (output positive-going) delay will increase. Minimum delay can be restored by addition of pull-up resistors.

Specifications are subject to change without notice.

RC-1010-IC-0666

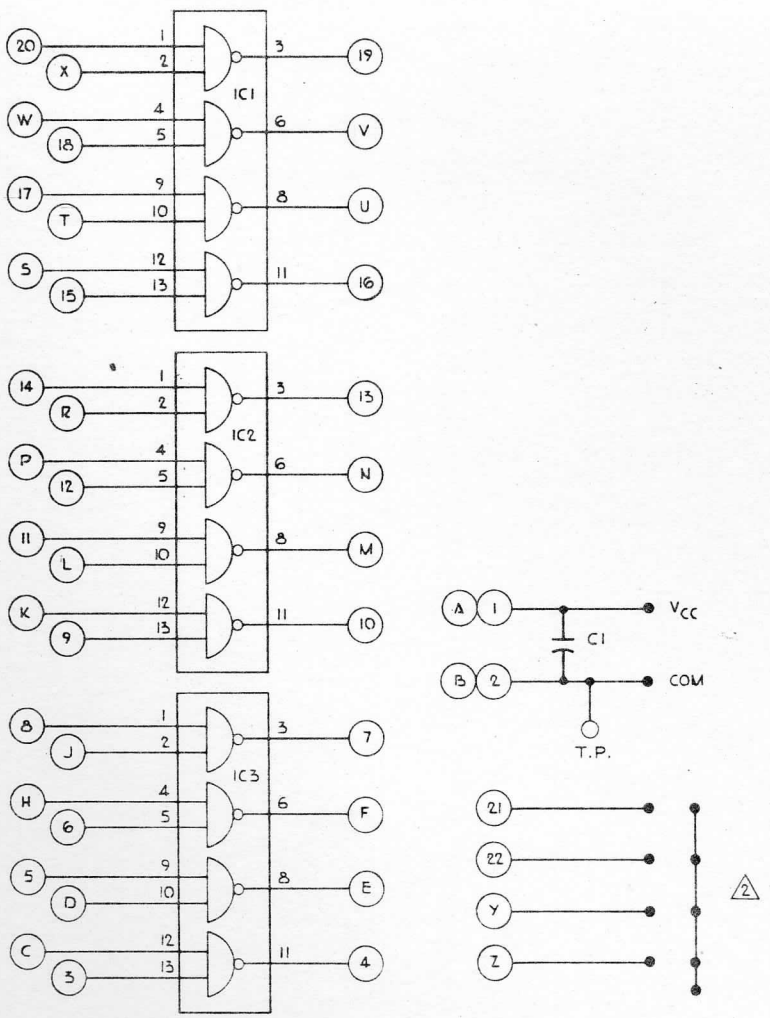
Wyle can supply all associated power supplies and mounting hardware.

(See Reverse)

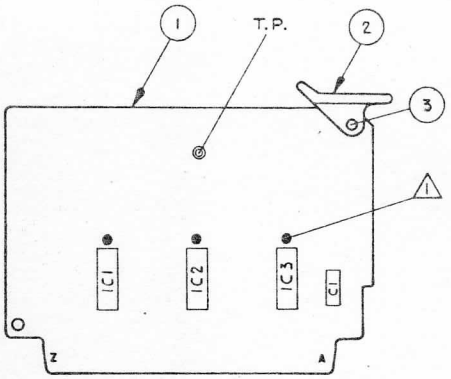
2.19

REVISIONS					
LTR	DESCRIPTION	ECN	DRN	APP	DATE
A	PRODUCTION RELEASE	2375	WC	JDS	9/4/66

LOGIC DIAGRAM



PARTS LAYOUT



C11999 A

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
5	1	69C103-104	CAPACITOR .1MFD	C1	AVL 103
4	3	A12007	IC MODULE TYPE WIC - 703	IC1, IC2, IC3	AVL 106
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-18	EXTRACTOR - CARD		
1	1	B11845	PROCESS BOARD CODE 621		

PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM.	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.03	THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES.	SCALE 1/1	DRAWN BY NAME H. DITTMAR DATE 4-25-66	CHKD BY 5-18-66	PROJ ENGR 5-19-66

1. DO NOT SCALE THE DRAWING
2. ALL DIMENSIONS ARE IN INCHES
3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT
4. BREAK ALL SHARP EDGES .010 R APPROX.

WYLE LABORATORIES
PRODUCTS DIVISION
EL SEGUNDO, CALIF.

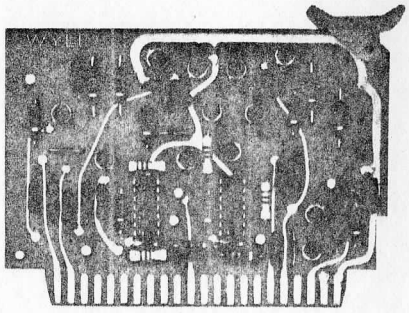
TITLE: ASSY. MNG-12
12 NAND GATES

DRAWING NO. C11999 REV A

⚠2 INDICATES CIRCUITRY AVAILABLE FOR OPTIONAL COMPONENTS, e.g., PULL UP RESISTORS OR GATE EXPANDERS.
⚠1 INDICATES NOTCHED END OF MODULE.
NOTES: UNLESS OTHERWISE SPECIFIED

MNG-12

MONOSTABLE MULTIVIBRATORS



Four fixed one-shot circuits (MOF-4)
Two fixed one-shot circuits (MOF-2)

Application — To generate single pulses with pulse width determined by fixed RC network on card

Specifications

Input loading (see Note 1):	3 unit loads plus 100 pf to common
Noise rejection:	1 volt, typical
Trigger transition time required (negative-going):	125 ns, or faster
Input/output levels:	
Logic 1:	+ 4 ± 1 volts
Logic 0:	+ 0.2 ± 0.2 volt
Propagation delay (see Note 2):	120 ns, typical; 150 ns, maximum
Output drive capability:	8 unit loads
Power requirements:	+ 5 ± 0.5 volts at 30 milliamps, maximum
Nominal pulse width:	1.0 microsecond
Minimum pulse width (with external capacitor):	10 seconds (see Note 3)
Minimum pulse recovery time:	15% of pulse width, typical
Pulse width adjustment range:	None
Operating temperature, ambient:	0°C. to + 70°C.
Circuit operation:	Circuits are triggered by a level change on the input of logic 1 to logic 0.

Note 1: When driven from standard integrated circuit gate, 100 pf of input load degrades input fall time by approximately 20 nanoseconds.

Note 2: Measured at 1.5 volts with output driving 8 unit loads and 40 picofarads. For decreased loads, turn-off (output positive-going) delay will increase. Minimum delay can be restored by addition of pull-up resistors.

Note 3: Where delay is extended by addition of external capacitor, approximately 100 pf is required for each microsecond of additional delay.

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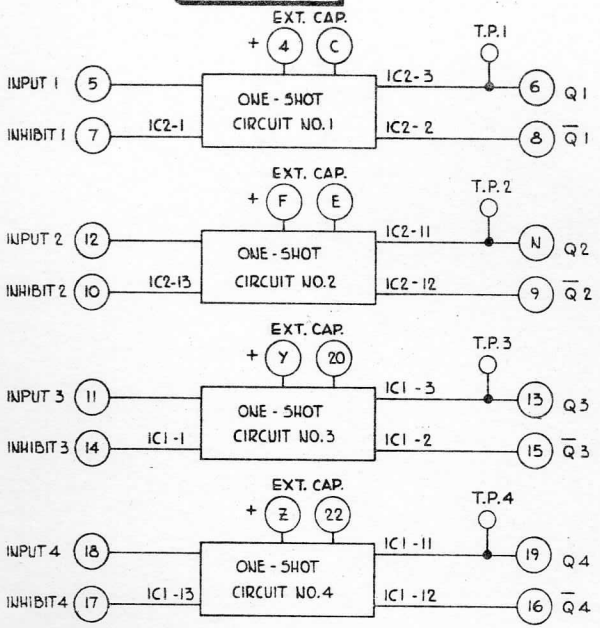
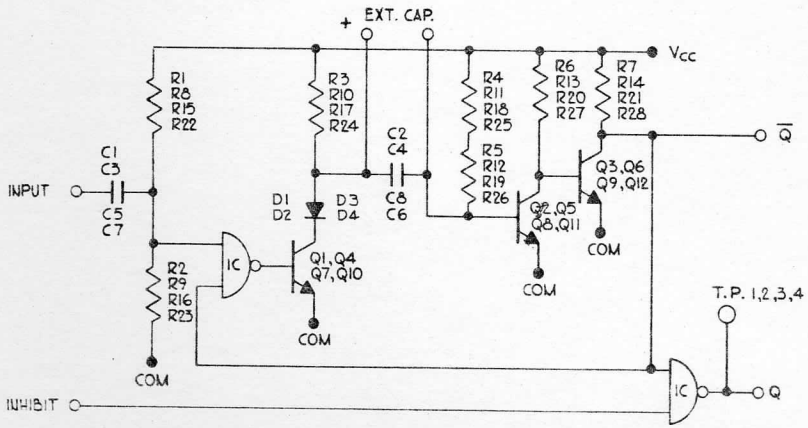
LOGIC DIAGRAM

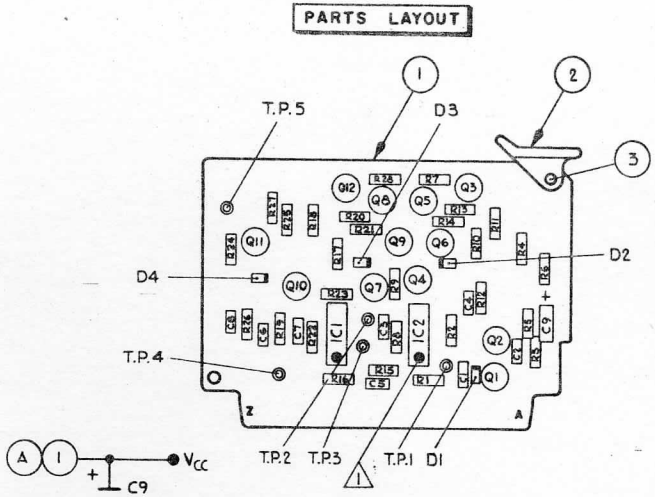


TYPICAL ONE-SHOT CIRCUIT



⚠1 INDICATES NOTCHED END OF IC MODULE.
NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LAYOUT



MECHANICAL SPECIFICATIONS

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED 44-PIN (.0156" CENTERS)

For MOF-2, components for One-Shot Circuits Three and Four are deleted from the card. See Wyle Drawing C12323.

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
16	4	75A118	TRANSISTOR, 2N3643	Q3,6,9,12	AVL 143
15	4	70C102-562	RESISTOR, 5.6 K 1/4W, 5%	R5,12,19,26	AVL 102
14	8	A12387-50	TRANSISTOR 2N3646-50	Q1,2,4,5,7,8,10,11	AVL 115
13	4	A11717	DIODE. TYPE WSD200	D1-4	AVL 118
12	8	70C112-562	RESISTOR, 5.6K 1/4W, 5%	R6,7,13,14,20,21,27,28	AVL 186
11	4	70C102-103	RESISTOR, 10 K 1/4W, 5%	R4,11,18,25	AVL 102
10	4	70C112-102	RESISTOR, 1K 1/4W, 5%	R3,10,17,24	AVL 186
9	4	70C112-222	RESISTOR, 2.2K 1/4W, 5%	R2,9,16,23	AVL 186
8	4	70C112-332	RESISTOR, 3.3K 1/4W, 5%	R1,8,15,22	AVL 186
7	2	A12007	IC MODULE, TYPE WIC-703	IC1, IC2	AVL 106
6	4	69C100-820	CAPACITOR, 82 Pf	C2,4,6,8	AVL 110
5	4	69C100-101	CAPACITOR, 100 Pf	C1,3,5,7	AVL 110
4	1	69C108-105	CAPACITOR, 1MFD 35V	C9	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-15	EXTRACTOR-CARD		
1	1	B11935	PROCESS BOARD CODE 635		

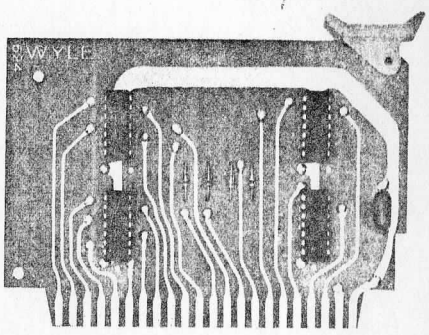
PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM.	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.03	"THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES."	SCALE 1/1	DRAWN BY H.DITTMAR	CHKD BY C.R.Mueller	PROJ ENGR C.R.Mueller
1. DO NOT SCALE THE DRAWING		NAME			
2. ALL DIMENSIONS ARE IN INCHES		DATE 5.26.66	6.15.66	7.16.66	
3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT	WYLE LABORATORIES PRODUCTS DIVISION EL SEGUNDO, CALIF.	TITLE ASSY. MOF-4 4 FIXED ONE-SHOTS		DRAWING NO. C12091	REV. D
4. BREAK ALL SHARP EDGES .010 R. APPROX.					

MOF-4

POWER NAND GATES

Three 2-input power NAND gates
Two 2-input power NAND gates with nodes
One 3-input power NAND gate with node
Two 4-input power NAND gates with nodes
Two 2-input diode gate expanders



Applications — Interface drivers, output level shifters, lamp drivers, NAND gates, inverters, and DC flip-flops, where output drive capability of standard NAND gate is inadequate

Specifications

Frequency:	DC to 5 mc
Input loading:	1 unit load each input
Noise rejection:	750 millivolts, typical, at logic 0 1 volt, typical, at logic 1
Fan-In (see Note 1):	12
Input levels:	
Logic 1:	+ 4 ± 1 volts
Logic 0:	+ 0.2 ± 0.2 volt
Output levels:	See Note 2
Propagation delay:	See Note 2
Output drive capability (with external resistor R=2000 ohms to Vcc=+5 vdc):	25 unit loads (see Note 2)
Power requirements:	+5 ± 0.5 volts at 96 milliamps, max., at no load
Operating temperature, ambient:	0°C. to + 70°C.
Storage temperature range:	-55°C. to + 125°C.
Circuit operation:	Output is logic 1 if one or more inputs is logic 0. Output is logic 0 only if all inputs are logic 1. Inputs left disconnected simulate logic 1 states. External resistors should be used with these gates.

Note 1: Where a node is provided, the number of inputs can be increased by use of diode gate expanders.

Note 2: For complete specifications for output levels, drive capability, and propagation delay, refer to Fairchild specification for DTμL 944.

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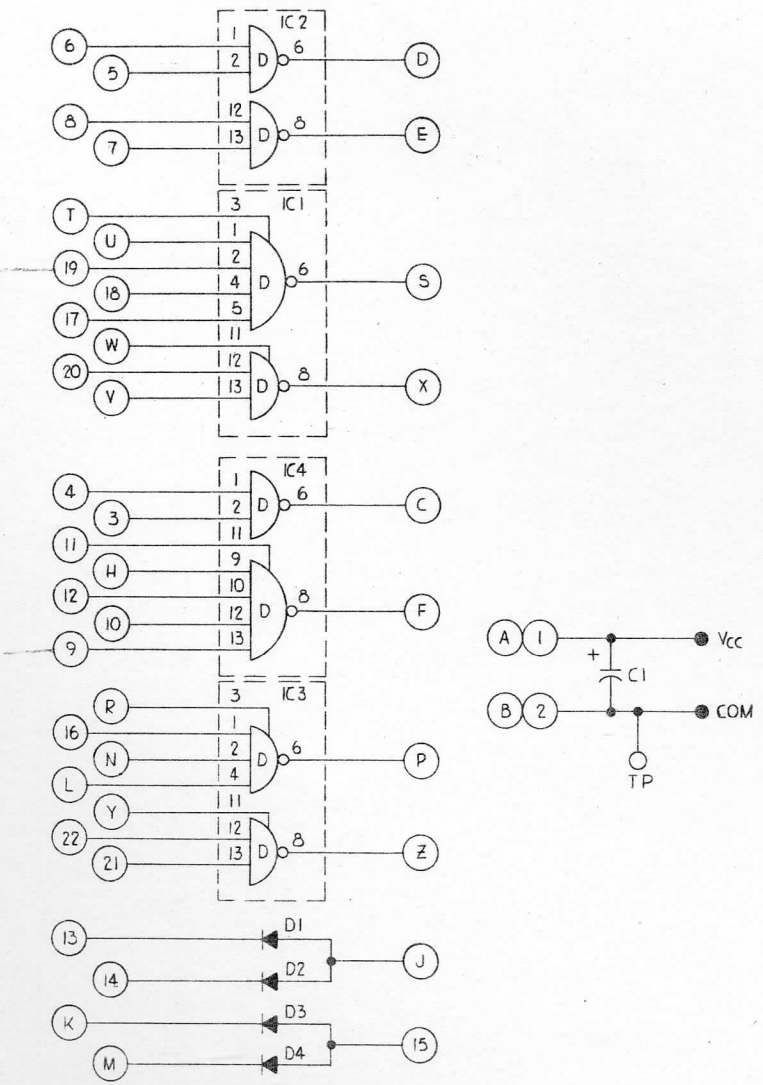
LOGIC DIAGRAM

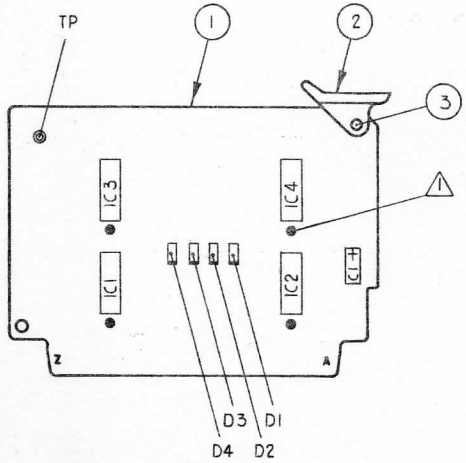


2. "D" INSIDE LOGIC SYMBOL INDICATES THAT COLLECTOR RESISTOR IS OMITTED FROM IC GATE.

⚠1 INDICATES NOTCHED END OF IC MODULE.

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LAYOUT



MECHANICAL SPECIFICATIONS

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED 44-PIN (.0156" CENTERS)

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
6	4	A12391	IC MODULE, TYPE: WIC 713	IC1-IC4	AVL 182
5	4	A11717	DIODE, TYPE: WSD 200	D1-D4	AVL 118
4	1	69C108-105	CAPACITOR, 1MFD, 35V	C1	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-71	EXTRACTOR-CARD		
1	1	B11924	PROCESS BOARD CODE 624		

PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM.	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.03 1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	"THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES."	SCALE 1/1	DRAWN BY	CHKD BY	PROJ ENGR
	WYLE LABORATORIES PRODUCTS DIVISION EL SEGUNDO, CALIF.	NAME			
		DATE 5 MAY 67	8 MAY 67	6-7-67	
	TITLE ASSY. MPG-8 8 POWER GATES	DRAWING NO. C 12452	REV. A		

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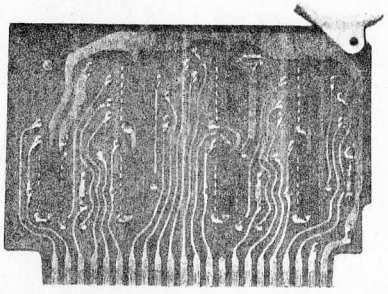
SHIFT REGISTERS



Two 4-bit gated shift registers
Two 2-input power NAND gates

Applications — Parallel-to-serial conversion, serial-to-parallel conversion, and recirculating registers

Specifications

Power NAND gates:	See specifications for MBD-8
Shift registers:	
Shift frequency:	DC to 5 mc
Input loading:	
Shift Clock:	12 unit loads per 4-bit register
Parallel Data Input:	1 unit load per stage
Parallel Data Transfer:	4 unit loads per 4-bit register
DCO (Reset):	12 unit loads per 4-bit register
Serial Input:	2 unit loads per 4-bit register
Input/output levels:	
Logic 1:	$+4 \pm 1$ volts
Logic 0:	$+0.2 \pm 0.2$ volt
Shift Clock pulse width:	30 ns, minimum
Data Transfer pulse width:	30 ns, minimum
DCO pulse width:	30 ns, minimum
Output drive capability:	15 unit loads
Power requirements:	$+5 \pm 0.5$ volts at 175 milliamps, maximum
Operating temperature, ambient:	0°C. to $+70^{\circ}$C.
Storage temperature range:	-55°C. to $+125^{\circ}$C.

Circuit operation:

A stage is set when Transfer goes to logic 1 with Parallel Data Input at logic 1. One Reset (DCO) line is provided for each 4-bit register. Register is reset either by Reset line going to logic 0 or by suitable number of clock pulses. All flip-flop outputs are available at the connector. Data can be shifted in serially. Registers can be connected in tandem. Two power NAND gates are provided on the card for driving the Reset inputs and Shift Clock. These flip-flops change state on the leading edge of the Shift Clock. To convert to trailing edge triggering, Shift Clock can be driven from buffer driver provided on card. A complete application note is available.

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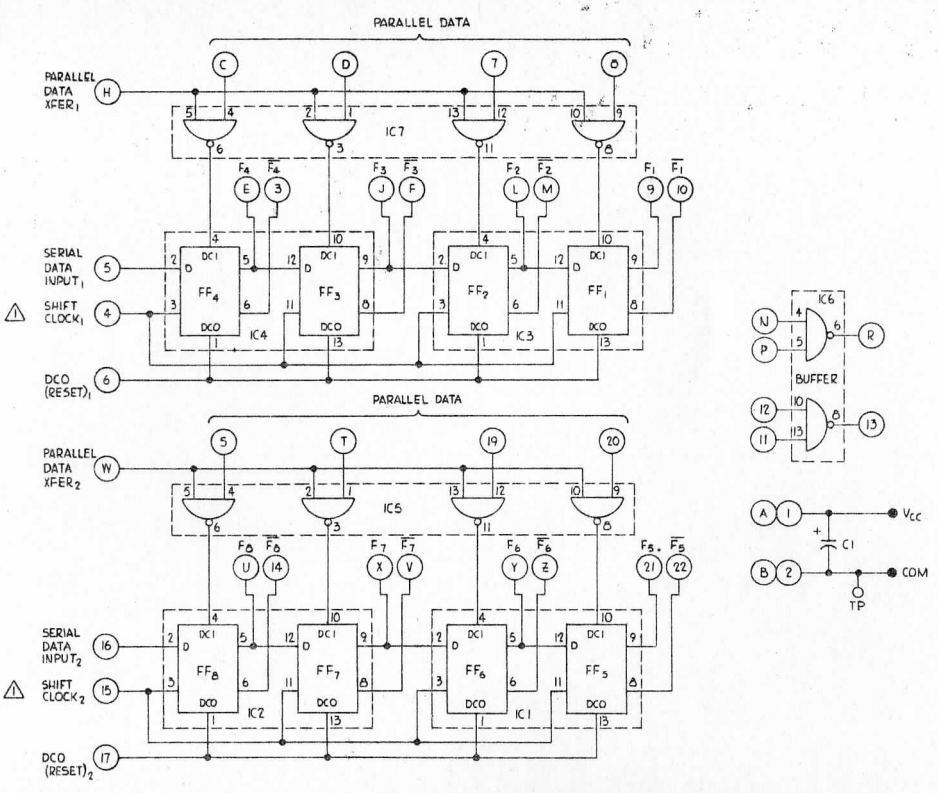


2. DO NOT SHORT FLIP-FLOP OUTPUTS AS ICS USED ARE "TTL" AND MAY BE DAMAGED.

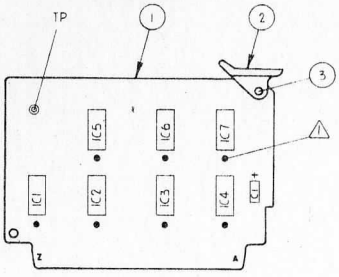
⚠ FLIP-FLOPS CHANGE STATE ON THE POSITIVE TRANSITION OF THE SHIFT CLOCK. USE BUFFER(S) FOR INVERTING SHIFT CLOCK(S)

1. INPUT IF NEGATIVE TRANSITION IS DESIRED.

NOTES: UNLESS OTHERWISE SPECIFIED

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.03	THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES.	SCALE: NONE	DRAWN BY: [illegible] 1.20.67	CHKD BY: [illegible] 4.5.67	PROJ ENGR: [illegible] 4-5-67
1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	WYLE LABORATORIES PRODUCTS DIVISION EL SEGUNDO, CALIF.	TITLE: ASSY. MSR-8 8 BIT SHIFT REGISTER		DRAWING NO: C12,367 SH 1 of 2	A REV.

PARTS LAYOUT



MECHANICAL SPECIFICATIONS

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED 44-PIN (.0156" CENTERS)

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
7	4	A12408	IC MODULE, TYPE WIC 714	IC1 - IC4	AVL 103
6	2	A12007	IC MODULE, TYPE WIC 703	IC5, IC7	AVL 106
5	1	A12006	IC MODULE, TYPE WIC 702	IC6	AVL 105
4	1	69C108-105	CAPACITOR, 1MFD, 35V	C1	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-64	EXTRACTOR-CARD		
1	1	B11965	PROCESS BOARD CODE 665		

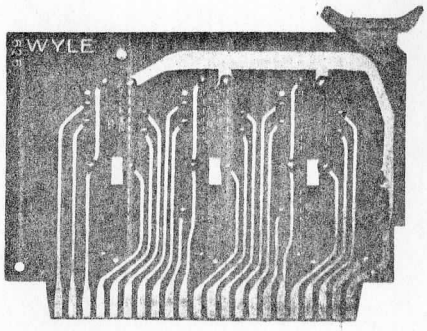
PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR ±1/2° XX = ±.03	THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES.	SCALE:	DRAWN BY:	CHKD BY:	PROJ ENGR
1. DO NOT SCALE THE DRAWING 2. ALL DIMENSIONS ARE IN INCHES 3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT 4. BREAK ALL SHARP EDGES .010 R. APPROX.	WYLE LABORATORIES PRODUCTS DIVISION EL SEGUNDO, CALIF	TITLE: ASSY MSR-8 8 BIT SHIFT REGISTER		DRAWING NO: C12367 SH 2 of 2	A REV.

⚠ INDICATES NOTCHED END OF MODULE.

NOTES: UNLESS OTHERWISE SPECIFIED

FLIP-FLOPS



Five universal flip-flops
One 2-input power NAND gate
One 1-input power NAND gate

Applications — Binary counters, shift registers, storage registers, bi-directional counters, and ring counters

Specifications

Power NAND gates:	See specification for Wyle MBD-8
Flip-flops:	
Frequency:	DC to 5 mc
Input loading:	
DC1 and DC0:	2 unit loads
S_1 and C_1:	2/3 unit load
Clock:	2 unit loads
Noise rejection:	750 millivolts, typical, at logic 0 1 volt, typical, at logic 1
Input/output levels:	
Logic 1:	+ 4 ± 1 volts
Logic 0:	+ 0.2 ± 0.2 volt
Propagation delay (see Note):	
DC1 and DC0 operating:	
Output positive-going:	35 ns, typical; 50 ns, maximum
Output negative-going:	50 ns, typical; 75 ns, maximum
S_1 and C_1 operating:	
Output positive-going:	40 ns, typical; 50 ns, maximum
Output negative-going:	50 ns, typical; 75 ns, maximum
Clock pulse-width:	30 ns, minimum
Output drive capability:	11-1/3 unit loads
Power requirements:	+ 5 ± 0.5 volts at 75 milliamps, maximum
Operating temperature, ambient:	0°C. to + 70°C.
Storage temperature range:	-55°C. to +125°C.

Note: Measured from clock input (negative-going) to either output at 1.5 volts with output driving 12 unit loads and 40 picofarads. For decreased loads, turn-off (output positive-going) delay will increase. Minimum delay can be restored by the addition of pull-up resistors.

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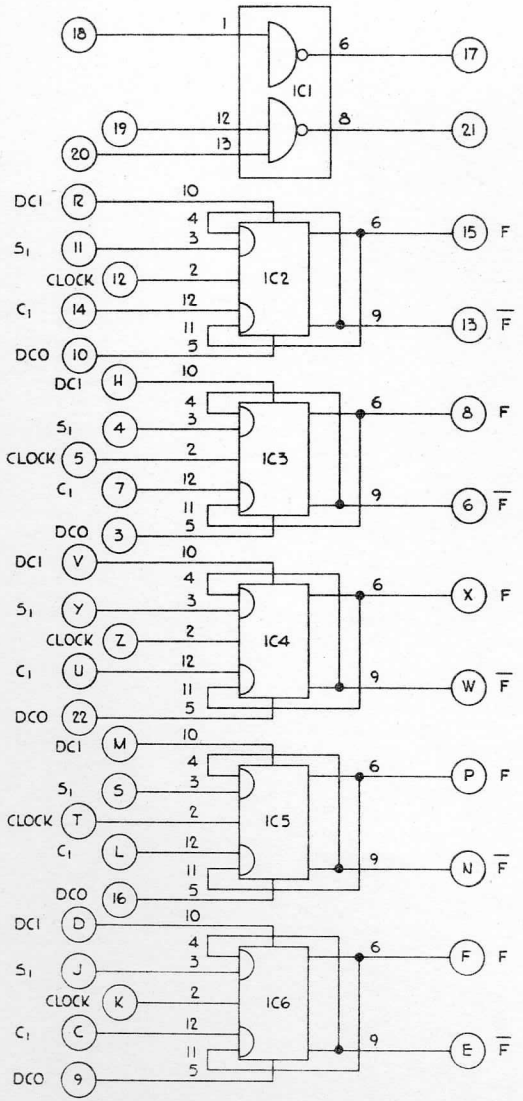
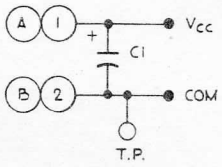
LOGIC DIAGRAM

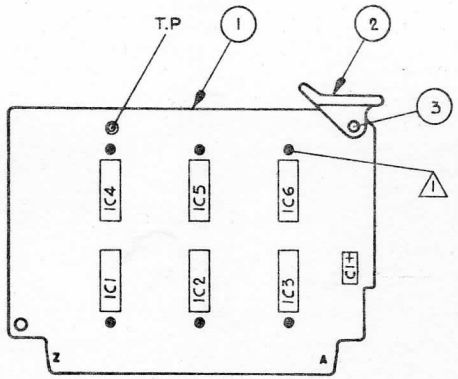


⚠1 INDICATES NOTCHED END OF IC MODULE.

NOTES: UNLESS OTHERWISE SPECIFIED



PARTS LAYOUT



MECHANICAL SPECIFICATIONS

(NOT SHOWN ON PRODUCTION VELLUM)

OVER-ALL BOARD DIMENSIONS:	4-1/2" WIDE, 3-1/4" LONG, 1/16" THICK
ASSEMBLY MOUNTING:	9/16" CENTERS
CONNECTOR:	ETCHED, GOLD-PLATED, 44-PIN (0.156" CENTERS)

ITEM	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION (S)	VENDOR CODE
6	5	A12008	IC MODULE , TYPE WIC-704	IC2-IC6	AVL 107
5	1	A12006	IC MODULE , TYPE WIC-702	IC1	AVL 105
4	1	69C108-105	CAPACITOR, 1MFD, 35V	C1	AVL 132
3	1	23C101-308	SPRING PIN		AVL 117
2	1	C11973-6	EXTRACTOR - CARD		
1	1	B11926	PROCESS BOARD CODE 626		

PARTS LIST

MATERIAL DESCRIPTION	MATERIAL SPECIFICATION	FIRST USED ON	SIMILAR TO	NEXT ASSEM.	MODEL
UNLESS OTHERWISE SPECIFIED TOLERANCES AND NOTES LINEAR XXX = ±.010 ANGULAR ± 1/2° XX = ±.03	THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED FOR MANUFACTURING PURPOSES WITHOUT WRITTEN PERMISSION FROM WYLE LABORATORIES.	SCALE FULL	DRAWN BY NAME H.DITTMAR	CHKD BY W.Gibson	PROJ ENGR C.R.Mueller
1. DO NOT SCALE THE DRAWING			DATE 5-27-66	5-31-66	6-7-66
2. ALL DIMENSIONS ARE IN INCHES					
3. DIMENSIONS APPLY AFTER FINISHING AND HEAT TREATMENT					
4. BREAK ALL SHARP EDGES .010 R. APPROX.					

WYLE LABORATORIES
PRODUCTS DIVISION
EL SEGUNDO, CALIF.

TITLE: ASSY. MUF-5
5 UNIVERSAL FLIP-FLOPS

DRAWING NO. C 11872 REV. B

MUF-5

5.0 REPLACEABLE PARTS LIST

TABLE 5-1 PROCESSOR

Circuit Reference	Description	Manufacturer	
		Name	Part No.
J1, J2, J3	CONNECTOR, BNC, Bulkhead adapter, UG492A/U	Amphenol	31-220
J101-113, J115	CONNECTOR, BNC, Panel jack	Amphenol	17825
	CONNECTOR, BNC, Angle plug	Amphenol	33275
J114	CONNECTOR, Receptacle, Male, 9 contact	Amphenol	165-15
J116,J117,J118	CONNECTOR, Receptacle, Panel, 37 contact	Amphenol	17-10370-1
	CONNECTOR, Printed circuit card, 44 contact	Amphenol	1-67031-0
P114	CONNECTOR, Plug, Female, 9 contact	Amphenol	165-13
P116, P117,P118	CONNECTOR, Plug, 37 contact	Amphenol	17-20370-1
	HOUSING, Cartridge light	Sylvania	SM-1A/300980
	LAMP, Cartridge indicator	Sylvania	905
	LENS, Cartridge, Translucent white	Sylvania	301460
	LENS, Cartridge, Translucent red	Sylvania	301470
	LENS, Cartridge, Translucent blue	Sylvania	301480
	LENS, Cartridge, Translucent green	Sylvania	301490
	MODULE, AND gates	Wyle	MAG-9
	MODULE, NAND gates	Wyle	MNG-12
	MODULE, Power NAND gates	Wyle	MPG-8
	MODULE, Flip-flops	Wyle	MUF-5
	MODULE, Shift registers	Wyle	MSR-8
	MODULE, One-shots, Fixed	Wyle	MOF-4
	MODULE, Crystal oscillator	Wyle	MCO-1
	MODULE, Decoder	Wyle	MBD-1
	MODULE, Scanner	Wyle	MDS-4
	MODULE, A-D converter	SSEC	1306-1A
	MODULE, D-A converter	SSEC	1306-2A
	MODULE, Video amplifier	SSEC	1306-3A
	MODULE, Reference frequency mixer	SSEC	1306-4A
P114	CONNECTOR, Plug, Female, 9 contact	Amphenol	165-13
P116,P117,P118	CONNECTOR, Plug, 37 contact	Amphenol	17-20370-1
S1, S2	SWITCH, Toggle, SPDT, Center off	C & K Components	7103

TABLE 5-2 POWER SUPPLY

Circuit Reference	Description	Manufacturer	
		Name	Part No.
J501	CONNECTOR, Receptacle, Line cord	Switchcraft	AC3C
J502	CONNECTOR, Receptacle, Female, 9 contact	Amphenol	165-16
P502	CONNECTOR, Plug, Male, 9 contact	Amphenol	165-13
F501	FUSE, 1/2 a., 3AG, Slo-blo	Littelfuse	3AG 1/2S
	FUSEHOLDER	Littelfuse	342012
I501	LAMP, Incandescent	GE	328
	LENS, Switch pushbutton	Useco	P-54
A501	MODULE, Power supply, DC, ±15 v., 0.5 a.	Technipower	DP-15.0-0.500
A502	MODULE, Power supply, DC, 5 v., 3 a.	Technipower	PC-5.1-3.0
	MOUNTING ADAPTER, Switch	Electro-Mech	Model 73
S501	SWITCH, Pushbutton, DPDT	Useco	49SCAP

TABLE 5-3 A/D CONVERTER, 1306-1A

Circuit Reference	Description	Manufacturer	
		Name	Part No.
A101, A102	INTEGRATED CIRCUIT, μA710C	Fairchild	U5B771039X
A103, A104			
A105, A106			
A107, A108			
A109			
C101, C102	CAPACITOR, .047 μf., 10%	Sprague	192P-47392
C103			
D101	DIODE, Zener, 1N4735	Motorola	
D102	DIODE, Zener, 1N4743	Motorola	
D103, D104	DIODE, Zener, 1N4742	Motorola	
R101, R102	POTENTIOMETER, 20K, 1/2 w.	Bourns	3067P-1-203
R103, R104			
R105, R106			
R107, R108			
R109			
R110, R111	RESISTOR, 4.3K Ω, 5%, 1/4 w.		
R112	RESISTOR, 47Ω, 5%, 1/4 w.		
R113	RESISTOR, 180Ω, 5%, 1/4 w.		
R114, R115	RESISTOR, 220Ω, 5%, 1/4 w.		
TP101	SOLDER TERMINAL	Cambion	1797-2
	BOARD, Printed circuit	SSEC	1306-1A

TABLE 5-4 D/A CONVERTER, 1306-2A

Circuit Reference	Description	Manufacturer	
		Name	Part No.
C201	CAPACITOR, .0082 µf., ±10%	Sprague	192P82292
C202	CAPACITOR, .047 µf., ±10%	Sprague	192P47392
Q201, Q204	TRANSISTOR, 2N3644	Fairchild	
Q205, Q208			
Q209, Q212			
Q213, Q216			
Q217, Q220			
Q202, Q203	TRANSISTOR, 2N3643	Fairchild	
Q206, Q207			
Q210, Q211			
Q214, Q215			
Q218, Q219			
R201, R203	RESISTOR, 10K Ω, 5%, 1/4 w.		
R206, R208			
R211, R213			
R216, R218			
R221, R223			
R228, R230			
R232, R234			
R202, R204	RESISTOR, 100K Ω, 5%, 1/4 w.		
R205, R207			
R209, R210			
R212, R214			
R215, R217			
R219, R220			
R222, R224			
R225			
R226, R227	RESISTOR, 20K Ω, 5%, 1/4 w.		
R229, R231			
R233, R235			
R236	RESISTOR, 2.4K Ω, 5%, 1/4 w.		
	BOARD, Printed circuit	SSEC	1306-2A

TABLE 5-5 VIDEO AMPLIFIER, 1306-3A

Circuit Reference	Description	Manufacturer	
		Name	Part No.
A301	INTEGRATED CIRCUIT, LM201	National Semiconductor	LM201
D301, D302	DIODE, 1N414B	General Electric	
D303, D304			
D305, D306			
C301, C302	CAPACITOR, .0033 μf., ±10%	Sprague	192P33292
C303	CAPACITOR, Ceramic disk, 12 pf., 10%	Centralab	Series DD
C304	CAPACITOR, Ceramic disk, 150 pf., 10%	Centralab	Series DD
Q301, Q304	TRANSISTOR, 2N3644	Fairchild	
Q305			
Q302, Q306	TRANSISTOR, 2N3643	Fairchild	
Q303	TRANSISTOR, 2N4222	Motorola	
R301	RESISTOR, 100K Ω, 5%, 1/4 w.		
R302	RESISTOR, 47K Ω, 5%, 1/4 w.		
R303, R305	RESISTOR, 10K Ω, 5%, 1/4 w.		
R311			
R304	POTENTIOMETER, 500 Ω, 3/4 w.	Spectrol	949-2-1-501
R306	RESISTOR, 2K Ω, 5%, 1/4 w.		
R307	RESISTOR, 82 Ω 5%, 1/4 w.		
R308	POTENTIOMETER, 1K, 3/4 w.	Spectrol	949-2-1-102
R309	RESISTOR, 6.8KΩ, 5%, 1/4 w.		
R310, R316	RESISTOR, 20KΩ, 5%, 1/4 w.		
R312	RESISTOR, 1KΩ, 5%, 1/4 w.		
R313, R319	RESISTOR, 4.7KΩ, 5%, 1/4 w.		
R320			
R314	RESISTOR, 7.5KΩ, 5%, 1/4 w.		
R315	RESISTOR, 100KΩ, 5%, 1/4 w.		
R317	POTENTIOMETER, 5M, 1/4 w.	Bourns	3051P-1-505
R318	RESISTOR, 5MΩ, 5%, 1/4 w.		
R321, R325	RESISTOR, 100 Ω, 5%, 1/4 w.		
R322, R324	RESISTOR, 10 Ω, 5%, 1/4 w.		
R323	RESISTOR, 62 Ω, 5%, 1/4 w.		

TABLE 5-6 REFERENCE FREQUENCY MIXER, 1306-4A

Circuit Reference	Description	Manufacturer	
		Name	Part No.
A401	INTEGRATED CIRCUIT, LM201	National Semiconductor	LM201
C401, C402,C403	CAPACITOR, .082 µf., ±10%	Sprague	192P82392
C404	CAPACITOR, 5 pf., ±10%	Centralab	Series DD
C405	CAPACITOR, 15 pf., ±10%	Centralab	Series DD
C406,C408,C409	CAPACITOR, 510 pf., ±10%	Centralab	Series DD
C407	CAPACITOR, 390 pf., ±10%	Centralab	Series DD
K401	RELAY, Dry reed, DPDT, 6VOC, 50 ohms	Magnecraft	W103MPCX-30
L401, L402	TOROID, 1.5 mh. @ 10 kHz.	Collins	MIC-3
L403	TOROID, 1.75 mh. @ 10 kHz.	Collins	MIC-4
L404	TOROID, 1.2 mh. @ 10 kHz.	Collins	MIC-2
Q401, Q403	TRANSISTOR, 2N3643	Fairchild	
Q402, Q404	TRANSISTOR, 2N3644		
R401, R402	RESISTOR, 100 Ω, 5%, 1/4 w.		
R403, R404			
R405			
R406	RESISTOR, 1.3K Ω, 5%, 1/4 w.		
R407, R408	POTENTIOMETER, 1K, 3/4 watt	Spectrol	949-2-1-102
R409	RESISTOR, 18KΩ, 5%, 1/4 w.		
R410	RESISTOR, 6.24KΩ, 5%, 1/4 w.		
R411	RESISTOR, 560 Ω , 5%, 1/4 w.		
R412	RESISTOR, 1.1K Ω, 5%, 1/4 w.		
R413	RESISTOR, 15KΩ, 5%, 1/4 w.		
R414	RESISTOR, 47K Ω, 5%, 1/4 w.		