COO-1422-98

PRELIMINARY REPORT ON A DUAL PHOTON BONE MINERAL MEASURING INSTRUMENT

MASTER

by

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SCOPE

This report describes the work accomplished in developing an operating breadboard of a two-channel pulse-height analyzer. This breadboard is to serve as a portion of a demonstration model of a proposed Bone Mineral Measuring Instrument system.

TECHNICAL DESCRIPTION

The analyzer is very similar to the technical concept originally outlined. The major functional units are a charge amplifier, two level discriminators, and associated 5-decade scalers.

A. Charge Amplifier

The charge amplifier is of conventional design, consisting of a charge loop, single RC-CR pulse shaping network with pole-zero cancellation, and variable gain voltage amplifier. Power required for the charge amplifier is obtained from a $\pm$ 12 v supply.

B. Charge Loop

The loop amplifier is a LM201 linear IC operational amplifier, compensated for stable operation, at zero input stray capacitance, with a 12 pf compensating capacitor. The feedback network provides a loop charge sensitivity of 0.25 v/pc with a 100 μs decay time constant.

C. Pulse Shaping Network

The input circuit to the pulse shaping stage provides a "zero" to cancel the 100 μs pole response of the charge loop, and differentiates the effective step function input with a 0.5 μs time constant. The integrating feedback network produces the desired 0.5μs, shaped pulse response. The gain element of the pulse shaping network is a high-performance CA3015A operational amplifier.

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DISCLAIMER

D. Voltage Amplifier

The voltage amplifier, also utilizing a CA3015A, provides adjustable gain for an overall amplifier gain range of 8v/pc to 1.3 v/pc.

The output dynamic range of the voltage amplifier is 0 to +7v.

E. Discriminator

The discriminator resolves the pulse height of the charge amplifier into two channels, or "bins". The upper and lower thresholds of each bin are separately adjustable. Functionally, the discriminator is divided into two functional blocks: the comparators and the comparator logic.

F. Comparator

The comparators are constructed on a separate board which is also powered from the $\pm$ 12 volt supply.

The charge amplifier output signal is AC-coupled to the inverting inputs of four differential comparator IC's. It is compared with a threshold voltage set by a potentiometer and resistor divider which is supplied from a reference zener voltage source. The threshold voltage is adjustable from 0 to +4.25 volts.

A second zener regulates the nominal -6v supply required by the comparator IC's.

G. Comparator Logic

The comparator logic operates on the comparator output signals to generate pulse outputs to the two scalers according to the Logic Function Table 1. It is assumed that the comparators A through D are set to successively higher levels, so any output state not shown in Table 1 is "illegal".

Comparator Output	"1" indicates comparator switched "0" indicates comparator not switched				
D	0	0	0	0	1
C	0	0	0	1	1
B	0	0	1	1	1
A	0	1	1	1	1
Logic Output	None	Pulse to low channel scaler	None	Pulse to high channel scaler	None

Table 1. Comparator Logic Function

The comparator logic consists of two functionally identical circuits, one of which operates on the A and B comparator outputs, the second on the C and D outputs.

The leading edge of the signal switches comparator A, which triggers MONO A1 and A2 in sequence. The output of A2 is applied through gating to the scaler input, unless the signal is sufficiently large to trigger comparator B and MONO B. In the latter case, the output of MONO A1 is inhibited by the MONO B output, therefore only those signals with a peak amplitude between the comparator A and B thresholds produce a count input to the low channel scaler. Identical operations are performed on the C and D comparator signals to generate the input to the high channel scaler.

H. Scalers

Two five-decade scalers accumulate the pulse outputs from the comparator logic. Separate reset lines are provided for each complete scaler.

MECHANICAL LAYOUT

The breadboard is constructed on three separate P-type "Vector" breadboards:

Board #1---Charge Amplifier
Board #2---Comparators
Board #3---Comparator Logic and Scalers

To aid in trouble-shooting and signal tracing, all integrated circuits are socket-mounted.

PERFORMANCE

The system operates to prescribed specifications.

To assure proper performance of the breadboard when packaged, the charge amplifier, including input and output lines, should be electrostatically shielded from all other circuits and wiring.

One input of the comparator logic output gates should be utilized as a scaler input inhibit to assure that the scaler content is static when transferring data to an output display device.

The 6.5 μs processing time will result in approximately 30% dead time at a counting rate of 50 KHz. Depending upon data accuracy requirements, it may be necessary to monitor the dead time or event rate, and apply a dead time correction factor.

ACKNOWLEDGEMENT

This work is supported in part by the U.S. Atomic Energy Commission through Contract AT-(11-1)-1422.