SSEC
Technical Memo
Project 1210

LINE START ERRORS IN THE SMS LINE-STRETCHER TIMING SYSTEM

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Forward

Current estimates of the SMS Line-Stretcher timing errors indicate that line start timing is sufficiently precise (less than 0.25 μsec RMS error) to cause no significant problems in cloud displacement measurements. However, the extreme importance of line start timing requires a critical review of current error estimates to establish their reliability. This document, which must rely to a large extent on work done by Philco-Ford and Westinghouse, is at least a partial fulfillment of that requirement.

Except for some minor inconsistencies, each major component of the SMS Line-Stretcher Timing System appears to be well defined in terms of its error contribution. Calculation, laboratory tests, and computer simulation have been appropriately used to study each component. The most recent estimate based on these analyses indicates an RMS line start timing error well below the 0.25 μsec previously specified.

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I. TIMING SYSTEM OPERATION

The SMS Line-Stretcher timing system is diagrammed in Figure 1. All timing information is derived from the output of the sun sensor on board the S/C, which produces one trapezoidal pulse per SMS rotation. The signal conditioner detects the time location of the leading edge of this pulse and creates two new pulses to specify it: an analog sun pulse (transmitted to the ground and used for coarse tuning of the CDA Phase Lock Loop); and a sun synch pulse which is used to turn on a S/C 3.5 MHz counter. At a later time determined by the S/C spin clock a DECOM SYNC pulse turns off the S/C counter and is simultaneously transmitted to the CDA station. The contents of the S/C 3.5 MHz counter are transmitted to the ground as the S/C DIGITAL SUN PULSE, which contains the 8 LSB (Least Significant Bits) of the number of 3.5 MHz clock pulses during the time interval between the SUN SYNC PULSE and DECOM SYNC PULSE.

In similar fashion the time interval between the smoothed SUN SYNC PULSE output of the CDA DPLL (Digital Phase Lock Loop) and reciept of the DECOM SYNC PULSE is measured by a CDA 3.5 MHz counter. The difference between this CDA DIGITAL SUN PULSE and the S/C DIGITAL SUN PULSE is the error signal used to provide phase and frequency corrections to the DPLL. The parameters A and B are adjustable and control the loop bandwidth.

The basic DPLL clock frequency depends on spin rate since it is adjusted to produce a constant number of counts per SMS rotation. (At 100 RPM the synthesizer frequency is 5.2416 MHz). The SUN ANGLE COUNTER (SAC) counts up to M=3144960 at a rate determined by the synthesizer frequency and then recycles. The DPLL smoothed sun sync pulse output occurs when the SAC reaches zero. This pulse turns on the 3.5 MHz CDA counter and also determines line start timing.

The DPLL output is a smoothed SUN SYNC pulse which is aligned to the mean leading edge of a sequence of sun sensor pulses. In addition to reducing the time jitter of the sun sensor output by averaging, the DPLL must also track variations in spin rate which occur during forward mirror stepping, retrace, and after eclipse. Since low RMS noise and accurate spin rate tracking (low bias noise) are somewhat contradictory requirements, optimum choices of the loop parameters A and B must be made for each situation.

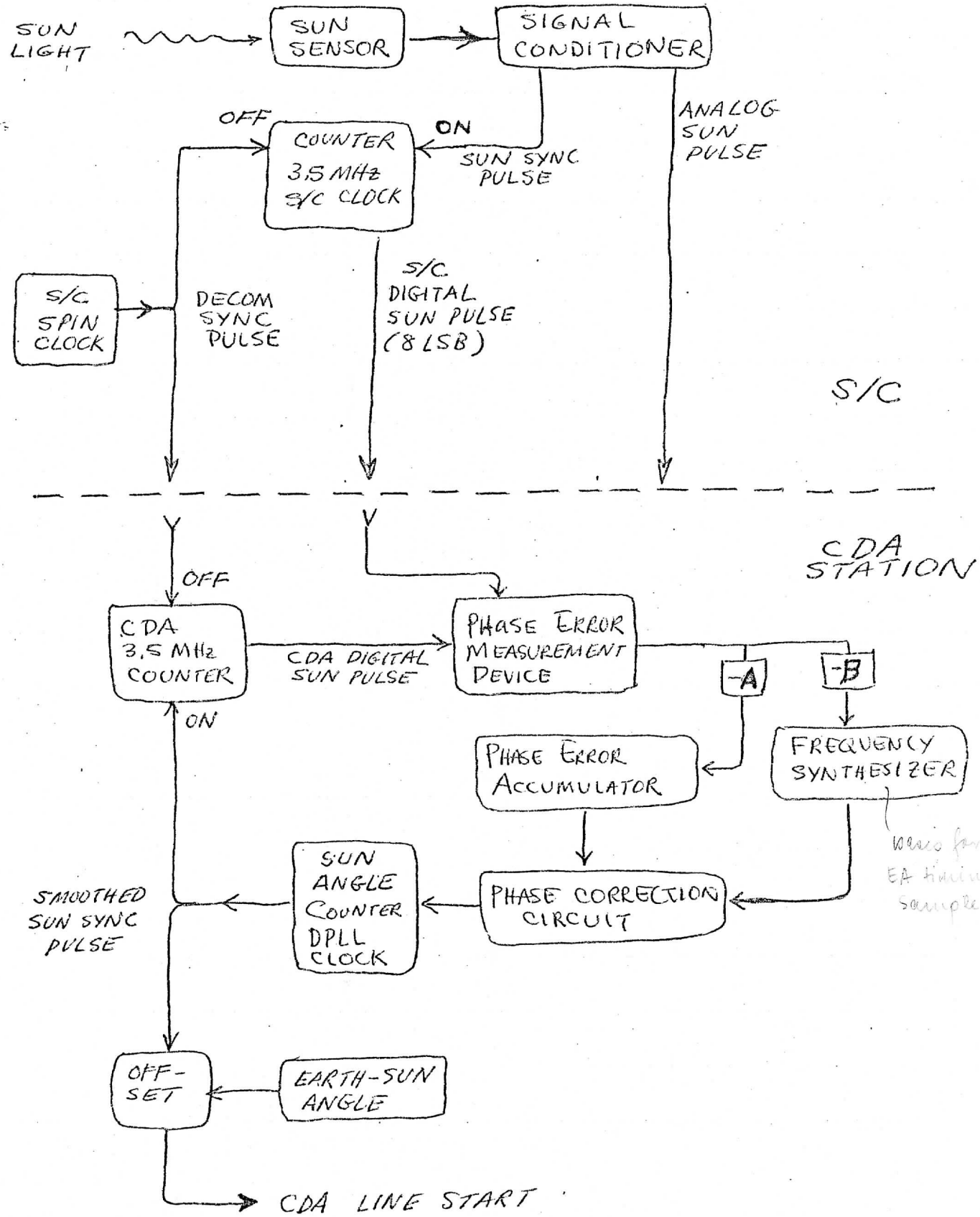
SUN LIGHT
SUN SENSOR
SIGNAL CONDITIONER
ANALOG SUN PULSE
OFF
ON
COUNTER 3.5 MHz S/C CLOCK
SUN SYNC PULSE
S/C SPIN CLOCK
DECOM SYNC PULSE
S/C DIGITAL SUN PULSE (8 LSB)
S/C
CDA STATION
OFF
CDA 3.5 MHz COUNTER
CDA DIGITAL SUN PULSE
PHASE ERROR MEASUREMENT DEVICE
-A
-B
ON
PHASE ERROR ACCUMULATOR
FREQUENCY SYNTHESIZER
SUN ANGLE COUNTER DPLL CLOCK
PHASE CORRECTION CIRCUIT
SMOOTHED SUN SYNC PULSE
OFF-SET
EARTH-SUN ANGLE
CDA LINE START

Figure 1

II. SMS LINE STRETCHER TIMING ERRORS

There are three factors which affect the timing error in the DPLL output: (1) noise in the sun sensor and signal conditioner electronics; (2) errors in communicating the sun pulse location to the CDA station; and (3) limitations in DPLL performance. The total effect of these factors follows a quantitative description of each.

1. Sun Sensor and Signal Conditioner Errors

A functional diagram of this system is presented in Figure 2. Operation of the system can be described best by quoting from Vol. I, Book 2, Phase C Design Report, Philco Ford, 30 June 1971 (p. 14-3):

> "The sun sensor consists of a light sensitive diode which is illuminated by the sun once per spacecraft revolution. The width and amplitude of the output current pulse are functions of the angle of the sun with respect to the spacecraft longitudinal axis. A preamplifier located in the sun sensor assembly convert the current pulse to a voltage pulse. This is accomplished at the sun sensor in order to minimize the effects of the noise picked up by the sun sensor to ADAC electronics wiring, and the equivalent input noise of the various amplifiers located in the signal conditioner assembly. The bandpass filter serves the dual purpose of reducing the signal noise bandwidth and eliminating the effect of preamplifier offset voltage drift. The peak signal voltage detector output, when divided in half, establishes a switching reference for the sun sync and sun angle comparators."
>
> "The leading edge of the sun sync comparator output pulse establishes a precise spin period reference while the width of the sun angle comparator output pulse is proportional to the spacecraft-to-sun angle. The effects of sun sensor thermal change are eliminated by the use of a peak detector for establishing threshold reference."

The time location of the 50% point of the sun sensor signal is communicated by the SUN-SYNC PULSE output of the threshold detector. The time jitter in the SUN SYNC PULSE is equal to the combined SUN SENSOR signal noise and threshold reference noise divided by the slope of the sun pulse at the 50% point (all quantities measured at the threshold detector input). Using a worst case

slope of 2.4 mV/μsec and a requirement of 1/3 μsec RMS time jitter Philco-Ford established a total noise budget of 678 μV at the threshold detector. Combining the effects of sun sensor noise, preamp noise, bandpass filter noise, peak detector and low-pass filter noise, threshold detector noise, spacecraft harness noise, and gain variation (some quantities measured and some estimated), they concluded that the system noise would not exceed the specified budget. Philco Ford also conducted laboratory tests on the sun sensor signal conditioner and preamplifier circuits using a simulated sun sensor input pulse. Results showed a probable RMS time jitter of 0.330 μsec and a worst case RMS jitter of 0.38 μsec (Philco-Ford, Phase C Design Report, Book 2, Vol. 1, 30 June 1971, p. 14-17). The latest SMS Error Budget up-date (Philco Ford, SMS-PCC-3577, 14 February 1972), indicates an RMS time jitter of 0.343 μsec and a DC offset error of 0.0292 μsec.

2. Communication Errors

The information which must be communicated to the CDA station DPLL is the time difference between the S/C SUN SYNC pulse and the DPLL output. The actual difference is between two digital 3.5 MHz counters, one on the S/C and one on the CDA station (see Figure 1), both turned on by the DECOM SYNC pulse. Errors produced in communicating this difference are:

(a) Quantization Errors: These result from the measurement of continuous time variables in discrete units (0.286 μsec). The combined counting error of S/C and CDA sun angle counters was computed by both Westinghouse and Philco-Ford, under what appear to be identical assumptions. However, Westinghouse (S/DB Design Plan, Oct. 1971, p. 2-61) derives an RMS counting error of 0.117 μsec, while Philco-Ford (TM #204, SMS-PCC-3452, SMS SUN-PULSE TIMING SUBSYSTEM ANALYSIS, J. Y. Huang, Oct. 1971, p. 3-19) obtains an RMS counting error of

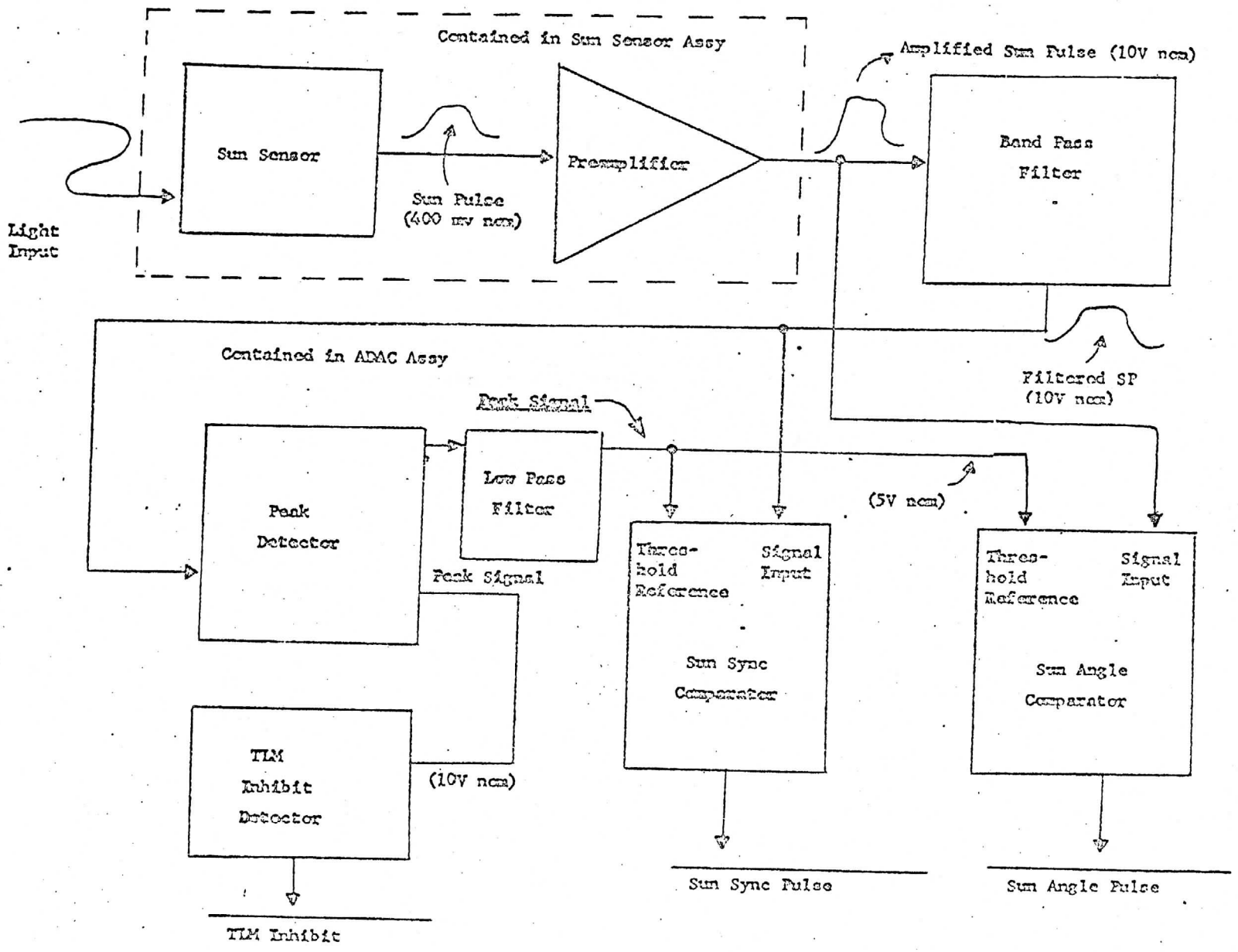

Figure 2. Sun Sensor Signal Conditioner Block Diagram

0.202 μsec. At present, information sufficient to explain this difference is not available. It should be noted that the most recent Philco-Ford update of the SMS error budget (SMS-PCC-3577, 14 February 1972) maintains the 0.2 μsec RMS counting error.

(b) Frequency Errors: These arise if the S/C and CDA station 3.5 MHz clocks do not have precisely the same period. Westinghouse (S/DB Design Plan, Oct. 71, p. 2-61 and 2-62) allocated 0.3 μsec RMS timing error to this source. They estimated equal contributions from short term drift of the S/C oscillator and from CDA tracking loop errors (the CDA oscillator is locked to the S/C oscillator by a PLL). The Philco-Ford group does not explicitly include frequency errors in its timing error analysis. They state no reason for this omission.

(c) Bit Errors: In the S/C - CDA station transmission link bit detection errors can cause an effective timing jitter in the digital sun pulse. The RMS value of this jitter depends on the number of bits in the data word and the probability, p, that one bit of data is erroneously detected. Huang (SMS-PCC-3452) found the RMS timing error to be $\sqrt{p}$ x 59.6 μsec. With a bit detection error probability of 10^{-5} the resultant RMS timing error turns out to be 0.188 μsec. (Incredibly, Westinghouse finds a linear dependence on p and estimates an RMS timing error of 0.042 μsec for $p = 10^{-3}$.)

Using the largest estimates for each of these sources we may estimate an RMS timing error due to communication of $[0.2^2 + 0.3^2 + 0.19^2]^{1/2} =$ 0.408 μsec. The most recent Philco-Ford update of the SMS Error Budget uses $[0.2^2 + 0.19^2]^{1/2} = 0.276$ μsec for the total RMS communication error.

3. Limitations in DPLL Performance

The basic task of the DPLL (Digital Phase-Lock Loop) is to track the real variations in spin rate (signal) and, at the same time, to smooth the

false variations due to sun pulse time jitter (noise). The primary sources by signal variations can be summarized as follows (N. Furomato, "Inputs to Line-Stretcher Timing System", SMS-PCC-1669; May 20, 1971):

(a) Thermally Induced Moment of Inertia Change Due to Eclipse. Two hours after eclipse the differential spin period change is 30 μsec per frame. This change decays exponentially in time with a two hour time constant. The change is less than 1 μsec ten hours out of eclipse.

(b) Stepping of an Unbalanced Scan Mirror. This causes S/C moment of inertia changes during each frame and results in a continuous spin rate change (linear in time) during normal scanning followed by an equal but opposite net change during retrace. Estimates for the peak to peak variation during a frame spin the range from 0.25 μsec (SMS-PCC 1669, May 1971) to 4.5 μsec (SMS-PCC-3452, Oct. 1971) depending on the assumed scan mirror imbalance. (Actually the 4.65 μsec estimate appears to be an error.) The most recent estimate (SMS-PCC-3577, Feb. 1972) is 2.33 μsec, assuming a dynamic imbalance of 7.08 $lb\text{-}in^2$.

(c) Nutation Due to Scan Mirror Stepping. Even if the scan mirror is balanced, reaction torque produced during scan mirror stepping causes the S/C spin axis to wobble (nutate). This causes an apparent periodic variation in spin period which is, nevertheless, considered as signal because both the sun sensor and the VISSR are similarly affected (i.e., nutation causes no apparent change in the angle between sun sensor and VISSR look directions). Under steady state assumptions, i.e., continuous mirror motion instead of the actual step and stop motion, the apparent spin period variation is periodic with an amplitude of 0.06 μsec (o.52 μsec during a two minute retrace) and a period of six seconds. Although the nutational transient was considered to be

a possible source of significant error (Westinghouse, S/DB Design Plan, Oct. 1971, P 2-71), attitude motion simulation tests by Philco-Ford (Phase C Design Report, Book 2, Vol. 1, p. 4-18, 30 June 1971) have apparently shown otherwise.

Since the DPLL is based on digital operations (during tracking), computer simulation of the system can be considered a meaningful test of its performance. Both Westinghouse and Philco-Ford conducted simulation tests of the DPLL. General results of these tests were presented in Table 1. Except for the noted difference in spin rate variation both groups used the same signal input discussed in this section. They both used a random noise of approximately 1.1 μsec superimposed on the DPLL signal input. Not suprisingly the determined values of RMS noise in the DPLL output are found to be quite similar also.

There are a number of DPLL performance characteristics which are not revealed in Table 1. Among these, the following might be significant:

(i) The loop cannot track periodic variations resulting from nutation because of their relatively high frequency compared to the natural frequency of the loop. This currently does not represent any serious problem because the peak timing drift due to nutation is only 0.06 μsec. However, any increase in nutation induced errors could be serious because the loop is powerless to reduce them.

(ii) In the presence of small loop frequency errors timing error linearly increases with time until a phase correction is required. This results in a sawtooth pattern of timing error, with a peak to peak amplitude of approximately 0.2 μsec and a period ranging from 10 to 100 input pulses per cycle. This "limit cycle" oscillation could result in frame to frame displacement errors which are periodic in scan line, and have peak errors as large as 0.4 μsec (leading to a 0.2 knot E-W velocity error for 30 minute

frame interval). Although this error is quite small in magnitude, for a given pair of frames it can be constant over a wide latitude band (70 km to 700 km) and completely immune to the averaging of displacement measurements of cloud elements within the band. Thus, it could interfere with determinations of small velocity large scale motions.

The simulation tests verify the linear mathematical analysis of the loop made by Huang (SMS-PLC-3452). The loop reduces random input RMS jitter by a factor 0.2; the loop introduces a peak quantization error of 0.1 μsec; the loop can't track nutational variations (this results in a peak error of 0.06 μsec).

Table 1. DPLL PERFORMANCE

TESTING GROUP	SIGNAL INPUT	RMS NOISE INPUT	RMS NOISE OUTPUT	BIAS ERROR (1 FRAME)	TIMING DRIFT (1 FRAME)
Westinghouse[1]	Nutation + 0.25 μsec/frame spin period change	1.1 μsec	0.24 μsec	0.104	N.A.
Philco-Ford[2]	Nutation + 4.67 μsec/frame spin period change	1.05 μsec	0.25 μsec	0.1 μsec[4]	0.7 μsec (peak-to-peak)[3]

NOTES: (1) S/DB DESIGN PLAN, Oct. 1971, p. 2-70

(2) "SMS SUN-PULSE TIMING SYBSYSTEM ANALYSIS, J. Y. HUANG, SMS-PCC-3452, Oct. 1971, p. ix

(3) This applies only to the first frame after acquisition of the DPLL. The drift drops to 0.35 μsec or less in the second and succeeding frames.

(4) This requires changing the DPLL bandwidth during retrace.

III. LINE START TIMING ERROR SUMMARY

Table 2 summarizes the contributions of all error sources previously discussed and the resulting error in the DPLL output sun pulses. The peak value stated is approximately equivalent to a 4σ value (the RMS error is approximately one fourth of the peak). The net error is probably somewhat conservative. It is slightly larger than the most recent Philco-Ford estimate of 0.57 μsec peak (SMS-PCC-3577, Feb. 72) because it includes frequency errors. It is smaller than Huang's first estimate of 1.16 μsec peak because a smaller (and more recent) value is used for the RMS jitter in the sun pulse signal conditioner output.

The line start time contains an additional source of error, i.e., the quantization error in the earth angle counter which counts the 24 bit β value and defines the angular delay between the scan synch pulse and the start of earth view sampling. Since this count is made at the VCO frequency (twice the synthesizer frequency) the unit of time is approximately 0.096 μsec. The peak and RMS errors from this source are thus 0.05 μsec and 0.03 μsec respectively. These are insignificant errors. Thus, it appears that the RMS jitter in line start timing should be well within the 0.25 μsec specified.

The significance of the systematic displacement error resulting from the limit cycle oscillation of the DPLL depends on user requirements for highly accurate measurements of large scale E-W motions. However, even if better than 0.2 knot accuracy is required, averaging over several frame pairs should be justifiable for this scale and effective in reducing the displacement errors since the limit cycle oscillations will have phases that are random from frame to frame.

Table 2. SUN PULSE TIMING ERROR SUMMARY

INPUT ERRORS

S/C SUN SYNC PULSE RMS Jitter	0.343 μsec
Communication Errors (RMS)	
Quantization Error	0.20 μsec
S/C to CDA transmission link ($P_E=10^{-5}$)	0.19 μsec
Frequency errors in 3.5 MHz clocks	0.30 μsec
Total RMS jitter input to DPLL	0.532 μsec

OUTPUT SUN PULSE ERRORS

RMS Jitter out = $(\sigma out/\sigma in)$ 0.532 = 0.106 μsec
4σ jitter = 0.425 μsec
DPLL Quantization (Peak Value) = 0.1 μsec
S/C Nutational Motion (Peak Value) = 0.06 μsec (not tracked by DPLL)

Total Timing Error (Peak Value) = 0.69 μsec

The probability that the timing error of any one of the smoothed pulses in a picture frame exceeding 0.69 μsec is approximately 0.10.