MAN-COMPUTER INTERACTIVE DATA ACCESS SYSTEM (McIDAS)

Continued development of McIDAS and operation
in the GARP Atlantic Tropical Experiment

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16. Abstract

Using McIDAS, the complete output of the Synchronous Meteorological Satellite (SMS-A) was recorded on one inch magnetic tape during the GATE period. 4337 images were recorded, 97.75% of all data transmitted.

The McIDAS quality control subsystem tests cloud track vectors against four sets of criteria; (1) rejection if best match occurs on correlation boundry, (2) rejection if major correlation peak is not distinct and significantly greater than secondary peak, (3) rejection if correlation is not persistent, and (4) rejection if acceleration is too great.

The cloud height program determines cloud optical thickness from visible data and computer IR emissivity. From IR data and temperature profile cloud height is determined.

The report also includes complete McIDAS functional description and electronic schematics.

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    Archive Power Box

VIDEO CHAIN

    McIDAS Unit Interface

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PREFACE

This is the final report of work performed under NASA Contract
NAS5-23296 during the period from 13 August 1973 to 11 December 1974. The
report includes the complete functional descriptions and schematics for all
of the subsystems of the Man-computer Interactive Data Access System (McIDAS).
This documentation of McIDAS is the deferred portion of the final report
on Contract NAS5-21794 also. The many minor changes in the McIDAS hardware
which have been made during the past 18 months are incorporated in the sche-
matics; therefore the documentation set represents the full shaken-down
version.

The sections on Cloud-Track Quality Control and SMS Cloud Heights des-
cribe major portions of the cloud-track wind measurement technique developed
at SSEC. Other major segments such as Navigation and WINDCO have been de-
scribed earlier. It should be noted that development and refinement of all
portions of the cloud-track wind measurement system are continuing. There-
fore, one may expect that details of the system descriptions contained in
this report will differ increasingly from current practice as time goes on.

I would like to thank the authors of several sections of this report for
their excellent work. We all recognize that the number of people who have
contributed to our successes in the McIDAS effort has been large and I view
their work with grateful admiration. Not the least of those who have helped
us has been Mr. Jim Greaves, GSFC Technical Monitor of McIDAS work. Jim has
combined patience with insistence, understanding with firm direction,
flexibility with highest integrity to establish a most effective and enjoy-
able relationship between ourselves and the National Aeronautics and Space
Administration.

Verner E. Suomi
Principal Investigator

ARCHIVING SMS DATA DURING GATE

GARP Data Systems Tests and the GATE program have requirements for rather sophisticated SMS image processing for the extraction of meteorological information. The McIDAS incorporates many of the needed extraction techniques provided it has a high quality readily accessible data base. The archive system developed under this contract provides that base.

The archive system consists of a 24 foot parabolic antenna, the receiver and controller, interface electronics, data buffers and an IVC video slant track recorder. The storage capability is approximately 32 full resolution SMS images per reel of tape. This represents about 5×10^{10} bits per reel.

Beginning in May 1974 plans were laid for the manning and training of personnel for the 24 hour archiving effort during GATE. Manuals, logging forms, etc. were prepared and students hired in anticipation of a 15 June starting date. However, due to NASA-NOAA system testing, archiving was not started until 27 June 0830 GMT. The training of the archive personnel (students) was accomplished by previously checked out staff members during the first two weeks of archiving. Archive quality checking was done on a nearly daily basis by displaying 12 samples of data from each data tape on the McIDAS system. Visual inspection was the only evaluation technique used. Only two minor problems were observed in the data until 8 August. One problem was bad chips in the data buffers which resulted in loss of approximately 1% of the data in each image. This was a continuing problem throughout the entire archive period as replacement of bad chips frequently caused others to fail. The other problem was the occasional (.2% per image) scrabbling of a line of data due to a dropped data bit. This problem was

eliminated in the first week of archiving. In total, equipment failures caused the loss of 96 images. One-third of each of 45 additional images were also lost due to an incomplete fix of one of the equipment problems. The period of this data loss was 1630 GMT, 6 August to 1800 GMT, 9 August. A second data recording problem effected data (184 images) between 1030 GMT, 12 September and 0400 GMT, 16 September. The problem was a drift in the alignment of record slant track recorder. The data quality is very high, but playback requires continuous manual adjustment of the playback recorder alignment. Archiving was completed as of 2350 GMT, 28 September 1974 at the end of GATE.

The statistics for the archive are as follows:

4437	Images transmitted
4	Images missed by operator errors
96	Images unusable due to equipment failure
4337	Usable images recorded (97.75%)
45	Degraded (noisy third line)
4292	High quality images recorded (96.75%)
184	Difficult to read
4108	Operational usable high quality images recorded (92.59%)

CLOUD-TRACK QUALITY CONTROL

INTRODUCTION

Any set technique for tracking cloud motions has inherent limitations on the accuracy of its results. If such tracking errors can be reduced by discarding apparently bad measurements, the value of the remaining wind vectors increases due to their increased reliability. However, bad measurements cannot be discarded without losing some accompanying good measurements. Quality measurements, compensation for missing data, and smoothing techniques can provide vector sets which will produce a better estimate of the wind field than will a data set containing spurious anomalies that distort the true circulation. This philosophy has guided the selection of a number of wind quality control criteria which discard measurements with a high probability of being in error while maintaining the through-put of the McIDAS.

How can such criteria be set? The image match procedures on the McIDAS determines a cloud's displacement based on the similarity of cloud features from two different satellite images taken over the same area at two different times. If this similarity satisfies a 'best fit' criterion in comparison to all other lag positions under consideration, that displacement is assigned to the cloud's motion. If the image match procedure is determined to have failed or to be below acceptable quality based on further criteria, that measurement will be discarded.

Four such criteria are discussed in this report. In the SSEC McIDAS these quality control criteria are combined with an operator's careful judgement to minimize the possibility of a bad measurement being accepted by the system.

Three techniques are applied during the image matching process; the last technique is not utilized until after wind vectors have been generated. Two methods require wind vector pairs separated by a time interval of 30-60 minutes. McIDAS wind computation is a cloud tracking process, which accumulates cloud motion measurements by tracking individual cloud targets in three (or more) successive image frames. This process provides at least two successive independent wind estimates which can be compared. The SSEC image matching techniques use a cloud target grid at time t_1 along with a larger data match grid at time t_2 containing the cloud target. An image matching grid is generated by the application of one of several metrics. The image match grid is composed of lag coefficients for each lag position the small target grid (t_1) can take with respect to the larger data match grid (t_2). These lag coefficients are scanned for the best match coefficient. The position of the best match coefficient is generally defined as the occurrence of the greatest relative maximum on the image match surface.

TECHNIQUE 1: Best Match Occurrence on Matrix Boundary

Since the image match procedure is dependent on finding a relative maximum on the match coefficient surface, the occurrence of a maximum on the boundary of the match coefficient array prevents the confirmation of a local maximum. A match coefficient which occurs on the boundary of an image match coefficient matrix is illustrated in FIGURE 1. These cases are marked with a type 1 error code and can be discarded by the system.

TECHNIQUE 2: Secondary Peak Comparison

Generally, an image match surface has more than one relative maximum. We distinguish the greatest relative maximum as the best match coefficient.

Other relative maxima are referred to as secondary peaks of the image
match coefficient surface. It is natural to compare secondary peaks to
the best match coefficient. These peaks may represent a number of possi-
bilities. Leese has suggested that, in certain cases, they represent cloud
displacements of the non-predominant cloud layers contained in the target
grids. Our investigations have shown that, generally, these peaks represent
spurious target matches, noise spikes and echo peaks in the image match
surface. FIGURE 2 illustrates an image match coefficient surface contain-
ing multiple peaks.

We have tried to develop a basis for deciding which relative maximum
indicates the true cloud displacement. Our analysis of image match surfaces
has revealed that secondary peaks are basically spurious alignments unless
they occur close to the absolute maximum or compete in size comparison.
Our criterion for a good measurement is a well defined dominant peak, as
indicated in FIGURE 2. Quality control can be applied whenever the surface
analysis indicates an ambiguous case.

The surface analysis technique determines three characteristics of
secondary peaks with respect to the dominant peak. FIGURE 2 illustrates
these characteristics with respect to peaks 1 (dominant peak) and 9
(secondary).

    a. Difference between secondary peak and dominant peak
       coefficients (R)

    b. Distance between secondary peak and dominant peak positions (D)

    c. Area dominated by stronger peaks with respect to secondary
       peak (surface area above thick horizontal line)

These characteristics are determined as follows:

Consider a t_1 target grid of size k lines by ℓ elements and a larger

t_2 match grid of size m lines by n elements. These grids will generate

a (m-k+1) by (n-ℓ+1) image match coefficient grid C. Let p be the number

of line lags of C such that,

$$p = m - k + 1$$

and q be the number of element lags where

$$q = n - ℓ + 1.$$

Let $c_{(s,t)}$ be the image match coefficient of matrix C at lag position

(s,t) where s=1, p, t=1, q. Let Y be the set of image match coefficients

of C greater than or equal to $c_{(s,t)}$. Then, $c_{(s,t)}$ is a secondary peak if

and only if no entry of Y is a neighboring point to $c_{(s,t)}$. A neighboring

point is defined as a point adjacent to the $c_{(s,t)}$ in question. Note that

the dominant peak is also considered a secondary peak in this context.

An algorithm which systematically finds necessary peaks in decreasing

order of their magnitude is as follows. Let the indices (s,t) of C be

ordered in an array D such that $i \leq j$ implies that $c_{(s,t)_i} \leq c_{(s,t)_j}$.

This is done efficiently with an oscillating tree sort. Then $c_{(s,t)_1}$ is

necessarily the coefficient of the dominant peak and $(s,t)_1$ is its lag

position. Let N be the number of secondary peaks in C. A secondary peak

position function $f(j) = (s,t)_{i(j)}$ is defined for j=1, N. Let f(1) be the

lag position of the dominant peak. The second value of f is found by testing

the ordered lag positions in D following f(1) for the first one not adjacent

to a prior position. This gives f(2) which is defined as $(s,t)_{i(2)}$ where

$i_{(2)}$ is the index of the entry in the ordered lag index array D. Further

secondary peaks are found in the same manner until the array D is exhausted.

The difference R, between the secondary peak coefficient $c_{(s,t)_{i(j)}}$ and

the dominant peak coefficient $c_{(s,t)_1}$, is tested against a constraint parameter.

When one applies the Euclidean Norm, each match coefficient measures the

square of the rms difference at that alignment position. There are three types of noise preventing zero rms difference at the correct alignment position; sampling noise, feature evolution noise, and random noise. The random noise is small since the comparison of cloud features is averaged over reasonably large areas. The sampling noise and the feature evolution noise are basically inseparable. However, if one has the additional information that large smooth features are under consideration, sampling noise will be smaller. One can estimate the total effect of the sampling noise and the feature evolution noise from the size of the minimum Euclidean Norm coefficient. The difference between the maximum coefficient and the next largest relative maximum coefficient should exceed this minimum Euclidean Norm coefficient for one to have confidence in the displacement measurement.

The distance D, between the secondary peak position $(s,t)_{i(j)}$ and the dominant peak position $(s,t)_1$, is tested against a second constraint parameter. The index $i(j)$, of the ordered lag position array D, corresponding to the total surface area dominating the secondary peak j, is tested against a third constraint parameter. If any of these tests fail, the cloud target is marked with a type 2 error code and can be discarded.

TECHNIQUE 3: Image Match Surfaces Comparison

A relatively stable cloud target can be tracked over more than one time interval. A quality control technique can then be applied by comparing the respective image match coefficient surfaces from successive intervals. This comparison produces a cross correlation coefficient and measures both cloud target evolution and differential motion across the cloud field. FIGURE 3 shows two image match surfaces C_1 and C_2, resulting from tracking

a cloud target over two adjacent thirteen minute time intervals. The similarity between the surfaces indicates that the cloud target was stable and that it was moving with its neighboring clouds.

For comparison, the matching surfaces are aligned so that the best matching coefficients from each matrix coincide. The resultant intersection contains two sub-surfaces which can be compared or correlated. FIGURE 4 portrays this alignment between two image match matrices. The cross correlation coefficient between the two sub-surfaces is an estimate of congruency which can be tested against a congruency threshold parameter. If the coefficient is below the criterion, the cloud target is marked with a Type 3 error code and can be discarded.

TECHNIQUE 4: Acceleration Criteria

Wind measurements that are made removed from severe weather activity are expected to be smooth with respect to time. Hence, acceleration terms across a period of one hour are expected to be small. The McIDAS system enables an operator to select the same cloud target for displacement measurement over two or more successive time intervals. The software provides for the computation of acceleration terms (*u and v component residuals) and further allows the discarding of wind measurements if the accelerations exceed set criteria.

Two acceleration terms are generated. The north-south components (v components) of two successive measurements are subtracted and tabulated into a table of intervals, yielding a v residual frequency distribution. The east-west components (u components) of the wind are treated identically. Plotting an acceleration frequency distribution yields two results. First, the spread of the distribution estimates the variance of the image matching technique's ability to resolve cloud displacements. Second, the shift of

the mean value of the dispersion from the origin of zero acceleration

estimates the acceleration bias induced in the wind measurements by the

navigational scheme. FIGURE 5 illustrates such a table. Both u and v

residual distributions are shown representing 168 vector pairs from July

26, 1969 ATS-III data.

Note that the mean value of each distribution is within 1 meter per

second of zero acceleration. These differences provide a best estimate

of navigational alignment accuracy. The spread of each distribution esti-

mates the magnitude of random error in the measurments. Comparison of

the distributions shows that the u component spread is greater than the v

component spread. The larger variance is due to line jitter inherent in

the ATS data, supporting the argument that the line step system is more

stable than the line sweep system. Thus, the random error of the measure-

ments can be constrained by discarding cases which exceed selected acceler-

ation criteria. Cloud targets which do not meet consistency parameters are

marked with a Type 4 error code.

There are meteorological situations with strong acceleration forces

such as cyclonic or anti-cyclonic circulation, jet streams and frontal

zones. Checks for u and v consistency (low acceleration restrictions) will

discard valid measurements. Quality control in these instances requires

either relaxing the u and v consistency constraints or checking other

parameters. Two alternative consistency checks can be applied with the

McIDAS software; these are a wind direction and absolute velocity check.

Clouc tracking is done in a lagrangian coordinate system. Since cloud

displacements are associated with the dynamic flow, cloud target paths of

known characteristics can be checked for verification. For example, if

winds associated with a jet stream are decelerating but not turning, a force on a cloud target is perpendicular to the direction of its motion, such as a cloud moving along the spiral of a vortex, the kinetic energy of the cloud mass ($\frac{1}{2}mV^2$) is conserved. Hence the absolute velocity $V = u^2 + v^2$ can be checked for consistency.

FUTURE DEVELOPMENTS

Future software will provide the system operator with more information on wind field quality. Time, height and spatial smoothing techniques (symmetric and asymmetric) will be available to merge vector clusters to a single best wind estimate. At the same time, conventional data will be made available for comparison. Analysis procedures will then be used to judge, on a weighted scale, the validity of wind estimates.

SUMMARY

McIDAS is an interactive system under control of the judgement of its operator. Automated quality control techniques serve only as an information source on the quality of cloud displacement measurements and do not automatically discard wind estimates. The system was designed to operate in this manner to minimize software validity check mis-evaluations. The operator uses the ability to synthesize a field of wind measurements displayed with their corresponding imagery, in a dynamically consisten situation, to finalize judgement on weach wind vector. This is the final step of the McIDAS quality control process.

Best match coefficient
occurs on matrix boundry

2-9
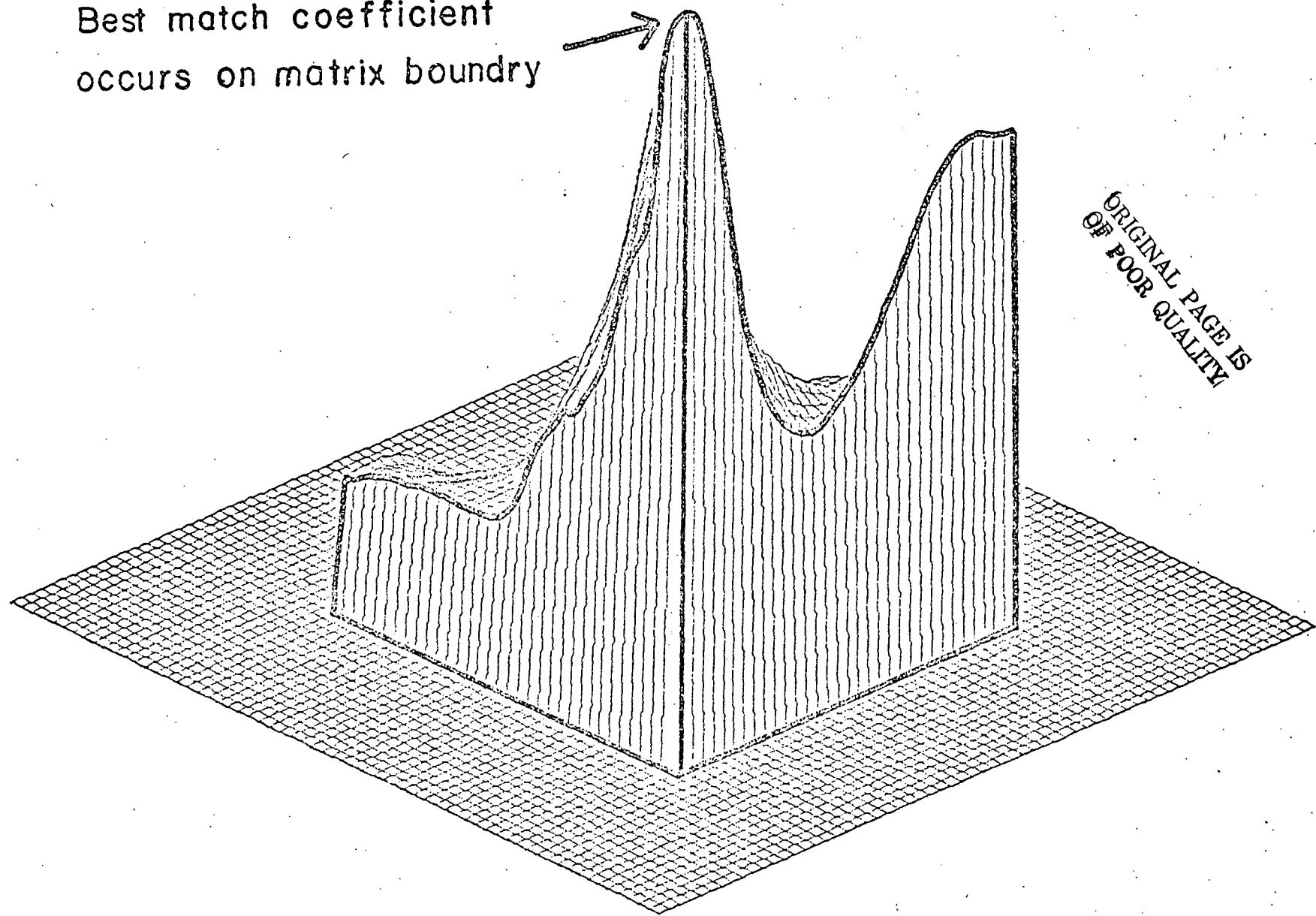
Figure 1

OCCURRENCE OF BEST MATCH COEFFICIENT ON BOUNDARY

Image Match Coefficient Surface With Multiple Peaks

Dominant Peak

Secondary Peak

C_{s_0,t_0}

D

R

C_{s_i,t_i}
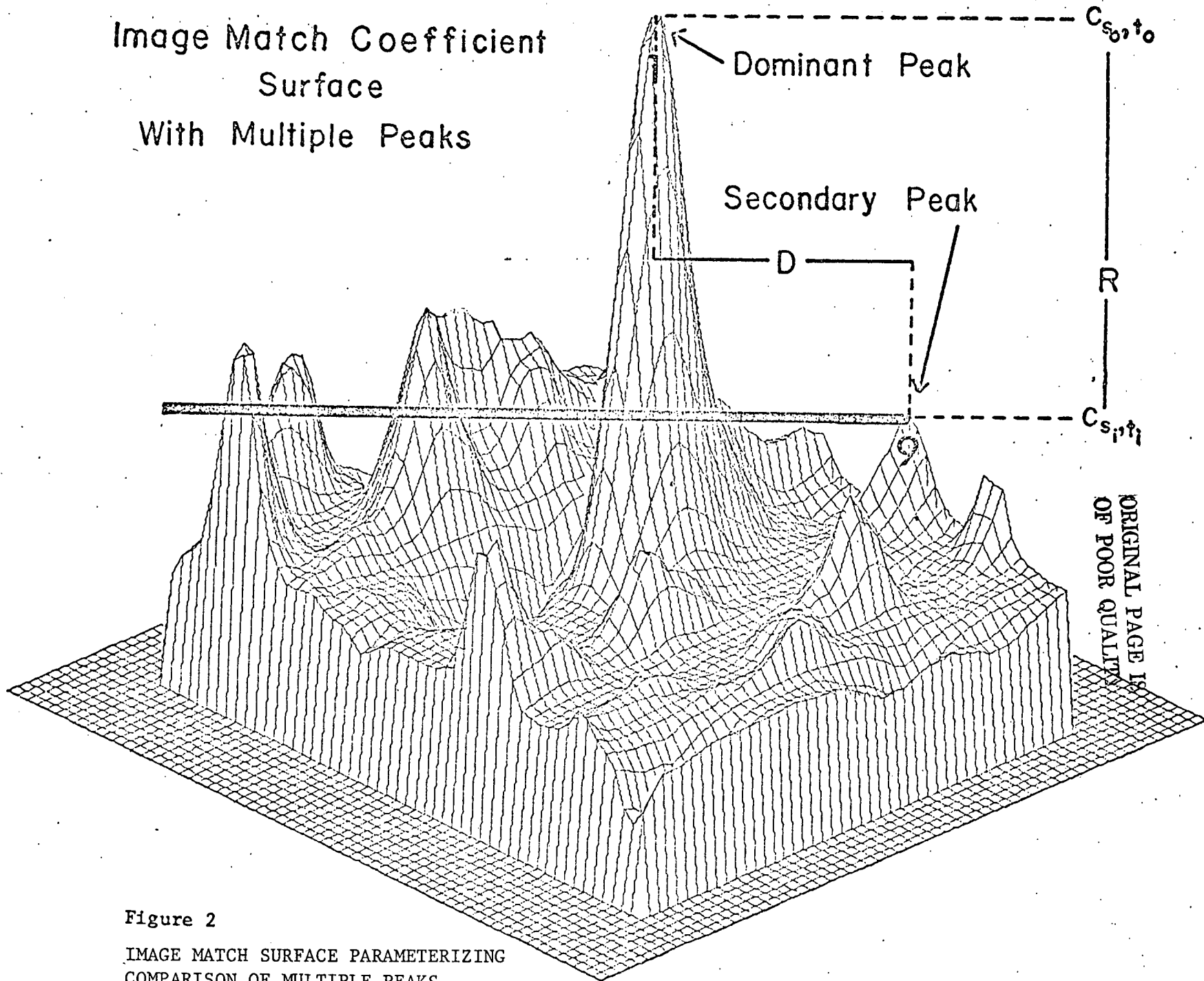
Figure 2

IMAGE MATCH SURFACE PARAMETERIZING COMPARISON OF MULTIPLE PEAKS
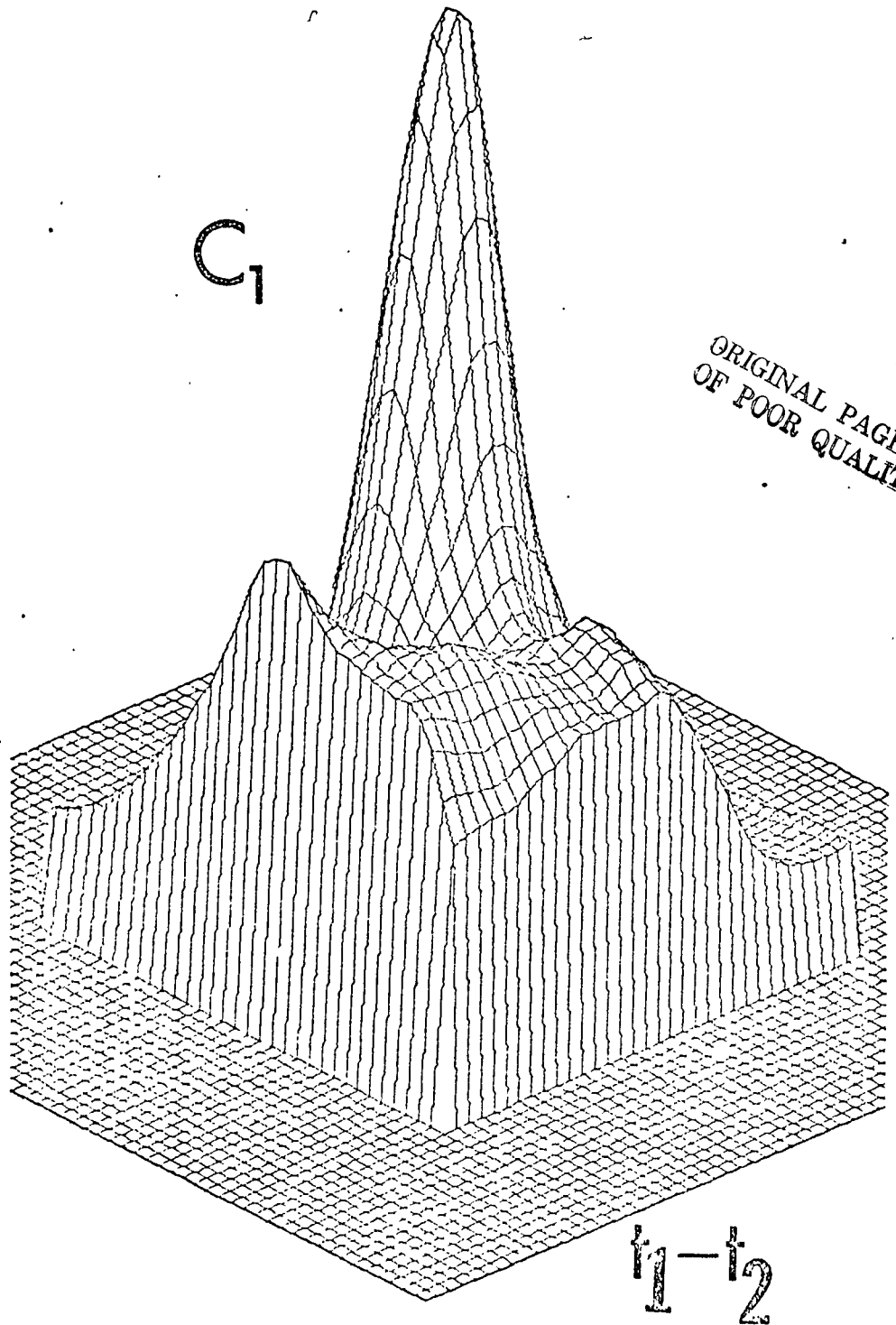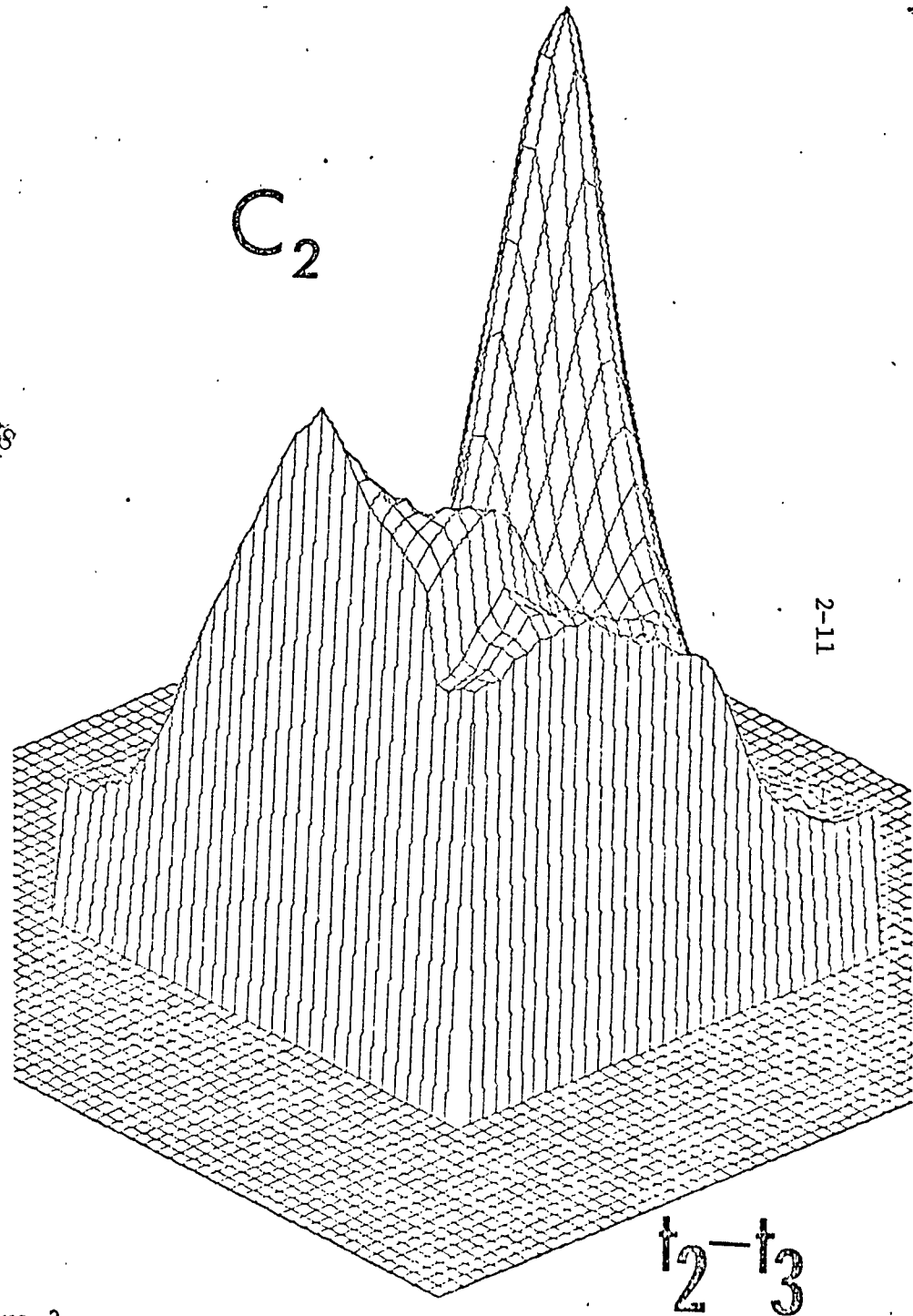
2-11

Figure 3

MATCH SURFACE ARRAYS OF SAME CLOUD TARGET OVER TWO DIFFERENT TIME INTERVALS

Alignment at Best Match Coefficients
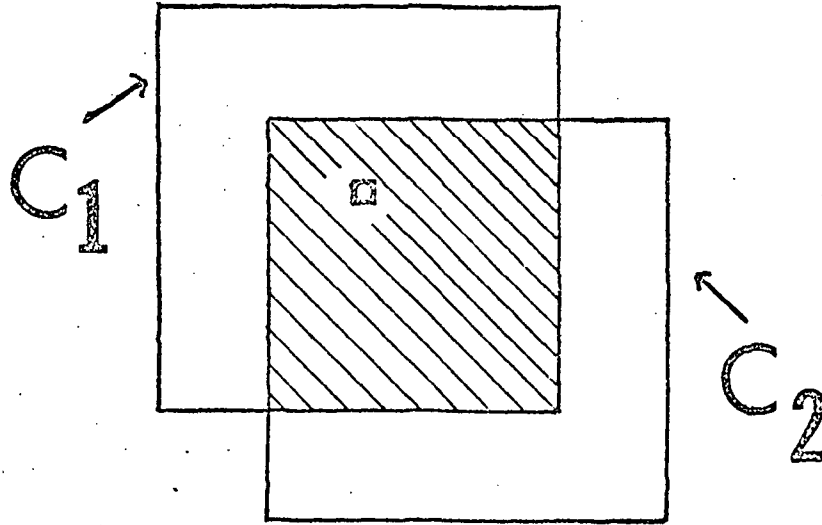
Shaded area represents intersection containing sub-surfaces which can be tested for congruency

Figure 4

ALIGNMENT OF TWO MATCH SURFACES AT COINCIDENCE OF BEST MATCH COEFFICIENTS

(N=168   JULY 26, 1969)

f

U COMPONENT

V COMPONENT
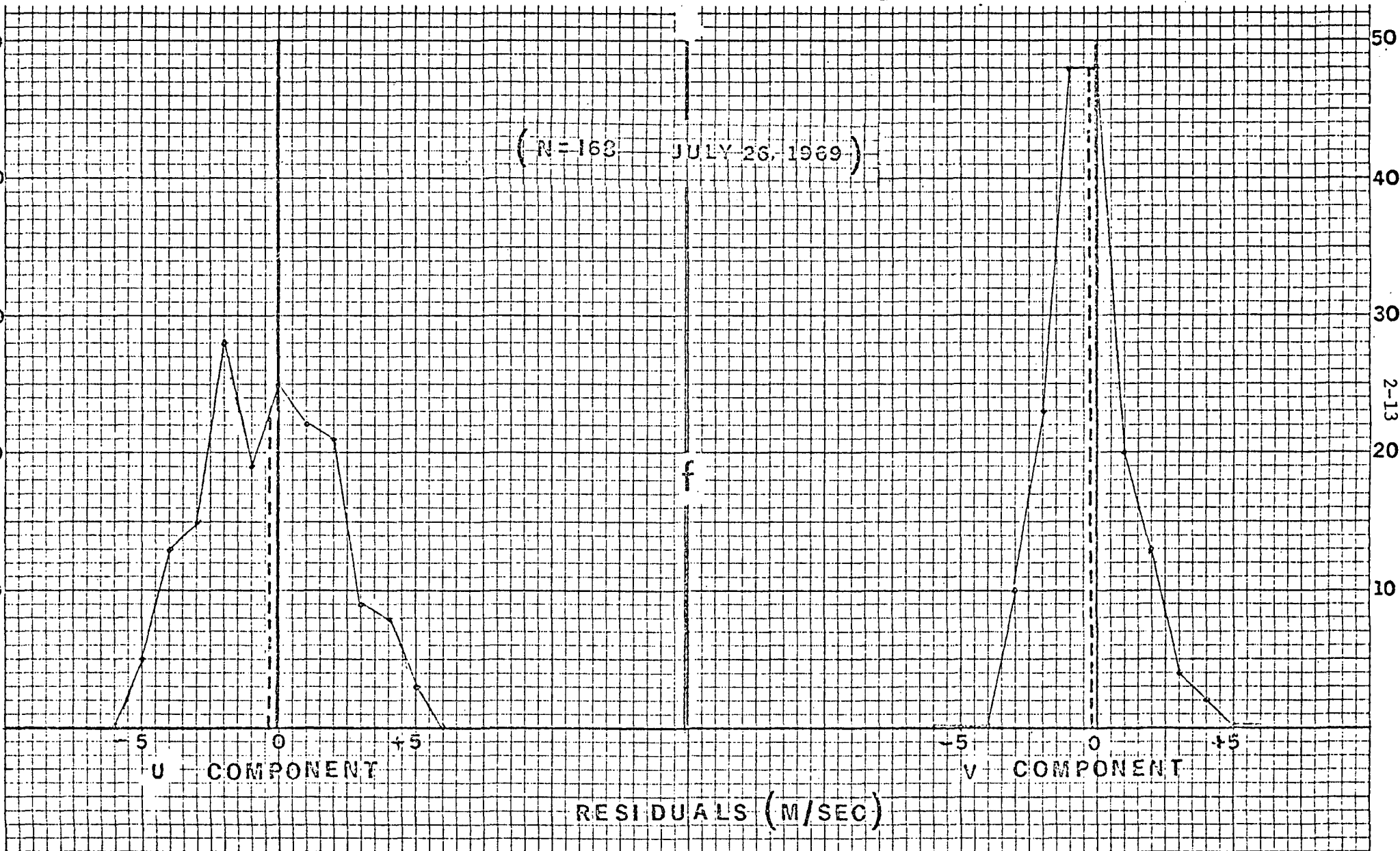
RESIDUALS (M/SEC)

Distribution means are given by dashed lines

Figure 5

U AND V VELOCITY RESIDUALS OF WIND SETS MEASURED OVER TWO INDEPENDENT TIME INTERVALS

· SMS CLOUD HEIGHTS

I.· INTRODUCTION

The determination of cloud height is important for many mete-
orological studies using satellite data. In the estimation of winds from
cloud tracers, the height of the cloud tracer is of fundamental importance.
One method of determining cloud height has been to obtain the temperature of
the cloud using an infrared radiometer on a spacecraft operating in a "window"
region of the infrared spectrum. Knowing the temperature of the cloud, one
can obtain the height of the cloud from a vertical temperature profile of the
area of interest. Fritz and Winston (1962), Rao and Winston (1963), and
Kuffler, DeCotiis, and Rao (1973) have developed procedures for estimating
cloud height from satellite infrared radiation data. A basic assumption
used in these procedures was that the clouds were opaque, and hence, had
emissivities equal to 1.

This method of determining heights has been reasonably successful for
a coarse height resolution, except for cirrus type clouds. Cirrus clouds
present the problem that their emissivity is not unity. Experimental studies
such as Kuhn (1963), Kuhn and Weickmann (1969), and theoretical studies such
as Jacobowits (1970), and Liou (1974) have shown that the emissivity of
cirrus clouds is substantially less than unity and varies with cloud thickness.

To improve the infrared estimate of a cloud top height, the emissivity of
the cloud needs to be obtained from some independent source. Using the fact
that both the visible reflectance and the infrared emissivity are dependent
upon the total number of cloud particles in a vertical column through the
cloud, Shenk and Curran (1973) have shown that cirrus cloud heights can be
determined to within $\pm$ 50 mb. The determination of optical thickness enables

one to determine the emissivity of the cloud. Knowing the emissivity of the cloud, the true temperature of the cloud top can be determined from the 10-12 micron infrared radiation. The height then follows from the temperature and a known vertical temperature profile.

II   DETERMINATION OF EMISSIVITY

The main difficulty in obtaining the emissivity of a cloud is the determination of the cloud thickness. This could be done by using a normalized reflectance which corrects for the effects of viewing and solar zenith angles. The thickness of the cloud can then be inferred from the brightness of the cloud.

The normalization of the light reflected from clouds is not a trivial matter. The reflected light from clouds depends upon several variables:

   a. The droplet size distribution and shape of the cloud particles.

   b. The number density of scattering particles in the cloud.

   c. The cloud thickness.

   d. The angular conditions of the measurement system (the zenith angles of the sun and the sensor and their relative azimuth angle).

   e. The shape of the cloud.

Since information on all the variables is not available to the satellite sensor, some of the effects must be parameterized in any normalization technique.

   A.   Brightness Normalization

There have been several approaches to normalization. The simplest has been to neglect all of the variables and assume the clouds are perfect isotropic reflectors and obey Lambert's law. The intensity of the reflected light will vary as the cosine of the solar zenith angle for an unchanging cloud. Martin and Soumi (1972) have shown that the tops of cumulonimbus clouds display a Lambertian behavior, and a cosine correction can be used to normalize the

brightness of thick cumulonimbus clouds.

There is, however, considerable evidence in the literature that neg-
lecting all the variables and assuming isotropic reflectance can lead to er-
roneous results. Bartman (1967), Ruff et al. (1968), and Brennan and Bandeen
(1970) have experimentally measured the scattering from clouds. They found
clouds generally show an anisotropic reflectance pattern which varies with
solar zenith angle. Normalization procedures based on this empirical data
base have been developed by Sikula and Vonder Haar (1972). The main problem
with this type of normalization has been the limited amount of empirical
data available. Since empirical data on the variation of the reflectance
pattern which is caused by variations in cloud thickness is generally not
available, the normalization procedures based on empirical data generally
have neglected the effects of cloud thickness.

To overcome the limitations of a restrictive data base, the
normalization procedure which has been developed at the Space Science and
Engineering Center, University of Wisconsin for the SMS/GOES data makes use
of a theoretical multiple scattering model to generate a large data base
for a large number of possible sun and observation angles. Data was
generated for 16 different thicknesses of clouds.

B. Multiple Scattering Model

The multiple scattering program which was used to generate the data base
of cloud reflectance patterns was a doubling method model developed by James
Hansen of NASA's Goddard Institute for Space Studies. The details of the
model are published in the January 1971 issue of the Journal of Atmospheric
Sciences. Results from the model are published in the November 1971 issue
of JAS (Hansen, 1971, a,b).

The doubling method works for a plane-parallel homogeneous cloud. Numer-

ical computations begin with a layer of such small optical thickness that scattering and transmission can be described by single scattering theory. The cloud thickness is built up by putting two layers together and computing the interactions that take place. The process of taking two layers, computing the transmission, reflection and interaction, combining the two into a single layer and then repeating the process for the new layer is the "doubling" procedure. By doubling, the thickness of the cloud increases by a factor of two after each computation, so very thick clouds can be generated quickly on the computer.

The single scattering phase function used as input to the multiple scattering doubling program was Deirmendjian's C-1 cloud model phase function. The forward scattering peak of the phase function was truncated and spread by the multiple scattering model (Hansen-Pollack, 1970). In the doubling model, 5 terms in the Fourier expansion were used, 3 terms in the sum over internal reflections between layers, 15 zenith angles were used for the Gauss quadrature integrations, and 37 azimuth angles were used. Conservative scattering was used with the local single scatter albedo set to unity.

The model as originally configured had the surface under the cloud as a perfectly absorbing black surface not accepting any other lower surface. While land and sea surfaces are dark compared to cloud, they are not entirely negligible, particularly for thin clouds. To include the sea surface brightness, the assumption was made that the light reflected from the sea was small compared to the light reflected from the thicker clouds, so that the energy which was lost by the light coming from the sea through the cloud toward the satellite did not interact with the light scattered originally in the cloud. The cloud scattering and the sea surface reflectance were computed separately and the results added.

The sea surface brightness was computed using sea surface albedo values

from Payne (1972). Payne performed an extensive experimental study of the albedo of the sea surface from a fixed platform and published tables of sea surface albedo as a function of the sun's altitude and atmospheric transmittance. To use these tables, the downward flux through the clouds and the atmospheric transmittance were computed. The flux impinging on the sea surface was then multiplied by the approximate albedo value to give a value for the flux propagating upwards from the sea surface. This upward flux was used as a new source of radiation and the directional transmittance to the satellite was computed using the multiple scattering program. The intensity of the sea surface was then added to the intensity of the cloud. Figure 1 shows the graph of intensity versus optical thickness with and without the sea surface brightness. As can be seen from the graph, the effect is significant for thin clouds.

The Rayleigh scattering of the atmosphere has been neglected in these calculations because its effect is smaller than the other effects. The sea surface brightness, as seen in Figure 1, is approximately .08. The brightness due to Rayleigh scattering for this geometry will be .018, a factor of four less.

At present the cloud height program only has a brightness data base of scattering from clouds with the sea surface beneath. This data base is presently used over land surfaces also. A similar data base for land areas could be added to the system in the future.

C. Parameterization of Variables

The amount of light scattered from real clouds depends upon the droplet size distribution of the cloud, the number density of scatters, the cloud thickness, the angular geometry of the sun and sensor, and the finite shape of the cloud. Some of these variables can be measured and used in the

VARIATION OF INTENSITY WITH AND
WITHOUT SEA SURFACE ALBEDO

$\Theta = 23°$
$\Theta_0 = 33°$
$\phi = 120°$

- - - INCLUDES SEA SURFACE ALBEDO
——— SEA SURFACE ALBEDO = 0

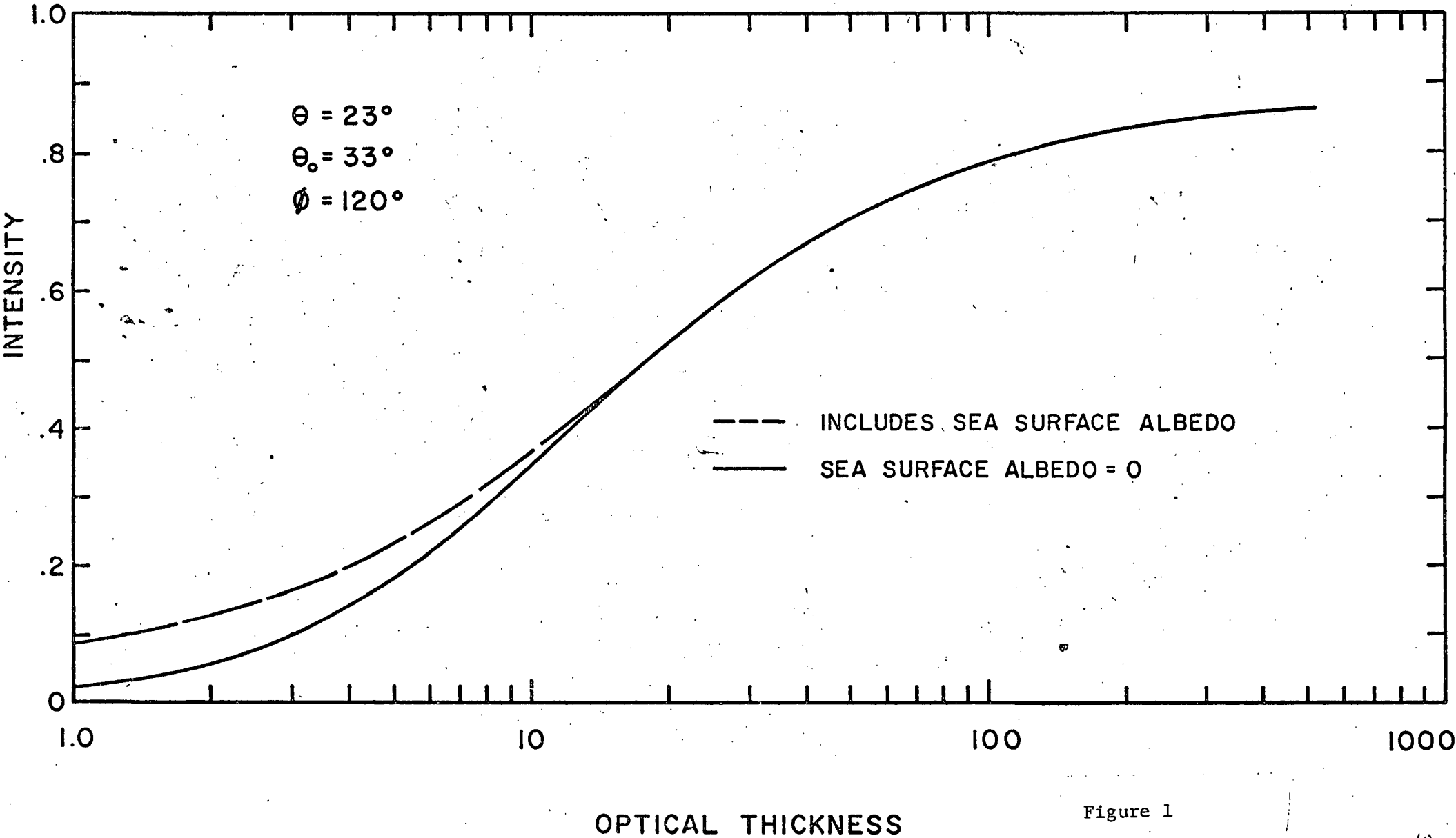INTENSITY

OPTICAL THICKNESS

Figure 1

normalization, but others must be parameterized.

The physical thickness and the number density of the droplets can be combined into the single variable of optical thickness:

$$\tau = KZ; \quad K = \sigma\rho$$

τ = optical thickness

Z = physical thickness

K = extinction coefficient

σ = scattering cross section

ρ = number density of scatters

The optical thickness τ of a layer is such that unit radiation normally incident upon the layer is reduced by single scatterimg in passing through to $e^{-\tau}$. The optical thickness, rather than the physical thickness, has been used in all the multiple scattering calculations since it combines the effects of the variables of number density and scattering cross sectional area.

The effect of variations in the particle size distribution on the intensity of light reflected from clouds is minor. The wavelength of the light is on the order of .5 microns. The particle size distribution of clouds have radii on the order of 5 to 10 microns (Diem, 1948). The droplets are very large compared to the wavelength of the light being scattered. The single scatter phase function has a very large forward scatter peak. Hansen (1971b) has shown in the near infrared that variations in the size of the particles do not greatly influence the multiple scattering intensities when the particles are large compared to the wavelength of the light. Figure 2 shows the variations in reflected intensity for visible light caused by differences in the particle size distribution for 4, 7, and 10 micron average radius particles. The phase functions for these particle distributions were generated by a Mie scattering program developed by James Hansen, NASA/GISS. The particle size

VARIATION OF INTENSITY
WITH PARTICLE SIZE

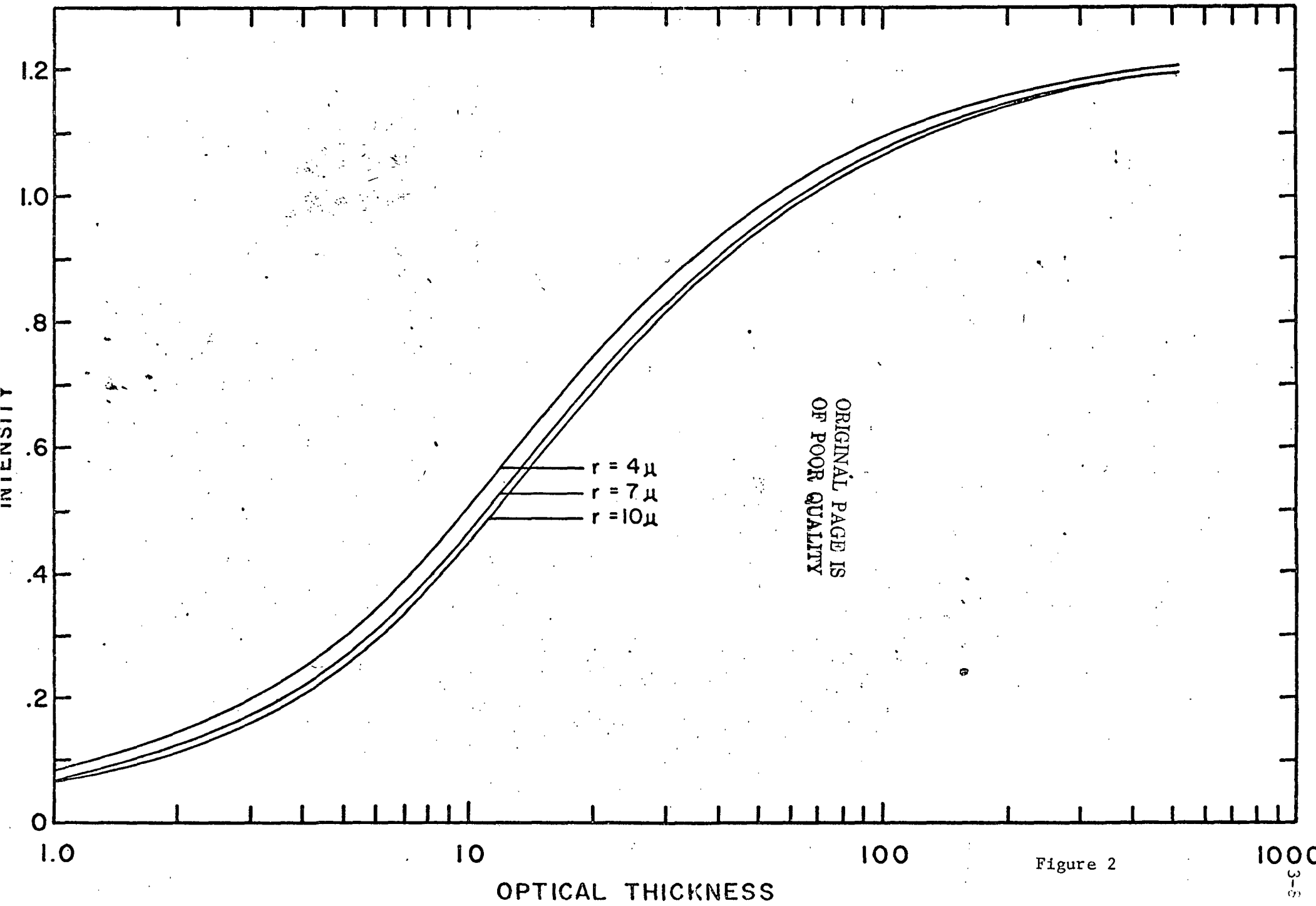
Figure 2

r = 4μ
r = 7μ
r = 10μ

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distributions of each had a variance of .111. The particle size distribution

used was a variation of the gamma distribution (Hansen, 1973b). The vertical

axis in Figure 2 is intensity in theoretical units for an input flux of π,

while the horizontal axis is optical thickness. The sun and the sensor

both had a zenith angle of 0°. A 12 micron average radius particle size

distribution was also computed, but its curve for Figure 2 was indistinguishable

from the 10 micron curve. Consequently, for this study the variation of

intensities of scattered light caused by variations in the particle size

distribution has been neglected. The 4 micron average radius distribution

of Diermendjian was chosen to represent all clouds including cirrus.

The effects of the shape of the clouds is largely unknown. The

plane-parallel cloud which was used in the theoretical multiple-scattering

doubling program had no horizontal limits. Experimental measurements of

scattering from clouds such as Bartman (1967) and Brennan and Bandeen (1970)

generally use stratus type clouds which also have no horizontal limits. For

clouds with vertical extent approximately equal to their horizontal extent,

such as cumulus clouds, some light energy should be lost or gained through the

sides in addition to what comes through the top and bottoms. McKee and Cox (1974)

have performed a study on the effects of the finite shaped clouds by using a

Monte Carlo multiple scattering program on a cube. The angular resolution of

their study was limited to light leaving the top, side, and bottom of the cube.

Their results show that the upward reflected light from the cube is about 25%

less than for the semi-infinite cloud. However, their angular resolution was

not sufficient to distinguish between the intensity of light coming from the

top center and the intensity coming from the top edges. One would expect

more light to escape from the edges than from the middle and a gradient of

brightness should be established due to the light escaping out the sides. Unfortunately, there is presently no data available on this problem. Consequently, for this study, the intensities from the doubling program, which uses a semi-infinite horizontal extent cloud, will be used. Although there will be some errors at the edges of the clouds, the errors at the centers of the clouds should be small.

The parameters related to the angles of the sun and the sensor can easily be calculated with the knowledge of the position of the cloud, position of the satellite, and the position of the sun. Since a wind measurement using cloud tracers already requires an accurate navigation of the satellite, the information required to calculate the angle of the measurement is readily at hand.

In determining the scattered intensity of the cloud, the variables have been reduced to optical thickness and angles. The effect of particle size distribution is small and the effect of finite size of clouds has been neglected. The determination of cloud thickness, and the implied normalization which takes place, can be performed by taking the intensity measurement from a calibrated satellite and converting it to optical thickness through use of the tables of intensity versus optical thickness generated by the multiple scattering program. This optical thickness can therefore be used in the determination of the emissivity of the cloud.

D.   Calibration of the Satellite Sensor

Unfortunately, like the Applications Technology Satellites (ATS) the SMS/GOES satellite lacks an on board calibration for the visible sensors. To perform quantitative radiance calculations, such as determination of cloud thickness, the satellite must be calibrated. To calibrate a satellite in orbit, a landmark of known brightness must be found. Previous

attempts at calibration include using the moon (Hansen, 1968), White Sands,

New Mexico and the South American salt flat Solar de Uyuni (Griffith and

Woodley, 1973). Calibrations using these landmarks have been hampered by the

lack of detailed knowledge of the bi-directional reflectivity characteristics

of these landmarks.

This study has taken a different approach at calibration of satellite

images. Figure 3 shows an example of intensity versus optical thickness for

the case of a solar zenith angle of 35°, satellite zenith angle of 20°, and

relative azimuth angle of 50°. As can be seen from the figure, as the cloud

becomes very thick, the intensity approaches a limiting value. The

fact that clouds become intensity saturated and reach a limiting value has

been the basis for a satellite calibration technique. Using the multiple

scattering program, it was determined that the optical thickness 512 has a

brightness which is within 3% of the ultimate limiting brightness. A cloud

with optical thickness 512, droplets of 10 micron diameter, and droplet

density of 250 droplets/cm^3 (as is representative of a large convective cloud)

would have a physical thickness on the order of 14 km or 40,000 feet. Conse-

quently, if edge effects can be neglected, any well-developed thunderstorm

or tropical cloud cluster should have an intensity within 3% of the brightness

of an infinitely thick cloud observed under the same sun and satellite angles.

Small variations in the physical thickness should not make much difference in

the brightness of these very thick clouds.

The calibration procedure used in this study involved selecting a very

bright thick cloud and assigning it an optical thickness of 512. The ratio of

the theoretical intensity of a cloud of optical thickness 512 to the measured

intensity of the very thick cloud was designated the calibration factor alpha

(α). With this calibration factor, any measured intensity can be converted

into theoretical units by multiplying it by alpha.

VARIATION OF THE BRIGHTNESS OF A PLANE PARALLEL CLOUD WITH CHANGES IN THE OPTICAL THICKNESS OF THE CLOUD
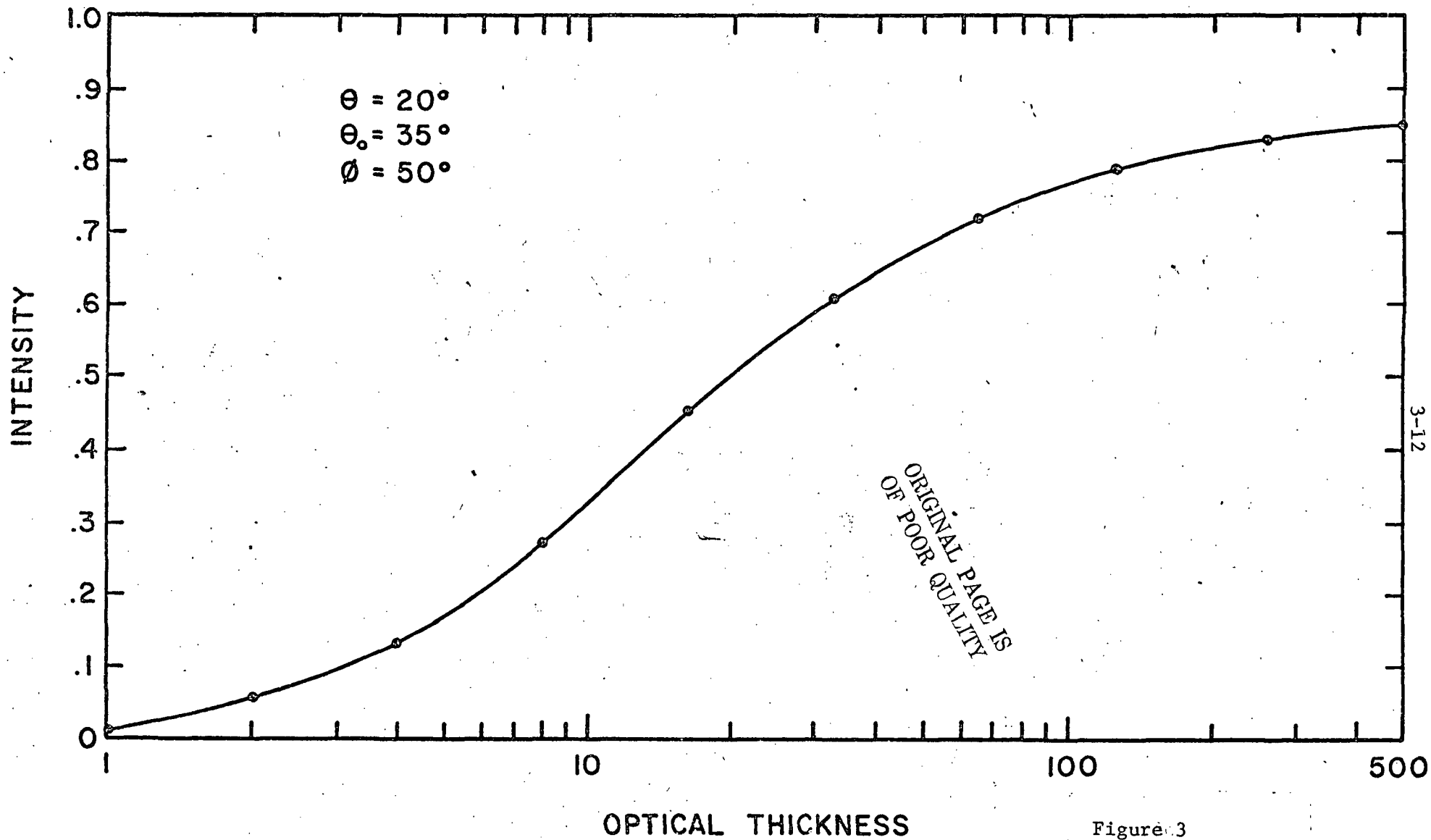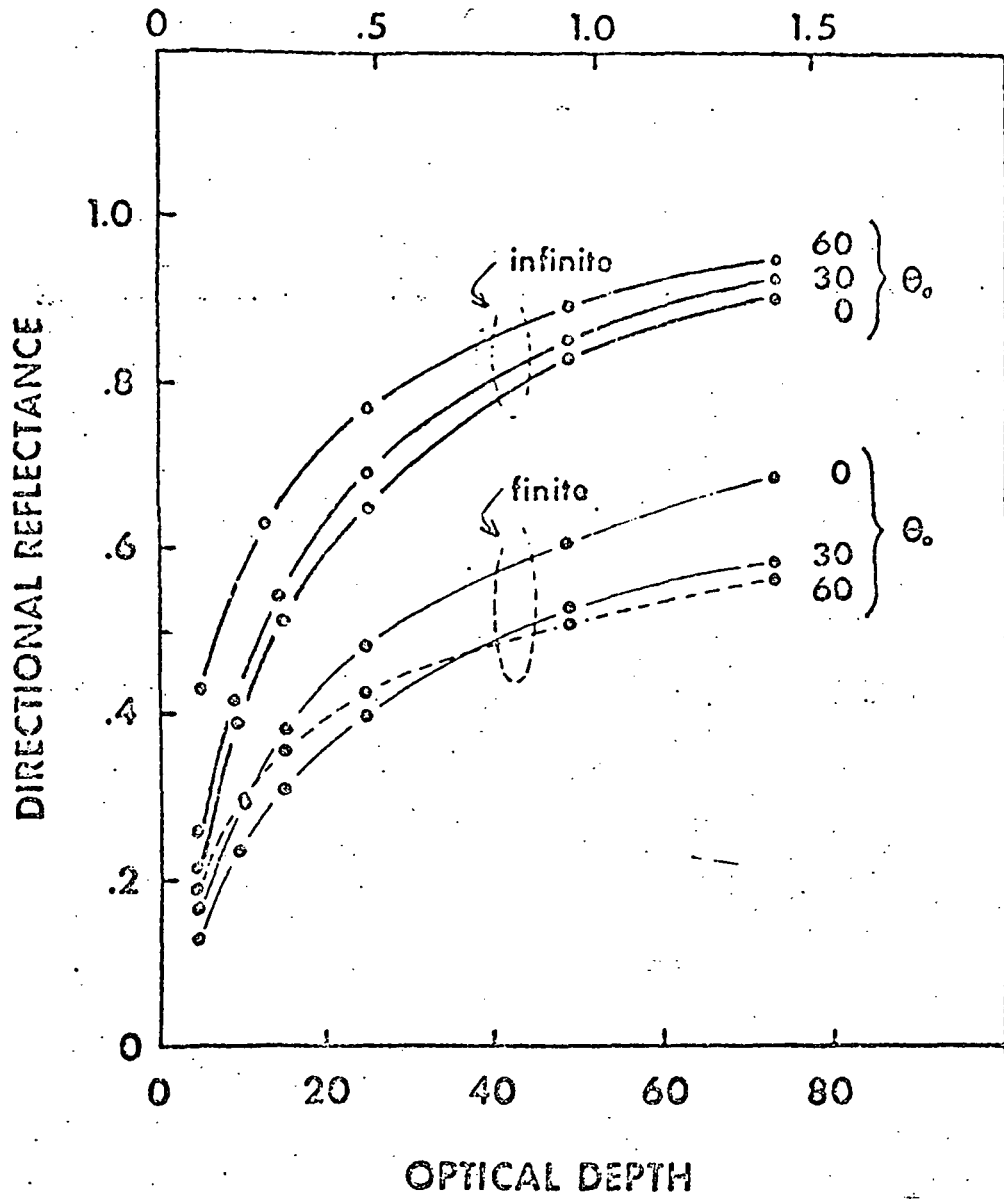

Figure 3

3-12

A check on the assumption that variations in cloud thickness has little

effect on the intensity of these thick calibration clouds was made by using

clouds with known heights from radar as calibration clouds for ATS III data.

A preliminary calibration check involved thunderstorms in the Miami area with

tops ranging from 44,000 feet to 51,000 feet. The standard deviation of

the calibration factors for these clouds was within 2% of the mean calibration

factor. Selection of calibration clouds from different parts of the earth so

that the local time, satellite, and sun angles would vary did not appreciably

affect the consistent determination of alpha.

When the calibration factor α determined from deep convective

clouds was used in the determination of the emissivity of clouds as is

described later in this report, the calculations gave an emissivity of

cirrus clouds equal to unity. The clouds, therefore, were too thick. If,

however, the calibration factor α was reduced from the measured .8 to .45,

the emissivity calculations showed reasonable results. The reduction in the

calibration factor would be necessary if the deep convective clouds used

for calibration were losing light from their sides. The study by McKee-Cox

(1974) showed that light does leak out the sides of finite cubic clouds.

Figure 4 reproduces a graph from their report showing the comparison of the

infinite horizontal extent cloud and the finite cubic cloud using a Monte Carlo

multiple scattering technique. When the doubling method multiple scattering

intensities used in this study are converted into the directional reflectance

to conform to the convention of McKee and Cox, the doubling results agree

closely with the infinite case of the Monte Carlo results. The reduction of

the calibration factor therefore is consistent with the results of McKee and Cox.

E.   Infrared Emissivity of Water and Ice Clouds

The infrared emissivity of clouds has been calculated using Kirchhoff's

Figure 4: Directional reflectance of infinite clouds and
finite cubic clouds. The upper abscissa is the
geometric thickness (km) for a 0.2 gm m^{-2} model
cloud. (from McKee and Cox, 1974)

law, equating the emissivity to the absorptivity. The absorptivity of

the cloud was calculated from the radiative transfer through the cloud by

the multiple scattering program configured to compute fluxes.

The infrared radiative transfer through a cloud is influenced by the size

and shapes of the scattering particles, and the real and imaginary parts of

the refractive index. The real part of the index of refraction is the para-

meter usually called the index of refraction in optics. The imaginary part

of the index of refraction is related to the absorption of light by the

scattering particles. Using Mie scattering theory the three fundamental

optical parameters (the phase function, the single scatter albedo and the

extinction cross section) can be computed from the particle size distribution

and the index of refraction. While Liou (1973) has computed Mie theory para-

meters for ice cylinders, most studies, including this one, have used spheres

in the Mie theory calculations. The Mie theory calculations in this report

were made using the Mie scattering program developed by James Hansen of NASA/

GISS. The single scatter albedo calculated from Mie theory is the fraction

of the energy incident on a single particle which is scattered. In the

visible regions of the spectrum, the single scatter albedo is unity with

no absorption. In the infrared regions, the single scatter is less than one,

so absorption occurs during scattering events. Table 1 shows the dependence

of the single scatter albedo on the particle size distribution for spheres

of ice and water with light of wavelength 11.5µ incident on them. The indices

of refraction were taken from Irvine and Pollack (1968). The imaginery part

of the index of refraction for ice in the portion of the tables for 10µ–12µ

of Irvine and Pollack appears to contain an error. The data

should be a factor of 10 larger. The initial calculations of this study used

the value of the imaginary part which was listed in the original paper,

but all the calculations using the ice calculations have been re-done using

Table 1

Ice Spheres

Average Radius	Single Scatter Albedo
30μ	.497
50μ	.510
80μ	.520
120μ	.526

Water Droplets

| 4μ	.240
10μ	.409
30μ	.484
50μ	.492

the correct value.

The emissivity of the clouds was calculated using the multiple scattering program configured to compute fluxes. The transmitted downward flux was computed at the bottom of the cloud and the reflected upward flux at the top of the cloud was computed for normally incident unit flux, The absorption was obtained from the difference between the incident flux and transmitted and reflected fluxes. The emissivity was set equal to the absorption. Figure 5 shows the variation of emissivity versus optical thickness for droplets of 4 to 10μ radius for 11.5μ radiation. Figure 6 shows the same for ice spheres. Since the single scatter albedo does not vary appreciably for variations in the sizes of ice spheres, the curve shown in Figure 6 is valid for all sizes of ice particles.

III. CLOUD HEIGHT PROGRAM

A. Methods of Height Computation for Different Types of Clouds

The cloud height program developed from the information of the preceding sections was written as a subroutine of the WINDCO cloud tracking program of the Space Science and Engineering Center. The cloud height program was designed so that the height of each tracer cloud would be determined automatically during the processing of the cloud tracking. The subroutine determines the height of wind tracer clouds by using the visible brightness to determine the thickness of the cloud. From the cloud thickness, the emissivity of the cloud is determined. Knowing the emissivity, the true temperature of the cloud top can then be determined. The height is gotten from a standard atmosphere of temperature vs. height, corrected for latitude and date. The height computation for each cloud adds about 1 second of processing time to the wind computation.

WATER DROPLETS

$\bar{r} = 4\mu$

$\bar{r} = 10\mu$

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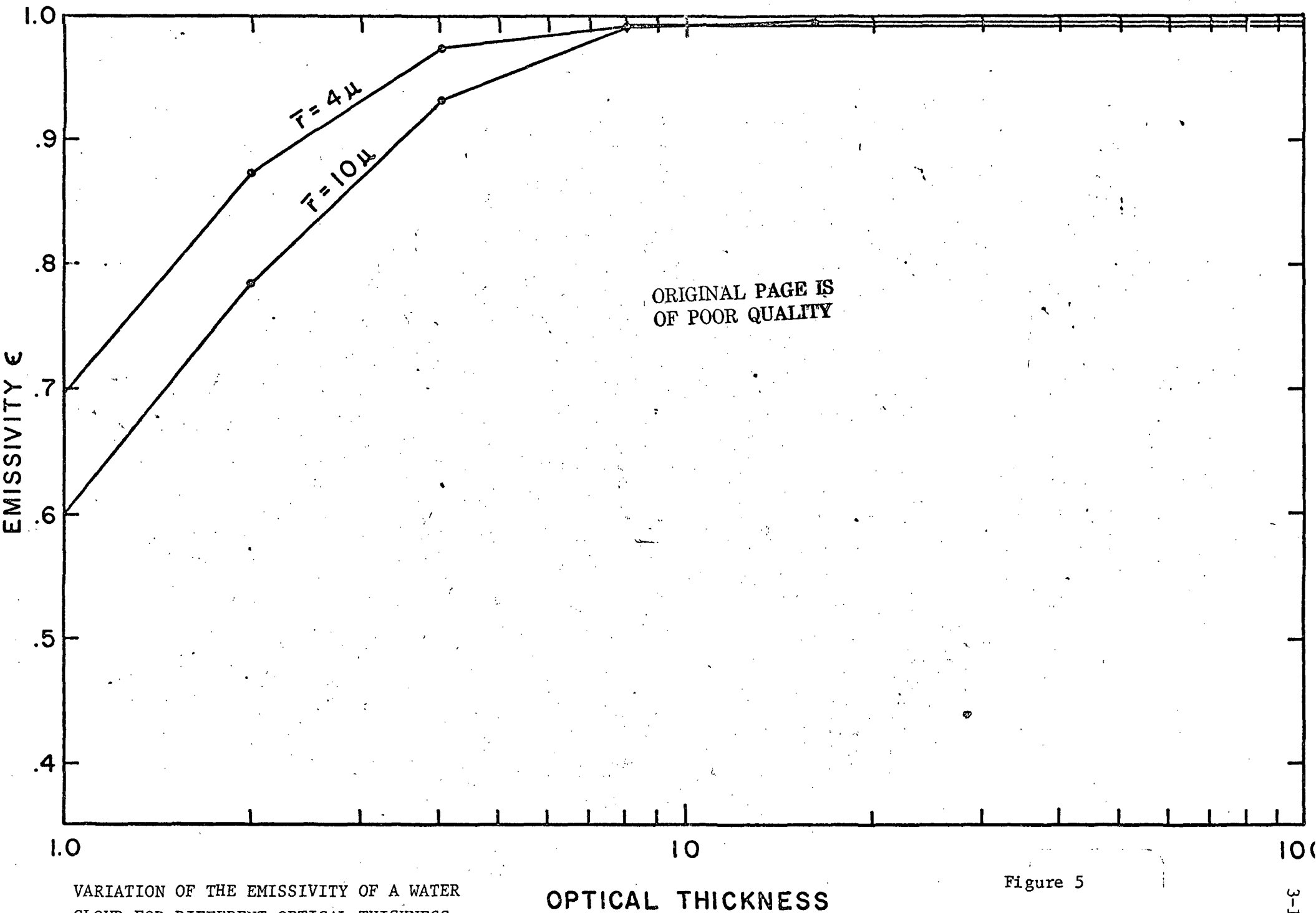
VARIATION OF THE EMISSIVITY OF A WATER
CLOUD FOR DIFFERENT OPTICAL THICKNESS

OPTICAL THICKNESS

EMISSIVITY ε

Figure 5

3-18

ICE SPHERES
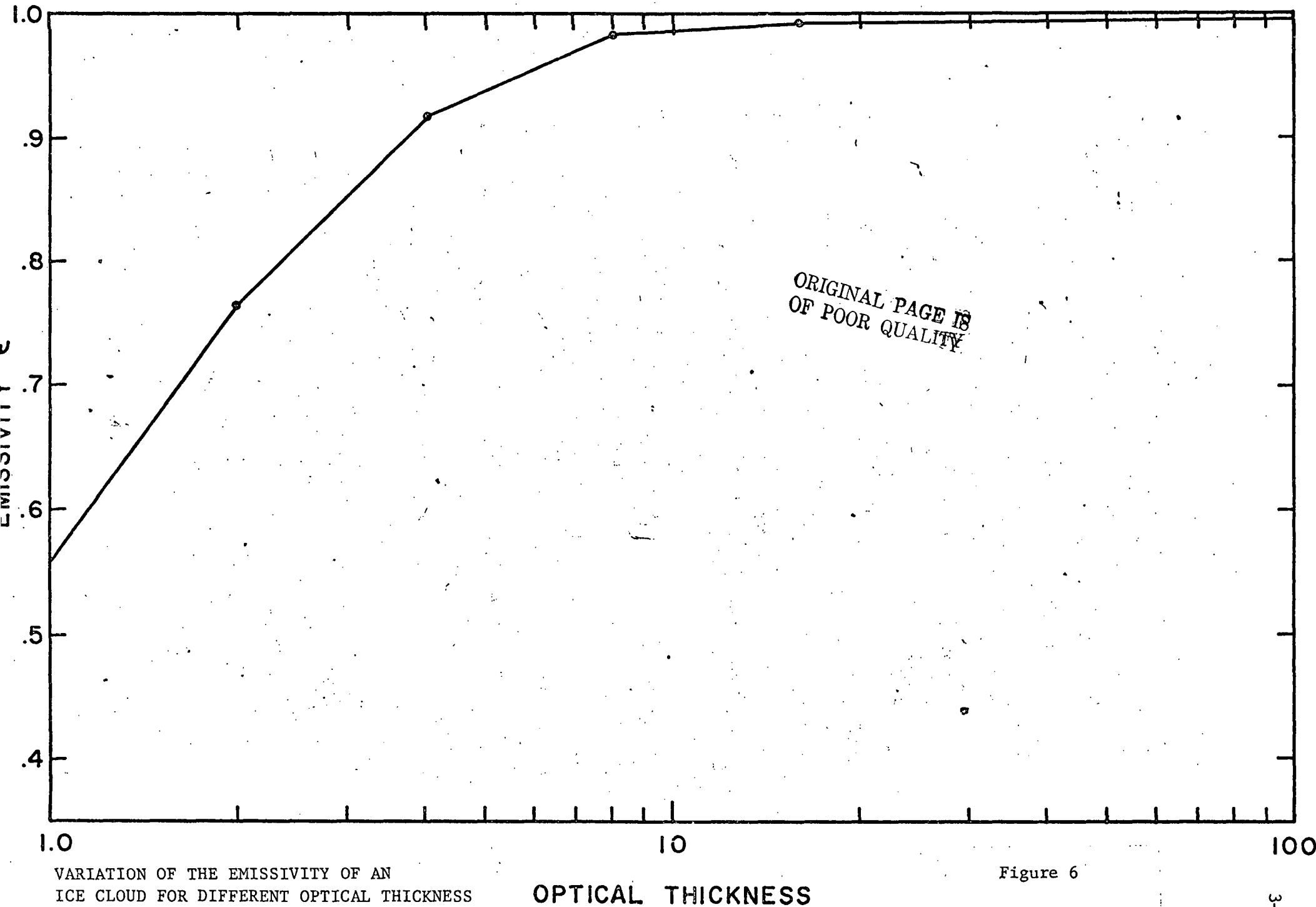
VARIATION OF THE EMISSIVITY OF AN
ICE CLOUD FOR DIFFERENT OPTICAL THICKNESS

OPTICAL THICKNESS

Figure 6

The cloud height program is configured to perform three passes at the cloud tracer. The first pass determines whether the center of the cloud can be considered blackbody. The optical thickness of the center pixel is computed, and the emissivity is computed from the optical thickness. If the emissivity is greater than .94 the cloud is considered to be blackbody and the blackbody temperature of the center pixel is used directly to compute the height of the tracer cloud.

If the first pass fails because of non-unity emissivity of the center pixel, a second pass at the data is performed. This second pass inquires if the cursor was not centered on the cloud, and a cloud with unity emissivity lies within the target grid of the cursor. A histogram of the brightness values of the target grid is computed, and the brightness cutoff for the brightest 20% of the population is determined. The entire data array is searched, and for each pixel brighter than the cutoff intensity, its emissivity is computed. For the subset of the 20% of the array's pixels, the average intensity and average emissivity is computed. If the average emissivity is greater than .94, the cloud is considered blackbody and the average radiative temperature of this 20% sample is used to obtain the height of the cloud.

If the first two passes at the data fail, the cloud is too thin to be considered a blackbody, and it is necessary to solve for the radiation coming from the cloud. Two areas in the target grid are needed to do this. The assumption is made that the ground in both areas has the same temperature, and the cloud cover for both areas is at the same height. The radiation reaching the infrared sensor for area 1 and 2 is

$$I_1 = I_g(1-N_1) + \varepsilon_1 N_1 I_c + (1-\varepsilon_1)N_1 I_g \qquad (1)$$

$$I_2 = I_g(1-N_2) + \varepsilon_2 N_2 I_c + (1-\varepsilon_2)N_2 I_g \qquad (2)$$

with I_g = radiation coming from the ground

I_c = radiation coming from the cloud cover

N = fractional cloud cover

ε = emissivity

Subscripts 1 and 2 refer to areas 1 and 2.

Assuming that the fractional cloud cover and the emissivities can be measured, there are two equations with two unknowns, I_g and I_c. Solving for the radiation coming from the cloud yields:

$$I_c = \frac{I_1(1-N_2\varepsilon_2) - I_2(1-N_1\varepsilon_1)}{\varepsilon_1 N_1 - \varepsilon_2 N_2} \quad (3)$$

The two areas in the target grid are selected by finding the visible brightest and dimmest areas of the target grid. The brightest area (1) will have radiation mainly from the cloud while the dimmest area (2) will have radiation mainly from the ground. Equation 3 can be solved with a minimum of error this way.

The fractional cloud cover is determined from the visible. The two areas each cover 32 visible pixels. The spatial resolution of the visible sensor has a strong effect on the estimates of the percentage of cloud cover. A study by Shenk and Salomonson (1971) showed that if a cloud/no cloud threshold technique is used to determine percentage cloud cover, the cloud must be 100 times larger than the spatial resolution for the calculated percentage to be within 10% of the true percentage. This study also showed if a two threshold approach (all cloud/50% cloud/no cloud) is taken, the cloud must only be 10 times larger than the resolution of the camera.

The fractional cloud cover routine used in the cloud height program is a modification of the two threshold approach. The fractional cloud cover is

calculated for each pixel and a running sum kept. To obtain the

fractional cloud cover of a single visible pixel an arbitrary threshold of

optical thickness 1 was established. Cloud pixels whose measured brightness

corresponded to an optical thickness greater than 1 were considered

completely covered with clouds. Pixels with the brightness of the sea

surface were considered to have no cloud cover. For pixels whose brightness

was between these two thresholds, the fractional cloud cover was considered

to be proportional to the optical thickness. The infrared radiances and

emissivities used in equation (3) are averages from each of the two areas.

B. Method of computing optical thickness

The optical thickness of a cloud is determined from the brightness of

the cloud. A multiple scattering program using the doubling method developed

by James Hansen of NASA/GISS was used as the source of data for the conversion

between brightness and optical thickness. Since the McIDAS Datacraft computer

is too small to run the multiple scattering program, a large table of 77,824

intensities was generated on the University of Wisconsin's UNIVAC 1110 and

stored on the McIDAS digital disk. This represents all possible combinations

of 16 solar zenith angles, 16 satellite zenith angles, 19 relative azimuth

angles, and 16 optical thicknesses. The received SMS visible data has a

six bit word with a square root digitization. To deal with a linear

brightness scale, the SMS data is squared, giving a 12 bit word. The

table of intensities has been multiplied by a scaling factor of 3166.9 prior

to storage so that a 12 bit integer word which matches the SMS intensity

resolution can be achieved. The height program first determines the solar

zenith angle, satellite zenith angle, and the relative azimuth angle for the

center of the cloud being tracked. The conversion of any visible pixel in

that cloud from brightness to optical thickness is done by using the large table

of intensities. Since the table only holds data at finite angles, an interpolation must be performed to obtain the optical thickness for a unique set of input angles. The program first generates a table of 16 intensities for 16 standard optical thicknesses by doing a linear interpolation from data on the digital disc. The intensity I, which is a function of sun angle θ_o, satellite angle θ, azimuth angle ϕ, and optical thickness τ, can be determined by

$$I_{(\theta, \theta_o, \phi, \tau)} = \left(\frac{\partial I}{\partial \theta}\right)_{\theta_o, \phi, \tau} d\theta + \left(\frac{\partial I}{\partial \theta_o}\right)_{\theta, \phi, \tau} d\theta_o + \left(\frac{\partial I}{\partial \phi}\right)_{\theta_o, \theta, \tau} d\phi + \left(\frac{\partial I}{\partial \tau}\right)_{\theta, \theta_o, \phi} d\tau + I_{(\theta_1, \theta_{o_1}, \phi_1, \tau_1)}$$

with $I_{(\theta_1, \theta_{o_1}, \phi_1, \tau_1)}$ being known.

For a constant optical thickness the intensity I can be obtained by finite differences as

$$I_{(\theta, \theta_o, \phi)} = \frac{\Delta I}{\Delta \theta}\bigg|_{\theta_o, \phi} (\theta - \theta_1) + \frac{\Delta I}{\Delta \theta_o}\bigg|_{\theta, \phi} (\theta_o - \theta_{o_1}) + \frac{\Delta I}{\Delta \theta_o}\bigg|_{\theta, \theta_o} (\phi - \phi_1) + I_{(\theta_1, \theta_{o_1}, \phi_1)}$$

In the partial derivatives, i.e., $\frac{\Delta I}{\Delta \theta}\bigg|_{\theta_o, \phi}$, the quantities θ_o and ϕ are held constant. Since there are only values of I at finite values of θ_{o_1} and θ_{o_2}, ϕ, and ϕ_2 available on either side of θ_o and ϕ, the finite values closest to θ and ϕ were chosen for the derivatives. The calibration factor of the visible sensor is then used to convert the observed brightness into the same units as the intensities on the digital disk. Then a linear interpolation is performed on the table of 16 intensities for 16 standard optical thicknesses to convert the observed brightness into optical thickness.

C. Method of Computing Cloud Emissivity

Once the optical thickness of a tracer cloud pixel has been determined, the emissivity at 11.5μ for that optical thickness is computed. The

program uses a table of emissivity vs. optical thickness for a water droplet particle size distribution with average radius of 4 microns, and an ice sphere particle size distribution. Figures 5 and 6 of this report show these curves. Since these curves differ slightly, a method of distinguishing between ice and water clouds is necessary.

The cloud type identification routine used in this program makes the assumption that any cloud with a true temperature higher than 250°K is a water cloud, and any cloud with temperature lower is an ice cloud. Using an assumed surface temperature of 295°K and homogeneous clouds, curves of the apparent blackbody temperature of these cloud were generated using:

$$I_{received} = \varepsilon I_{cloud} + (1-\varepsilon)I_{ground}$$

and Plank's law

$$I = \frac{C_1}{\lambda^5} \frac{1}{\exp(\frac{C_2}{\lambda T}) - 1}$$

Figure 7 shows the curves for ice and water clouds. As can be seen from the curves, they do not agree and there is an area of ambiguity between the two curves for small optical thicknesses. The apparent blackbody temperature for ice clouds can be warmer than for water clouds. The operator supplied flag of the height guess is used to help resolve this ambiguity.

The program uses linear interpolation to generate the point on the curves which correspond to the input optical thickness. If the input measured blackbody radiative temperature is colder than the water curve, the cloud is definitely an ice cloud. If the input temperature is warmer than the ice curve, it is a water cloud. If the input temperature lies between the two curves where the ambiguity occurs, the operator's height guess is checked. If the height guess is less than 500 mb, the cloud is assigned an ice type. Otherwise, it is assigned a water type.

APPARENT BLACKBODY TEMPERATURE OF CLOUDS FOR DIFFERENT OPTICAL THICKNESSES
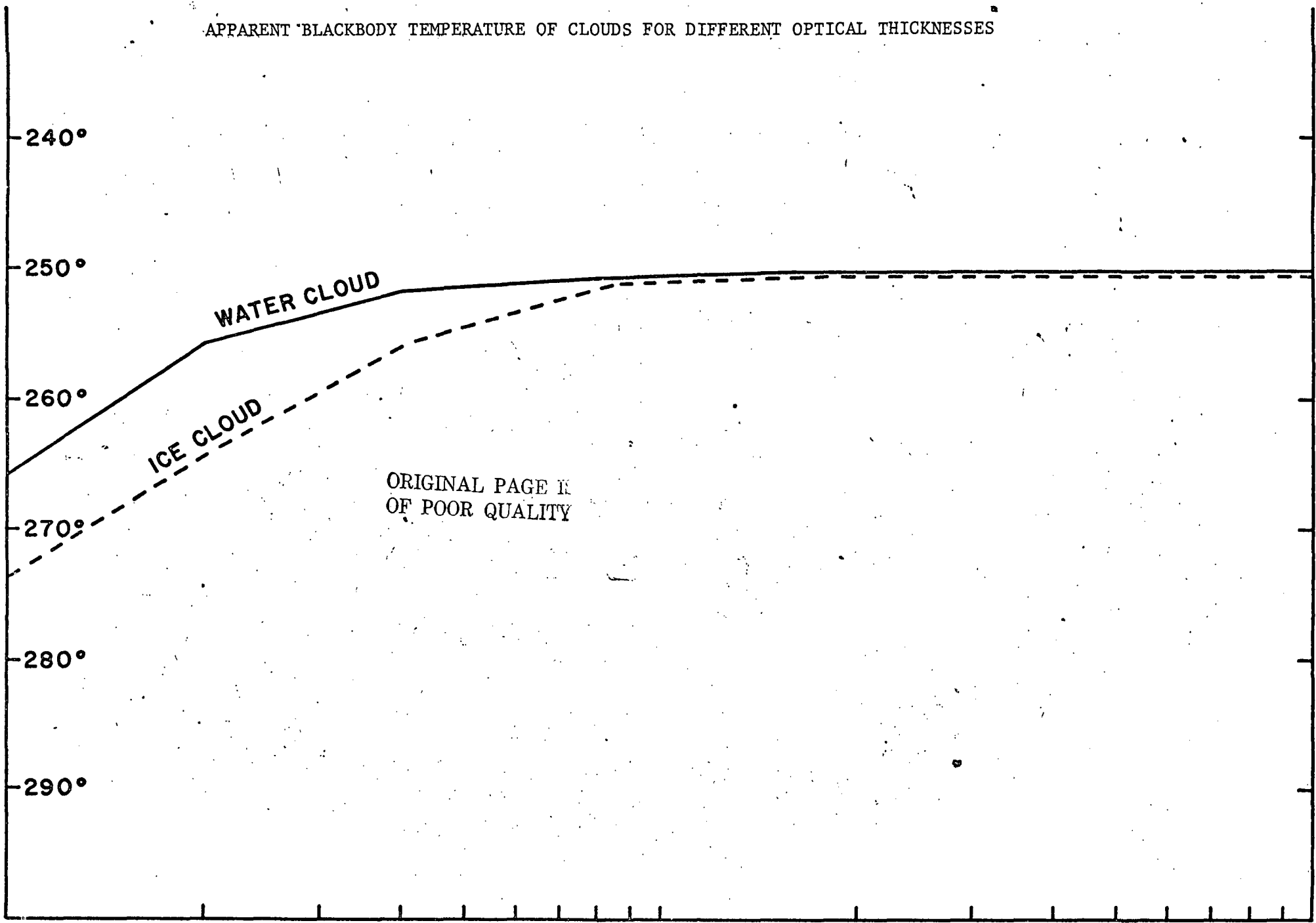
Figure 7

Once the type of cloud has been established, the emissivity of the cloud is calculated by linear interpolation of the emissivity tables.

D. Method of Converting Between Temperature and Height

The height program computes the true temperature of the cloud top. To convert from temperature to height, a sounding of temperature vs. height is necessary. Ideally, current synoptic soundings should be used for this task, but unfortunately, the Space Science and Engineering Center does not presently have access to world wide synoptic soundings. The cloud height program uses standard atmospheres corrected for latitude and the time of year. Standard atmospheres for latitudes 15°, 30°, 45°, 60°, and 75° for January and July are used. The standard atmospheres extend up to the tropopause, but inversions have been made almost isothermal so as to produce a function of temperature which is single valued with height. A linear interpolation of soundings is made between latitudes for the two times of the year, January and July. Then an interpolation using a cosine function is performed to correct the standard atmosphere soundings to the current data of the cloud tracer.

If current synoptic soundings were made available, the cloud program could easily use them. The program was constructed using a modular design. The conversion from temperature to height is a separate subroutine which could easily be replaced with one which uses current soundings instead of standard atmospheres.

E. Nighttime Heights

During nighttime cloud tracking operations, only the infrared channel is available. Hence there is no information available from the visible channel for the determination of cloud thickness and cloud emissivity. Preliminary analysis of the SMS infrared images coupled with the visible images show that there are no immediately obvious clues (such as area,

texture, etc.) which exist in the infrared image which could be used to determine the emissivity of the cloud in an automatic height determination system. Consequently the preliminary nighttime heights algorithm has been kept simple and uses the blackbody assumption. The center pixel of the cloud is used to determine the height. This algorithm will be used until the statistical error analysis algorithms have been completed and studies can be done on nighttime algorithm improvements such as searching for the coldest area of the cloud, averaging techniques, and manual guessing of the emissivity.

IV. OPERATION AND ASSESSMENT OF CLOUD HEIGHT SYSTEM

The cloud height system was installed on the McIDAS system in August 1974, and received its first major use during the Data System Test of October 28-November 1, 1974. The cloud height system is configured so that the heights of the tracer clouds are computed automatically as the operator selects the candidate cloud tracers. No additional effort is required of the operator beyond setting up the initial conditions of the processing and the selection of the cloud tracers. The cloud height system can also be used separately from the cloud tracking system. The operator can put the cursor over the cloud of interest, press H on the keyboard, and the cloud height in kilometers and millibars plus some diagnostics will be displayed. Other diagnostic commands are also available.

The cloud height program uses some simplifications and parameterizations of the clouds whose heights are being measured (such as parameterization of particle size distributions of clouds, horizontal homogeneous assumption, etc.) which result in an accuracy of the cloud height system of no better than ± 50 mb. Preliminary analysis of the consistency of the height

computation over two consecutive picture pairs shows this error expectation

to be reasonable for the lower clouds, but the upper level clouds might have

relative errors as large as ±100 mb for the present configuration of the

cloud height system.

The absolute accuracy of the cloud height system is at present unknown.

Requests have been made for aircraft observations of cloud top height,

cloud base height, and the temperature of the cloud, but we have not yet

received any of these reports. The winds produced during the Data System

Test of October 28-November 1 were transmitted to the National Meteorological

Center (NMC) by way of NASA's Goddard Institute of Space Studies. The

validation analysis of these wind sets by NMC has not been made available yet.

The absolute accuracy of any height determination depends upon the

absolute accuracy of the VISSR thermal channel calibration on the SMS/GOES

satellite. While the system has an onboard calibration system, problems

such as unexpected thermal gradients continue to limit absolute accuracy

of the system. During the times of eclipse in the fall and spring,

diurnal variations in the sensitivity of the instrument can cause

diurnal errors of 3.5°K for warm sea surface measurements. A long term

drift of sensitivity of the instrument has caused errors as large as 5°K

in sea surface measurements. Cloud temperature errors were somewhat less

than this. A new thermal channel calibration was applied to the satellite

on October 31, 1974.

To obtain a preliminary idea on the performance of the cloud height

accuracy, plots of the wind fields generated from cloud motions were

compared against plots of wind fields measured by radiosondes over the

United States. These plots are shown in Figures 8-13. The winds generated

by the cloud motions have been divided into three groups, (surface-800 mb,

700-500 mb, and 400-100 mb). The heights assigned to the individual vectors

are plotted next to the vectors. The heights are in hundreds of millibars so 0=near surface, 9=900 mb, etc. The radiosonde winds are for 1200Z of October 30, 1974. The cloud winds are for 1400-1500Z. The sunrise line is just to the west of the wind measurements on the surface-800 mb plot of cloud winds. Measurements of upper level winds west of this line were made using only the IR channel. As can be seen by the visual comparison of the McIDAS cloud winds and the radiosonde winds, there appears to be good agreement between the two types of measurements.

Work has started on a verification against radiosondes and an error analysis system for height and wind determinations. When this system has been completed, a much better assessment of the accuracy of the cloud heights will be available.

V. SUMMARY

A cloud height determination system has been developed which takes into account the variable emissivity properties of clouds. The visible brightness of the cloud is used to calculate the optical thickness. The optical thickness is used to compute the infrared emissivity of the cloud. The true temperature of the cloud can be calculated using the emissivity. From the temperature of the cloud and a sounding, the height can be determined. The cloud height system is operational and is coupled to the WINDCO cloud tracking system so that the heights of tracer clouds are computed automatically along with the wind computation. The height computation adds approximately 1 second to each wind calculation time.

VI. RECOMMENDATIONS FOR IMPROVEMENTS

The cloud height system at present is usable and appears to give good results. However, there are several areas which could use some more work for

improving the system.

A. Verification and Error Analysis

The cloud height and wind determination systems need scientific

verification. Verification is not a trivial problem and deserves a

serious effort. Verification needs to be made against "primary" standards

such as independent aircraft measurements of cloud height and motions.

Verification also needs to be made against "secondary" standards such

as radiosonde wind fields. Also, since the winds generated by cloud

motions are primarily intended for numerical models, the numerical models

should be used in the verification to see how these cloud winds improve

the forecasts. Before improvements can be added to the height and wind

systems, a good verification system is needed to judge the value of the

improvements.

B. Infrared Calibration

Since the absolute accuracy of the cloud height system depends on the

accurate calibration of the infrared sensors, and since there are errors in

the present calibration, further work is required on IR calibration.

C. Visible Calibration

The optical thickness measurement depends upon a calibration of the

visible sensors. Further work is required on comparing the calibration results

from thick cloud calibrations to other methods of calibration. Also the

calibration technique using thick clouds could use further analysis to

determine the effect of the horizontal dimension of the thick cloud on the

calibration.

D. Finite Cloud Multiple Scattering

The data base for the brightness to optical thickness calculation used in

this study was generated by a state of the art multiple scattering model which had no horizontal boundaries. Real clouds have horizontal boundaries. When multiple scattering theory has progressed far enough so that the finite cloud problem can be solved for thick clouds, these results should be included in the data base for conversion from brightness to optical thickness.

F. Fractional Cloud Cover

The computation of a thin cloud's true temperature requires a knowledge of the fractional cloud cover in the infrared scanning area. The fractional cloud cover routine used in this study is fairly crude and somewhat arbitrary. Further refinement of this routine is possible.

G. Land Brightness

The data base used to convert brightness to optical thickness contains information in it on the albedo of the sea surface, but not of land surfaces. The sea surface albedo is used over land. Another data set could be generated with a land albedo. Use of this data set would require the system to determine when a point is over a land mass.
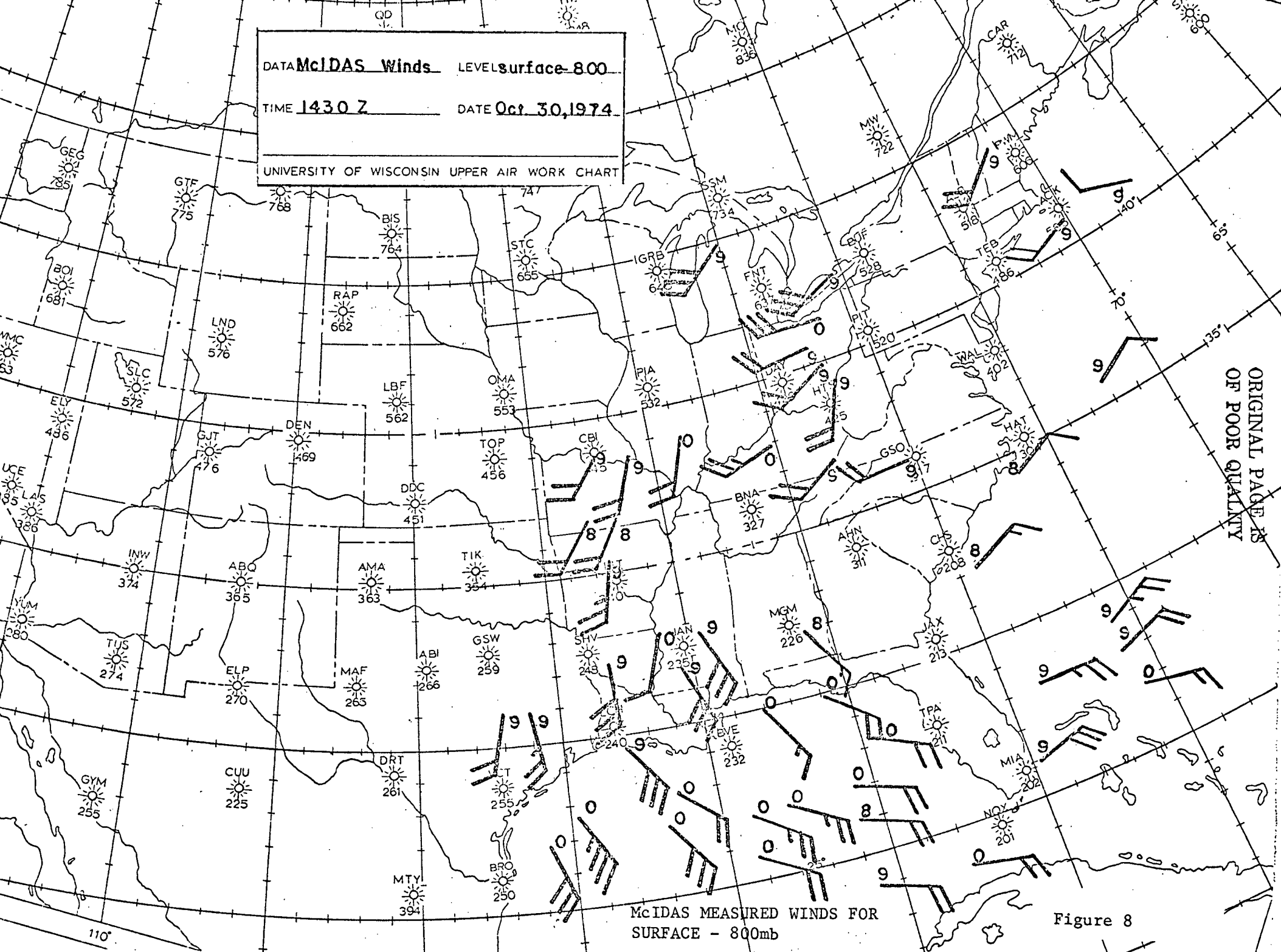
H. Real soundings

The cloud height system presently uses standard atmospheres corrected for latitude and date in the conversion of temperature to height. The addition of real soundings to the system would improve the height determination accuracy.

McIDAS MEASURED WINDS FOR SURFACE - 800mb

Figure 8

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RADIOSONDE MEASURED WINDS FOR
850mb

Figure 9

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McIDAS MEASURED WINDS
FOR 700-500mb

Figure 10

Figure 11

DATA **McIDAS Winds**   LEVEL **400-100mb**

TIME **1430 Z**   DATE **Oct. 30, 1974**

UNIVERSITY OF WISCONSIN UPPER AIR WORK CHART

McIDAS MEASURED WINDS
FOR 400-100mb

Figure 12

Radiosonde

DATA Winds   LEVEL 300 mb

TIME 1200 Z   DATE Oct. 30, 1974

UNIVERSITY OF WISCONSIN UPPER AIR WORK CHART

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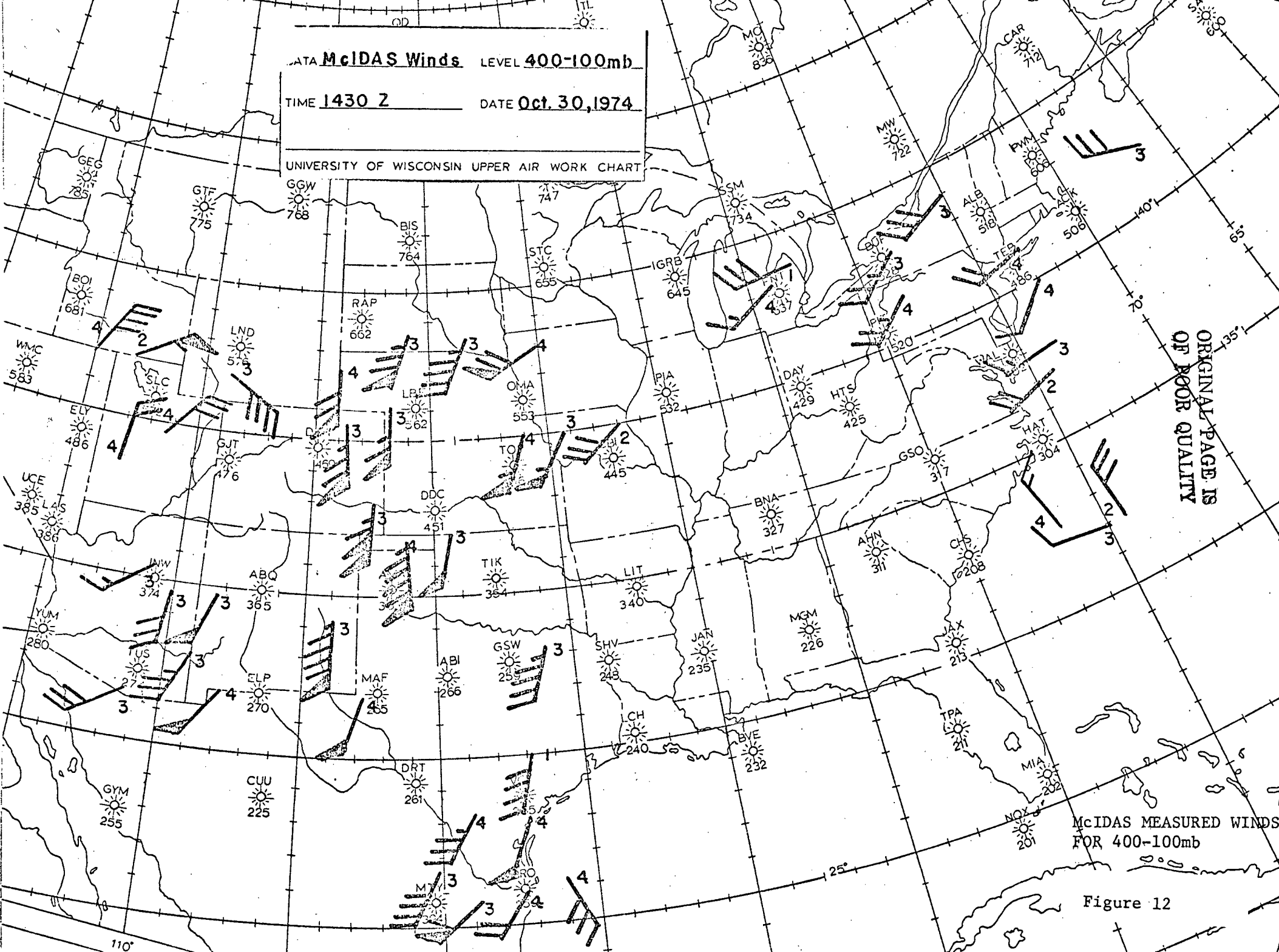
RADIOSONDE MEASURED
WINDS FOR 300mb

Figure 13

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McIDAS ARCHIVE SYSTEM

GENERAL THEORY OF OPERATION

The purpose of the McIDAS Archive System is to receive the digital image data from the SMS satellite, record and archive it to full resolution on a 24 hour a day basis, and to have this archived data on line to the McIDAS Computer in blocks of 32 complete images.

To this end, the Archive System consists of the following subsystems, (See FIGURE 3; McIDAS Archive System Functional Block Diagram):

1. The DUS/Antenna Subsystem which receives the retransmitted, duty cycle improved, parallel to serial converted SMS data; and demodulates it and presents it as a digital serial bit stream containing data, clock, timing, sensor identifier and data documentation.

2. The Archive Subsystem which accepts this bitstream; stabilizes it and extracts a bit clock; decodes the PN sequence and separates the nine sensor scans; performs an asynchronous phasing and time base translation to the 7 mega bit rate necessary for recording in the Slant Track Video Recorder format; adds a locally generated documentation word of 384 bits; extracts the necessary information to automatically start up the Slant Track Video Recorder at the beginning of each picture and stop it at the end; and modulates the data in the biphase format.

3. The Archive Slant Track Video Recorder accepts the biphase encoded bit stream from the Archive Subsystem and records it on one inch magnetic tape according to a typical helical scan format with one sensor scan recorded on each track. The Slant Track Video Recorder is not synchronized with the satellite spin rate and records 20 slants per

second. The satellite generates only 15 sensor scans per second
at 100 rpm, so that only about 75% of the slants contain data. Even
with this inefficiency, one 7500 foot reel of tape will record 32 full
resolution (IR and visible combined) SMS images. This represents
over 50×10^9 (billion) bits per reel of tape.

4. The Mass Storage Unit (MSU) subsystem consists of the Playback Slant
   Track Video Recorder to play back the tapes generated in the Archive
   Subsystem; a demodulator to convert the biphase format to the more
   useful NRZ(L) with clock format; and a computer interface which
   allows ingestion of the data in 24 bit word groups by the McIDAS
   Computer for display and analysis. In addition, the MSU Subsystem
   allows for remote control of the Slant Track Video Recorder by the
   computer so that appropriate data can be found quickly and automatically.

McIDAS ARCHIVE SYSTEM

DETAILED THEORY OF OPERATION

DUS ANTENNA SUBSYSTEM
     Refer to FIGURE 3; McIDAS Archive System Functional Block Diagram

     The DUS Antenna Subsystem consists of a 24 foot disk antenna mounted on the roof of the Meteorological & Space Science Building on the Madison Campus of the University of Wisconsin; a Feedhousing mounted at the focal point of the antenna and containing the 1.6871 GHz Paramp and Downconverter; a J-Box mounted to the antenna frame which contains the power distribution for the antenna two axis (hour angle and declination) remotely controlled mount; and the DUS Rack installed in the sixth floor McIDAS Operations Room and containing the PSK Demodulator electronics, the Receiver Test Unit and the antenna mount control unit.

     This entire subsystem was specified by NOAA and built by Radiation Incorporated, and is documented in the following volumes:

     Operation and Maintenance Manual for the DUS Receiving System

     Date Utilization Station (DUS) Test Procedure and Test Report
     (2 Volumes)

     Paramp/Downconverter Maintenance Manual

     DUS Electrical Diagrams

     DUS Complete Mechanical Drawings

ARCHIVE SUBSYSTEM

BIT SYNCS
      Refer to FIGURE 3; Archive System Functional Block Diagram

      The Bit Syncs receive the demodulated digital data from the PSK Demodulator
in the DUS Antenna Subsystem via an optoisolator; they stabilize the time base
of the digital bit stream by band pass filtering utilizing phase locked loop
techniques; and they extract a bit clock properly phased to the data.

      Two bit syncs are used because the bit stream contains data at two distinct,
duty cycle shared frequencies, (one associated with the visible sensor data and
one associated with the infrared (IR) sensor data). The bit syncs are identical
units with different plug-ins. Both are EMR/Schlumberger Model 2726-02 PCM
Signal Conditioners.

      The retransmission of the sensor scans are assigned to the time interval
during which the satellite is scanning space (not scanning the earth) on a
duty cycle basis, and therefore, the exact bit rate will be dependent on both
the resolution mode the satellite is operating in and its exact spin rate. The
resolution mode is a gross, step function bit rate change and requires a specific
plug-in for the visible bit sync for each mode. The modes are A, B, C & D, and
only the visible resolution is affected from mode to mode.   The IR
resolution and therefore bit rate, remains constant. Refer to Appendix A;
SMS VISSR Data Formats.

      The satellite spin rate is a smaller bit rate change and the bit syncs are
designed to track this drift over a $\pm$ 2.5 rpm (@ 100 rpm nominal) spin rate
change. This is a relatively large spin rate change and will be experienced
only when the satellite jets are fired during maneuvers. Small timing boards
are provided for the bit sync plug-ins to allow them to track the satellite
spin rate over its entire designed operating spin rate range of 50 rpm to

110 rpm.

The output of each bit sync is a digital bit stream and a bit clock phased to it. In reality, two bit clocks are available, one in phase with the data and one lagging the data by 90 degrees.

The bit syncs are written up in detail in the manuals provided by EMR/ Schlumberger (PCM Signal Conditioner Model 2726-02 and Selector Modules Model 2727).

DUS/ARCHIVE INTERFACE
    Refer to FIGURE 3; McIDAS Archive System Functional Block Diagram

The DUS/Archive Interface accepts the visible and IR serial bit streams
with associated bit clocks from the Bit Syncs; decodes the PN sequence to
determine the data interval for each sensor scan (8 visible and 1 IR); decodes
data documentation to be displayed on the front panel and to be distributed
to the Archive Control; and translates the data to the NRZ(L) format, which
is supplied (with a clock) to the Archive Control.

    The DUS/Archive Interface is, in reality, a subsection of the "Direct
Readout Ground System Digital Interface Electronics System (EMR POA B5885)"
as designed and built by EMR/Schlumberger for NOAA. Checking the manual for
the above named system, (FIGURE 1-1, page 1-2) indicates that the DUS/Archive
Interface is the EMR Frame Synchronizer without the simulator or the PSK
Modulator.

    The DUS/Archive Interface also contains a subsystem known as the "Data
Stripper and Display" which the EMR/Schlumberger unit does not contain. Its
purpose is to selectively decode data documentation words (either IR or
visible) and to display this data in the form of a bit pattern and a hexa-
decimal encoded readout. The operator selects the word number and whether
IR or visible by means of thumbwheel switches.

    More details on the operation of the DUS/Archive Interface Data Stripper
and Readout will be made available at a later date.

ARCHIVE CONTROL
    Refer to FIGURE 3; McIDAS Archive System Functional Block Diagram

GENERAL

The Archive Control accepts the SMS serial data, data clock, sector clock, sector end, and frame code from the DUS/Archive Interface and together with the three Data Buffers and the Documentation Generator, supplies the SMS data to the biphase modulator at the proper rate (7 megabits) and with the proper phase, to allow recording it on the Archive Slant Track Video Recorder.

The recording format on the Slant Track Video Recorder calls for one sector (sensor scan) to be recorded on one track of the tape. Refer to FIGURE 4; Slant Track Video Recorder Tape Format. The Slant Track Video Recorder operates asynchronous from the satellite spin rate and writes 20 slants per second. Therefore, it can accept satellite data at rates up to 20 sectors per second. The SMS satellite has a nominal spin rate of 100 rpm and produces nine sensor scans (8 visible and 1 IR) for each rotation when in mode A (half mile resolution). This means 900 sectors are generated per minute or 15 sectors are generated per second. On the average then, 20 tracks are available to record 15 sectors of information; which implies a slant utilization efficiency of 75%. The slants that do not contain data (missed slants) are recorded with proper multiple sync and sync pulses, but all data is forced to zero.

All sectors, however, do not contain the same number of bits. The eight visible sectors each contain 104,832 bits for mode A, 52,416 bits for mode B, and 15,968 bits for modes C & D. The IR contains 39,312 bits per sector for all modes. Refer to APPENDIX A; SMS VISSR Data Formats. When the tracks are written however, the bit rate is constant at 7 megabits and consequently, a sector with fewer bits does not fill the entire track.

The remainder of the track is filled with whatever happened to be left over in the higher level addresses of the Data Buffer used for that slant. This means the archive becomes less and less efficient as the satellite changes from mode A to mode B to mode C/D. Mode B (one mile resolution) for instance, implies half the number of visible sectors per satellite rotation and half the number of bits per visible sector. This means only 5 sectors (4 visible and 1 IR) per satellite rotation; which in turn implies only 8.3 sectors per second (at 100 rpm satellite spin rate) for a track utilization efficiency of only $\frac{8.3}{20}$ x 100 = 41.5%. The bit packing efficiency is even less because each visible slant recorded is only half full and the IR slant is only about 40% full.

LOADING SEQUENCE

The Frame Code word of the IR and visible data documentation (word 4 in both cases) goes to a one with the first satellite rotation of a new picture and goes to a zero after the end of the last satellite rotation of the picture. Refer to APPENDIX A; SMS VISSR Data Formats. The DUS/Archive Interface decodes the Frame Code word of the IR data documentation and provides it (as Frame Code) to the Archive Control. See Archive Control Schematic. This Frame Code signal is used to put the Archive Slant Track Video Recorder into the record mode via JK Flip Flop chip 27 and the Relay Interface and to initialize the entire Archive Control by generating a Master Clear via mono chip 9 and gate chip 8.

Once the picture transmission is started, the DUS/Archive Interface provides the data and data clock for each sector (sensor scan) to the Archive Control, as they are received. These sectors include the data, the data documentation and the PN sequences; but not the earth view interval.

In addition, the DUS/Archive Interface provides the Sector Clock signal, which is a zero going pulse of one bit period duration, synchronous with the data clock cycle previous to the first data bit of each sector. Actually, it is previous to the first bit of the data documentation. This format is the same for IR and visible and for modes A, B, C & D; the only difference is the actual frequencies involved.

The very first sector clock of a picture transmission is used to enable the ÷ 3 Sequencer within the Archive Control, which had been initialized to state 00 by the Master Clear pulse generated by the Frame Code word. Once enabled, the ÷ 3 Sequencer advances on the lagging edge of each successive sector clock pulse and thereby sequentially interrogates the three data buffers (via the Data/Data Clock Multiplexer), as SMS data is provided sector by sector, from the DUS/Archive Interface. Note that the buffer loading is an "advance then load" operation in that the ÷ 3 Sequencer is advanced to its new state just before the data for that state is presented.

Each Sector Clock enables the Data Clock to be presented to the Data/Data Clock Multiplexer by means of JK Flip Flop Chip 3 and gate Chip 6. The Data Clock remains enabled for the duration of the sector and is disabled via the Sector End signal from the DUS/Archive Interface.

UNLOADING SEQUENCE

The unloading sequence is synchronous with the Archive Slant Track Video Recorder. The "Slant Track Control" board within the Archive Slant Track Video Recorder generates a zero going pulse of approximately 1 μsec duration called the Start Slant pulse. The leading edge of this pulse occurs when the scanning record/reproduce head is at the proper point on the track to begin recording

data. This start slant pulse is sent to the biphase Modulator where it initializes the recording process. It is also sent to the Archive Control where it initializes the unloading process if conditions are "proper".

In order to understand what is meant by "proper conditions", it is necessary to realize that unloading the Data Buffers must be in the same sequence as they were loaded in and must be phased so that as each Data Buffer loading is completed, the very next Start Slant pulse will result in this Data Buffer being unloaded. The Sequence Coincidence Detector (See Archive Control Schematic) assumes that if the Unloading ÷ 3 Sequencer is attempting to unload a particular Data Buffer when a start slant pulse is generated, and if the Loading ÷ 3 Sequencer is presently loading the next Data Buffer in the sequence, then and only then, will the Start Slant pulse be allowed to initialize the unloading process.

There are three conditions which will result in a Start Slant pulse initializing the unloading process; if Data Buffer A is to be unloaded and Data Buffer B is being loaded; or if Data Buffer B is to be unloaded and Datter Buffer C is being loaded; or if Data Buffer C is to be unloaded and Data Buffer A is being loaded. If either of these three conditions are present when the leading edge of a Start Slant pulse arrives at the Archive Control, JK Flip Flop Chip 23 will be toggled. Because of the feedback from $\overline{Q}$ to the asynchronous reset of this Flip Flop, only a narrow pulse (approximately 500 nsec duration) will be generated. This zero going pulse is sent to the Documentation Generator as the Start Documentation pulse to start the encoding of the documentation word.

Meanwhile, the biphase Modulator has also received a Start Slant pulse from the Slant Track Control Board Recorder and immediately starts to encode data. Once initialized, the Modulator controls the entire recording process until the

end of the track. First of all, it records a Multiple Sync Word, which is eight sync words in a row. A Sync Word is one cycle of a square wave with a period of 420 nsec (3 x 140 nsec). See FIGURE 10; Archive Track Format. Then it encodes as the first bit, the level which exists on the Slant Track Data line, and at the same time sends an active edge (positive going) of Slant Track Data Clock to the Archive Control and to the Documentation Generator, asking for the next data bit. On the next cycle of the 140 nsec biphase clock, this data bit is encoded and the next bit is asked for. See FIGURE 9; Biphase Encoding Format. This continues for an entire record (192 bits). The Modulator then inserts a Sync Pulse before it continues to encode the next record. After all 548 records are encoded, the Modulator encodes the second Multiple Sync Word, sends a Slant Done pulse of approximately 1 μsec duration to the Archive Control, and terminates encoding until the next Start Slant.

It should be noted that although the Archive Control and Documentation Generator send data in response to the Modulators request for bits only under "proper conditions", the Modulator always records a track in response to a Start Slant. The Multiple Sync Words, Sync Words, and data encodings are generated and recorded properly. However, because the Archive Control and Documentation Generator do not respond, the data always appears to be zeros and therefore, skipped slants contain all zero data.

When the Documentation Generator receives the Start Documentation pulse from the Archive Control, it begins to send documentation data to the Modulator in response to its Slant Track Data Clock. The documentation data consists of one record (192 bits) of a zero-one fill pattern and one record (192 bits) of documentation data. Refer to FIGURE 5; Documentation Data Format.

The zero-one fill pattern is generated in the Archive Control by JK Flip Flop chip 24, under the control of the Documentation Generator. Immediately after receiving the Start Documentation pulse, the Documentation Generator sends the Fill Pattern Enable signal to the Archive Control which allows JK Flip Flop Chip 24 to respond to the Modulator's Slant Track Data Clock and thereby generates the zero-one fill pattern.

The Documentation Generator counts the Slant Track Data Clock pulses and sends the Fill Pattern Reset signal to the Archive Control to terminate the zero-one fill pattern when 192 bits have been recorded. The Documentation Generator then records the 192 bits of documentation data according to the Slant Track Data Clock, by sending an active Documentation Data Gate and the documentation data itself to the Archive Control. This same Documentation Data Gate is resent from the Archive Control to all three Data Buffers as a pre-unload signal which is used to disable the refresh clock.

After the 192 bits of documentation have been encoded, the Documentation Generator sends a Documentation Completed pulse (zero going) to the Archive Control. This pulse is processed in the Unload Multiplexer to provide an Unload signal to the appropriate Data Buffer. In addition, the Documentation Completed pulse is used to gate the Slant Track Data Clock to the same Data Buffer. The Data Buffer then sends SMS data to the Archive Control and ultimately to the Modulator. In this manner the sequence of recording the fill pattern, documentation, and SMS data (for one sector) is accomplished.

When the Modulator finishes recording all 548 records for that track, it records the final Multiple Sync Word and sends a Slant Done pulse (zero going) of approximately 1 μsec duration to the Archive Control. This pulse disables the Slant Track Data Clock from getting to the Data Buffers and advances the Unload ÷ 3 Sequencer.

Note that although the Unload ÷ 3 Sequencer is advanced immediately after a Data Buffer is unloaded, it still amounts to an advance-unload operation because it was "advanced" to zero during the master clear which was held active between pictures and released at the beginning of the picture in question. Thus both the Load ÷ 3 Sequencer and the Unload ÷ 3 Sequencer are advance - load/unload operations and therefore Data Buffer A will always be first loaded and first unloaded.

DATA BUFFERS
    See FIGURE 3; McIDAS Archive System Functional Block Diagram

GENERAL

The purpose of the Data Buffer is to provide temporary storage of the

data from one sector (sensor scan) of the SMS satellite. The sector data

is loaded into the Data Buffer in synchronism with the satellite via the

Archive Control. It is then held and finally unloaded in synchronism with

the Archive Slant Track Video Recorder under the control of the Modulator.

In this manner, the Data Buffer performs the time base translation and the

phasing function which ties together the asynchronous SMS data source and the

SMS archive tape.

The McIDAS Archive System must buffer three sectors deep as shown in

FIGURE 6; Data Buffer Load/Unload Sequence, and therefore requires three

Data Buffers.

Each Data Buffer has a storage capacity of 131,072 bits (128 x 1024) and

is used to store one sector (sensor scan) of data from the SMS satellite.

The exact number of bits contained in a sector depends on whether it is a

visible or IR sector and if visible, what resolution mode the satellite is

operating in. The largest capacity is required to store a visible sector

in mode A (half-mile resolution). In this case, a 104,832 bit capacity is

required.

Each Data Buffer consists of a Memory Board containing 128 dynamic

(MOS) RAM chips each organized as a 1024 x 1 bit memory; a Buffer Control

Board; and a board containing eight sense amplifiers. The memory chips

used are the Mostek MK 4008-9P. Refer to APPENDIX B: Miscellaneous

Data Sheets. Because it is a dynamic RAM, there is a minimum clock fre-

quency as well as a maximum clock frequency for proper operation of the

chip. The chip requires a minimum of 1 µsec for a write or refresh cycle (800 nsec for a read cycle) and can only store data for about 1 msec. The chip is not refreshed during a read cycle, but is refreshed during a write or refresh cycle. The Data Buffers are designed without a separate re-fresh cycle, and will work with IR and mode A or B visible data only.

The highest freqencies occur during unload when data must be provided to the Modulator at a 7 megabit rate. It is precisely because of the need to keep up with the demands of the Modulator that it is difficult to add a priority refresh cycle to the memory during the unload phase. Yet, be-cause the unloading takes about 14 msec to accomplish, the memory must be refreshed. The Data Buffer design solves the 7 megabit rate problem by storing the data as 16 bit words and solves the refresh problem by combining a refresh cycle with each read cycle.

The memory cycle when loading is Read-Write, and when unloading is Read-Refresh. During loading, the Read portion of the memory cycle does not accomplish anything useful.

MEMORY ORGANIZATION

The memory is wired as 8 sets of 16 chips each for a total storage capacity of 8192 (8 x 1024) 16 bit words. Data is moved in and out of the memory in 16 bit blocks. Each 16 bit chip set, has 1024 locations which are interrogated with two 5 bit words (Row Address & Column Address). The 8 sets are interrogated in sequency by utilizing the chip enable (CE). See MK 4008-9P Specifications in APPENDIX B; Miscellaneous Data Sheet and FIGURE 7; Data Buffer Functional Layout.

The Memory Address Generator (refer to the Data Buffer Schematic) pro-duces the Row Address, Column Address and Row Enable signals necessary to sequence the memory properly for loading and unloading. Because refreshing

a chip requires all 32 Row Address locations to be interrogated, the
Row Address sequences are at the highest rate. The Row Enable is next
and the Column Address sequences last.

The relative position of the Row Enable and the Column Address can be
reversed, but is this way because it produces a "fail soft" situation in
case a chip or chip location does not store data properly. Accordingly,
as Row Enable is advanced, it means an entire new set of 16 chips is
selected. This means that if a chip location is bad, less adjacent data
will go through that chip location before the next chip location is
selected. If the Column Address had been sequenced after the Row Address
instead of Row Enable, 32 times as much adjacent data would have been
lost. In an image, the difference is between 32 relatively small vertical
strips of bad data versus one wide strip of bad data. It should be pointed
out that this organization is complicated by the fact that a particular chip
handles only one bit of a 16 bit word which in turn, is made up of 6 bit
words for visible or 9 bit words for IR. This means that a bad chip affects
only one bit of a data word at a time and the binary weight of the affected
bit changes from one data word to the next. It has, of course, a well
defined repeatable pattern, but the point is that the 16 bit word organiza-
tion in itself contributes to a fail soft situation in the case of bad
chip locations. Experience has shown that bad chip locations result in
image damage which is aesthetically noticeable and which causes automatic
correlation programs difficulty, but enough data is present to generally
allow a viewer to determine what is happening in the area.

TIMING

Unloading the Data Buffer is done at the 140 nsec period (7 megabit) bit
rate of the biphase Modulator. This 140 nsec rate is constant no matter whether the

data is IR or visible or what resolution mode the satellite is in. This means the Data Buffer must provide a 16 bit word every 2.24 μsec (446K Hz rate). The minimum time for a read-write/refresh cycle is 1.45 μsec (t_{CE} = 450 nsec + t_W = 450 nsec + t_{AW} = 550 nsec). The actual design has t_{CE} = 600 nsec, t_W = 500 nsec and t_{AW} = 1.14 nsec. See FIGURE 8; Data Buffer Load/Unload Timing.

The important factor when loading the Data Buffer is the time the chips can hold the data before they must be refreshed. The MK 4008-9P are cheaper, selected versions of the MK 4006/4008 chip which has a refresh time of 2 msec. The MK 4008-9P is specified for only 1 msec refresh time. The other two specifications which are reduced is memory cycle time and "power down" characteristics. A refresh cycle for a chip actually requires 32 separate write or refresh cycles to be performed, i.e. the 32 states of the 5 bit Row Address must each be hit with a write or refresh cycle. The design of the Data Buffers is optimized in view of this restriction by using the Row Address as the highest speed addressing index and by organizing the memory so that all the chips in the memory receive the same Row Address (and Column Address) and are either written or refreshed for every 16 bit word loaded. This means that for every 32 16 bit words loaded into the Data Buffer, the entire memory (all 128 chips) is refreshed.

SMS IR data comes in at the rate of 524.16 K bits/sec for the nominal satellite spin rate of 100 rpm. This means a 16 bit word is received every 30.5 μsec. The 32 words required to refresh the memory will take 0.977 msec. Comparing this to the 1.0 msec refresh time specified for the chip, it is close.

Visible mode A data (half mile resolution) on the other hand, has a bit rate of 1.747 megabits/sec @ 100 rpm, which means that the memory is refreshed every 293 μsec. Visible mode B data (one mile resolution) has a bit rate of only 436.8 K bits. Note this is less than the IR bit rate of

524.16 K bits. Visible Mode B will refresh the memory every 1.17 msec.
This is some 17% over the specified refresh time for the MK 4008-9P chip,
but still well within the 2 msec refresh time of the MK 4006/4008 from
which the MK 4008-9P is selected. It is to be expected that the Data
Buffers should work in mode B, and in fact, experience indicates that
they do.

Modes C and D on the other hand, have a bit rate of only 33.28 K bits
@ 100 rpm, which results in a refresh time of 15.38 msec. The Data Buffers
can definitely not handle the mode C & D visible data. Note that the IR
bit rate is still the same and can be processed no matter what resolution
mode the satellite is in.

DETAILED OPERATION

The proper control signals for the memory chips are generated in the
Buffer Control. See Data Buffer Control Schematic. One of three clock
signals are always presented to the 16 Bit Word Formatter via gate Chip 4.
The Load Clock and the Unload Clock come from the Archive Control and are
gated in conjunction with the Load and Unload signals (as applied to gate
chip 1 of the Buffer Control) so that only one or the other (never both)
can be present at any one time. If the Data Buffer is not in either the
load or unload mode, i.e., in a standby (or data hold) mode, then the
Refresh Clock, as generated by mono chip 3, is applied to the 16 Bit Word
Formatter.

Chips 26, 27, 13 & 14 divide the input clock (chip 4 pin 12) by 16
in order to generate the Word Clock (chip 21 pin 4). Simultaneously, the
input clock is also advancing the 16 bit serial to parallel converter
(chips 28, 29, 15 & 16) and the 16 bit parallel to serial converter
(chips 32, 33, 19 & 20). The Word Clock resets the ÷ 16 shift register

and stores the contents of the 16 Bit Serial to Parallel Converter in a
16 bit latch (chips 30, 31, 17 & 18). See FIGURE 8; Data Buffer Timing.

Simultaneous with the generation of the Word Clock, chip 22 is
asynchronously set by the ÷ 16 Shift Register (chip 14 pin 11). This puts
the 16 Bit Parallel to Serial Converter into the parallel load mode. When
the active edge of the next clock pulse occurs, a new 16 bit word from the
Memory is loaded. This same clock edge clocks chip 22 to the reset state
and thereby returns the 16 Bit Parallel to Serial Converter to the serial
mode so that subsequent active clock edges will shift the data out to the
Archive Control and ultimately to the Modulator.

Note that even though one clock edge was used to do a parallel transfer
of date into the 16 Bit Parallel to Serial Converter, no data was lot be-
cause the parallel transfer operation places the next bit on the Data Out
line.

The lagging edge of the Load/Shift Control signal (chip 22 pin 6)
triggers mono chip 21 pin 5 which generates a 600 nsec pulse. At the time
of the leading edge of this pulse, the decision is made whether this is to
be a write cycle or a refresh cycle. If the Data Buffer is in the load mode,
then gate chip 1 pin 5 will be low and the 600 nsec pulse will not set JK
Flip Flop 22 pin 9 and chip 12 will be enabled. This will allow Row Enable
signals to be generated and data will be written into memory as required
by the Load Mode.

On the other hand, if the Data Buffer is not in the Load Mode (implies
either in the Unload or the Standby Mode) the 600 nsec pulse will get to
JK Flip Flop chip 22 pin 9 and its leading edge will cause the Row Enable
signals to be disabled thereby refreshing the chips.

The 600 nsec pulse width is necessary to allow the Row Enable signals to stabilize if they were changed on the leading edge. The lagging edge triggers mono chip 5 pin 12 which generates a 500 nsec pulse which is routed to all the chips in the memory as the Read/Write (R/W) pulse. At the time of the lagging edge of this pulse, each chip is either written or refreshed depending on the state of its Chip Enable. If the Chip Enable is low, the chip will be written and if it is high, it will be refreshed.

At the completion of the R/W pulse (mono chip 5 pin 12), the Memory Address Generator is advanced to the next address location and the cycle is repeated.

The timing described above results in a Read-Write/Refresh sequence which occurs for each Word Clock (16 data clock cycles) whether the Data Buffer is in the Load, Unload or Standby Mode. The Unload and Standby Modes are the same except for the origin of the data clock. In the Unload Mode, the data clock comes from the Archive Control as the Unload Clock, and for the Standby Mode, the data clock is the Refresh Clock generated in the Buffer Control section of the Data Buffer. The unique feature about the Load Mode is that JK Flip Flop chip 22 pin 9 is held reset for the duration of the Load Mode and therefore, the memory chips are always enabled. This produces the write cycle instead of the refresh cycle in the basic Read-Write/Refresh memory cycle.

DOCUMENTATION GENERATOR
Refer to the Documentation Generator Schematic

The purpose of the Documentation Generator is to generate, store, and insert 384 bits of "documentation data" into the first two records (192 bits per record) of each track recorded by the Archive Slant Track Video Recorder. These two records are in addition to the SMS sector data which is recorded and which contains its own documentation (referred to as "data documentation".)

The first record written contains only a zero-one fill pattern, i.e., a recurrent 0-1-0-1-0-1 bit pattern for 192 bits. The purpose of this record is to provide an "average" type signal to the RF Equalizer of the Playback Slant Track Video Recorder during playback to allow the turn-on transcient to settle down under optimum conditions.

The second record contains the Frame Number, Slant Number, Manual Set information, Time, and Sector Identifier. See FIGURE 5; Documentation Data Format.

The Sector Identifier originates in the DUS/Archive Interface by decoding the PN sequences to find the IR sector, and counting the visible PN sequences to generate the visible sector identifier. Note, for mode B the sector identifier counts, 0000, 0001, 0010, 0011, 0100. No allowance is made for the fact that in mode B the sensors are paired (1 & 2, 3 & 4, 5 & 6, 7 & 8) to produce the four visible sensor scans.

Also, the Sector Identifier is generated, sent to the Documentation Generator, and recorded on the Slant Track Video Recorder in real time, whereas the SMS data being recorded on the same track has gone through a Data Buffer. This means that the Sector Identifier recorded on a particular track does not correspond to the SMS data on that track. Instead, it corresponds to the SMS data which will be recorded on the next track.

The zero-one fill pattern is not generated in the Documentation Generator. It is generated by JK Flip Flop chip 24 pin 7 in the Archive Control. Its generation is, however, controlled by the Documentation Generator. When the leading edge of the Start Documentation pulse is received from the Archive Control, the Fill Pattern Enable signal is brought high and sent to the Archive Control to enable JK Flip Flop chip 24 pin 7 to generate the zero-one fill pattern synchronously with the Slant Track Data Clock from the Modulator. In addition, the Slant Track Data Clock is applied to the 96 bit shift register in the Documentation Generator. Because the Shift/Load signal is low at this time, this results in loading the documentation data into the 96 bit shift register for each of the 192 Slant Track Data Clock cycles involved in recording the fill pattern. As the fill pattern is being recorded, chips 49, 54 & 59 of the Documentation Generator count 192 Slant Track Data Clock cycles (one record) and then terminate the fill pattern by sending the Fill Pattern Reset Signal to the Archive Control.

At the same time, the Documentation Data Gate signal is sent to the Archive Control to enable the documentation data to be recorded as the next (second) 192 bit record, and the 192 bit shift register containing the documentation data is put in the shift mode by bringing the Shift/Load signal (gate chip 56) high. The next 192 Slant Track Data Clock cycles result in the documentation data being shifted out of chip 45 pin 12, sent to the Archive Control, and ultimately recorded as the second record on the track.

After a total of 384 Slant Track Data Clock cycles are counted, JK Flip Flop 63 is set, resulting in the Documentation Data Gate and the Fill Pattern Enable signals being reset. Mono chip 65 pin 5 is also triggered

and the resultant 100 nsec pulse is sent to the Archive Control where the lagging edge is used to gate on the Slant Track Data Clock; and to enable the ÷ 3 Unload Sequencer, in preparation for recording the SMS data from the Data Buffer. The 100 nsec delay is to make sure that the Slant Track Data Clock is gated during the interval of the inter-record sync pulse. This eliminates any possibility of a glitch due to different delays involved in getting the Slant Track Data Clock from the Modulator to the Documentation Generator, and from the Modulator to the Archive Control.

MODULATOR

Refer to FIGURE 3; McIDAS Archive System Functional Block Diagram and the Modulator Schematic.

Details on the operationof the modulator is not now available and will be provided at a later date.

RECORDING SUBSYSTEM

SLANT TRACK VIDEO RECORDER

　　Refer to FIGURE 3; McIDAS Archive System Functional Block Diagram

GENERAL

The Slant Track Video Records work in conjunction with the Archive

Control and the Modulator to record SMS data and in conjunction the Demodula-

tor & MSU Control to playback SMS data. The Slant Track Video Recorder consists

of a scanner assembly containing the video record/reproduce head which

rotates at 3600 rpm (60 rps); a tape transport which moves tape past the

scanning head at 2.30 inches per second; a transport Remote Control Assembly

which allows the Slant Track Video Recorder to be automatically started and

stopped as data is received from the satellite; and a Slant Track Control

Board which maintains the proper relationship between the scanning head and

the tape in order to initiate recording of each track (by generating the

Start Slant signal), to document where on the tape this track is located

(by generating the Audio I tone burst) and to initiate the playing back of

each track (by generating the Playback Gate Signal).

The details of operation of the Scanner Assembly, the Tape Transport,

and the Remote Control Assembly, is covered in the Service Manual of the

IVC-900 Video Tape Recorder. The Slant Track Control Board is not a normal

part of the IVC-900 Video Tape Recorder, and represents what had to be added

to the IVC-900 Videotape Recorder to make it a Slant Track Video Recorder.

In normal operation, the tape moves a linear distance of 115 mils for

each scan of the rotating record/reproduce head. This provides a 6 mil wide

video track with a 3.5 mil guard band on either side of it, written at an

angle of 4.75 degrees from the direction of tape motion. This format records

60 tracks a second, with each track capable of recording 16 msec of data

with frequency components up to about 10 MHz. See FIGURE 4; Slant Track

Video Recorder Tape Format.

The SMS data to be recorded is received from the Modulator as 14 msec bursts, biphase encoded at a 7 megabit rate (140 nsec period). Each burst contains one sector (sensor scan) of SMS data and nine bursts are generated for each satellite rotation for resolution mode A (half mile resolution). Since the satellite nominal spin period is 600 msec (100 rpm), there will be 15 data bursts to be recorded per second. The maximum designed spin rate of the satellite is 110 rpm and therefore, the maximum burst rate would be 16.5 bursts per second.

Since each data burst can be recorded on one track, the normal 60 tracks per second write rate of the Slant Track Video Recorder is wasteful of tape. To correct this, the tape speed has been modified to 20 slants per second by reducing the diameter of the motor drive pulley by a factor of three and recording on every third scanner rotation. This results in the same 6 mil video track with 3.5 mil guard bands, but the angle the track is written at is slightly larger due to the reduced linear tape speed.

SLANT TRACK CONTROL BOARD

The Slant Track Control Board provides the timing necessary to record and play back data in the above described format. See Slant Track Control Board Schematic. The basic input is the Scanner Tach Pulse which originates as a photo electric pickup from a strip of reflective tape mounted to the Scanner Assembly of the Slant Track Video Recorder. This Tach Pulse signal contains both positional frequency and phase information about the scanning record/reproduce head, and is picked off at pin 2 of the Scanner Servo No. 2 Board and routed to pin 30 of the Slant Track Control Board.

The Tach Pulse is detected by comparator CM339-A3 which in turn clocks mono 4013-A1. The lagging edge of this Record Delay Mono Pulse is adjusted to occur just after the crossover (point where the head momentarily leaves the tape and returns to begin another slant track), so that data is positioned properly on the track. This lagging edge also clocks an 8 bit shift register (4015-A1 & A2) which feeds a selection matrix made up of gates 4011-A, -B, -C and 4012-A. This selection matrix determines how many scans are made between recordings and is presently wired to divide by three.

The lagging edge of the Record Delay Mono also clocks Flip Flop 4013-A2 which enables an astable (4013-C2) to produce a 1KHz tone burst. This Pre-Slant Signal is fed to the Audio I Board via a 0033C coax driver, and is recorded on the tape. The Pre-Slant Signal is recovered on playback to indicate which scan of the record/reproduce head is actually traversing the center of the recorded track.

The lagging edge of the Record Delay Mono also clocks Flip Flop 4013-B1 which delays one scan and then triggers mono 4013-C1 to produce the Start Slant pulse. This pulse goes to the Modulator and the Documentation Generator to actually start the recording process. In this manner, the Pre-Slant Signal is recorded one scan early to allow the proper gating to be accomplished before the beginning of the scan of interest.

Switch S1 was originally included to allow setting up the Record Delay

Mono but is no longer used because a better setup procedure is now used.

The switch should be left in the +12v Record position at all times.

In playback, the Pre-Start Signal from the Audio I Board is detected

by comparator CM339-A1 and fed to a peak detector and integrator consisting

of D6, R41 & C16. Comparator CM339-A2 detects the integrated signal and

provides an enable to Flip Flop 4013-D2. Meanwhile, Playback Delay Mono

4013-D1 has been detecting the Tach Signal and providing a clock to Flip Flop

4013-D2 at the exact center of the record/reproduce crossover. Consequently,

Flip Flop 4013-D2 toggles just before the recorded data will be played back.

This signal is sent to the Demodulator as the Playback Gate.

MSU SUBSYSTEM

DEMODULATOR

Refer to Demodulator Schematic

The Demodulator receives the archived data from the Playback Slant Track Video Recorder; translates the biphase data information to the more useful NRZ (L) with clock format; and extracts the Multiple Sync Words, Sync Words, and XSN Gate, needed by the MSU Interface to properly present the recorded SMS data to the McIDAS Computer.

The Demodulator uses the Playback Gate from the Slant Track Control Board within the Playback Slant Track Video Recorder to determine when to start looking for the RF. In reality, the RF for a particular track is present for all three scans of the Record/Reproduce head, but only one scan is directly down the center of the recorded track. The other two overlap the guardband and the previous track on one side and the guardband and the next track on the other side, and consequently, have reduced signal to noise ratio. By using the Playback Gate, the Demodulator is assured of working with the best signal.

After determining which scan to work with, the Demodulator uses the Unlimited RF from the RF Equalizer of the Playback Slant Track Video Recorder, to determine when the crossover gap is completed and the actual RF is being received. The Unlimited RF is detected by comparator chip 2 pin 11, and a short pulse is generated on each transition of the resultant square wave by monos implemented with gate chips 3 & 5. These pulses are sent to the retriggerable mono chip 18 which generates the Slant Duration signal which stays high until a gap in the pulses of greater than 28 μsec is detected. The leading edge of this Slant Duration signal toggles D Flip Flop chip 15 pin 5 (if the playback Gate is active) to produce the XSN Gate signal. This XSN Gate enables the Demodulator to start decoding the SMS data.

The RF from the Playback Slant Track Video Recorder is in the biphase

format (See FIGURE 9; Biphase Encoding Format) and as such, information is contained in the absolute timing between successive zero crossings. This makes it necessary to detect the zero crossings very accurately. The phase and frequency compensation and the first three levels of limiting is performed in the RF Equalizer Board of the Playback Slant Track Video Recorder. This limited RF is then sent to the MSU Bay where three more levels of limiting are performed (in the RF limiter) before it reaches the Demodulator as the Limited RF.

The zero crossings of the Limited RF are detected by comparator chip 8 to produce a square wave. If the XSN gate signal is active, (indicating that the Limited RF being received should be decoded) this square wave is presented to two monos (chips 11, 10 & 12) which produce 20 nsec pulses at each zero crossing. These XSN pulses (chip 12 pin 3) are fed to retrigerable mono chip 22 which decodes the Sync Pulses. These Sync Pulses indicate the intervals between 192 bit records and are used in the Sectorizer to do a preselection of the data which is sent to the Computer. Within the Demodulator, the Sync Pulses are sent to mono chip 21, shift register chip 20, and Flip Flop chip 15 where the Multiple Sync Word is detected. A Multiple Sync Word is written only at the very beginning and the very end of the recorded track and is used via gate chip 5 pin 9 to terminate the XSN Gate at the end of the recorded data on the track.

The XSN Pulses are also applied to the data decoding mono (chips 14, 13, & 12), which together with JK Flip Flop's (Chips 14 pin 7 and 19 pin 9) produce the data in the NRZ(L) format. The Data Clock is generated by mono chip 25 pin 5 utilizing the Sync Pulse and the leading edge of the XSN Pulses. Both the Data and the Data Clock are sent to the Computer Word Generator via the Digital Mux.

C-2

MSU CONTROL
Refer to the MSU Interface Schematic

MSU INTERFACE

The MSU Interface coordinates the efforts of the Computer Word Generator, the Sectorizer, and the Digital Mux, so that the handshaking conventions of the Computer (through its remotest periferal, the Unit Interface), are obeyed, and that the Real Time and Archive SMS data is properly ingested into the McIDAS System. The proper place to begin to understand the details of the MSU Interface operation is with the Computer Word Generator.

COMPUTER WORD GENERATOR

The purpose of the Computer Word Generator is to convert the serial data from either the Demodulator or the Real Time Ingestion System to the 24 bit word format required by the McIDAS Computer.

The Data arrives in the NRZ(L) format with the Data Clock. The Data Clock simultaneously shifts the Data into the 24 bit Data Shift Register and a "one" into the ÷ 24 shift register. After 24 shifts, the "one" reaches the final stage of the ÷24 Shift Register and is used to reset the ÷24 Shift Register and to load the 24 bits of Data contained in the Data Shift Register into the Data Transfer Buffer. These 24 bits of Data are then presented to the Unit Interface and put on the input bus to the computer. The reset pulse is also applied as a clock to JK Flip Flop C14 pin 13, which generates a Data Available signal to the computer (via the Unit Interface Board) if the Gated On-Line signal is active. (C14 pin 11).

The Gated On-Line signal originates in the MSU Interface as the On-Line signal. This On-Line signal is the Playback On-Line control signal from the computer, synchronized to the beginning of the next playback track. It

it ANDED with the output "mask" of the Sectorizor to produce the Gated

On-Line signal. The Playback On-Line control signal from the Computer arrives

vis the Unit Interface at latch chip C17 pin 12 and is applied to JK Flip Flop

chip C16 and pin 3. This Flip Flop then generates the On-Line signal at the

beginning of the next full track utilizing the XSN Gate signal and the Slant

End Interrupt signal.

Latch chips C17, C18, C19 and C20, comprise a small memory for control

bits as sent by the Computer (via the Unit Interface), to control the

operations of the MSU Subsystem and the Playback Slant Track Video Recorder.

C17 pin 12 is the Playback On-Line control bit which is discussed above. C18

pin 13, C18 pin 12 and C19 pin 15 are the three bits for control of the

Playback Slant Track Video Recorder transport (Fast Forward, Fast Reverse

and Play). C19 pin 13 is the Direct Mode/Archive Control bit which operates

the Digital Mux within the MSU Interface to select either real time SMS

data or archive SMS data to be inputted to the Computer Word Generator and

ultimately to the Computer. C18 pin 14 is the Mask Loading Enable Control

bit which is routed to the Sectorizer where it enables the Computer to load the

appropriate "mask" into the Sectorizer for preselecting the data ingested

by the computer.

SECTORIZER

The purpose of the Sectorizer is to allow the Computer to cull the data

it ingests from each track of the Playback Slant Track Video Recorder, before

it gets to the computer. This is important because of the large volume of

data contained on each track and because of the large amount of core and CPU

cycles involved in handling all this Data.

The Sectorizer accepts a 32 bit word (mask) from the Computer via the

Unit Interface and stores it in a 32 bit shift register. Each bit position

corresponds to a block of 16 records of 192 bits each, as recorded on Archive tape. If a "one" is loaded in a particular mask location, the Computer will receive this 16 record block of data. If a "zero" is loaded, it will not.

The 32 bit mask is stored in shift register chips F1 through F8. Sync Pulses arrive from the Demodulator as a double pulse for each 192 bit record. JK Flip Flop F9 pin 1 and mono D2, convert them to a single pulse per record and route them to two sets of counters, providing the Delayed XSN Gate from the Demodulator (F9 pin 9) is active. The ÷ 36 Counter allows the first 36 records to always be sent to the computer, and then enables the ÷ 16 counter which generates the basic Mask Clock. The Mask Clock shifts the mask shift register and applies the mask, one bit at a time, to gate E13 pin 4, where it is ANDed with the On-Line signal from the MSU Interface to produce the Gated On-Line signal. This Gated On-Line Signal controls generation of the Data Available Signal in the MSU Interface.

The remaining circuitry in the Sectorizer (chips E14, E16, E15, etc.) is involved in loading the mask. Both the Command Word and the Data Word from the Computer are involved. For more details, see the UNIT INTERFACE section below.

UNIT INTERFACE

The Unit Interface is a Universal 24 bit Unit Interface board purchased from Datacraft (Harris) and represents the remotest control point of the Computer. It is at this point that the Archive SMS data and the Real Time SMS data is ingested into the McIDAS system. The Unit Interface instruction set is available in the Datacraft (Harris) publication No. RM 61396-00P, entitled Reference Manual DC 6024/5 Computer Input/Output Interface, Publication No. RM 61397-00 entitled Reference Manual DC 6024/5 Computer System may also be useful.

The set of five schematics for the Unit Interface have been provided by Datacraft (Harris) and are labeled Universal 24 bit Unit Interface. No further information is available.

REAL TIME SMS INTERFACE

      Refer to FIGURE 3; McIDAS Archive System Functional Block Diagram and the Real Time SMS Interface Schematic

      Details of the operation of the Real Time SMS Interface is not available at this time and will be supplied later.

GENERAL THEORY OF OPERATION
   Refer to FIGURE 1; McIDAS System Functional Block Diagram and
   FIGURE 11; McIDAS Video Chain Functional Block Diagram

The McIDAS Video Chain receives both Control Data and digital Image

Data from the McIDAS Computer Subsystem. Under the direction given by the

Control Data, it processes the digital Image Data to the standard analog

T.V. Video format. Up to 500 of these images are stored in the Video Disk

Subsystem and presented, either individually or in sequence, to the Enhance-

ment Subsystem where their grayscale information is subjected to various

black/white and color transformations before it is presented for Display

and Distribution in the RGB Standard T.V. format.

The purpose of the enhancement is to increase the perceptual awareness

of the McIDAS Operator, to the "information" contained within the image data,

and is performed on each image element (pixel) under the indirect control of

the computer. This transformation can be changed and/or modified on an

interactive basis.

The Cursor Generator allows the computer to position a cursor over the

image data at a precise position relative to the original digital data

within the computer, from which the image was generated. The McIDAS Operator

tells the computer where to position the cursor by means of a two dimensional

joystick which is interfaced directly into the Computer. The Cursor allows

the Operator to accurately indicate areas of interest within the image. In

this manner the McIDAS System uses the Operator to "choose" areas of interest

and processing functions, and it uses the computer to "measure" the pertinent

image parameters.

The Level Discriminator provides the Enhancement Subsystem with the

capability to change enhancement and even image source as a function of the

instantaneous image grayscale value. The Level Discriminator compares each image element to the criterion established by the Computer and performs the proper response in real time as the image is being displayed.

McIDAS VIDEO CHAIN

DETAILED THEORY OF OPERATION

UNIT INTERFACE

The McIDAS Video Chain Unit Interface consists of a Universal 24 bit Unit Interface board purchased from Datacraft (Harris); a set of line drivers to distribute the computer generated subsystem Control Bits to the Digital Interfaces; and a Data Injestion System consisting mostly of a Datel DAS-16M Data Acquisition system which interrogates an digitizes (to 10 bits) any one of up to 16 analog inputs. The entire McIDAS Video Chain Unit Interface is built up on the Universal 24 bit Unit Interface wire wrap board.

The schematics for that portion of the McIDAS Video Chain Unit Interface built by Datacraft (Harris) and which performs the interfacing and handshaking with the Computer channel, are a set of five drawings labled Universal 24 bit Unit Interface. These schematics have been supplied by Datacraft and a description of the basic timing of the Universal 24 bit Unit Interface can be found in the Datacraft (Harris) publication No. RM 61396-001P) entitled Reference Manual, DC 6024/5 Computer Input/Output Interface; especially Section VI, ABC/SE/24.

The 24 data bits arrive from the computer via the Universal 24 bit Unit Interface as signals DFC00 + through DFC 23+, and are routed to line driver chips 109 2E througb 13 E. These line drivers send the data bits to both Digital Interface No. One and No. Two by a daisy chain arrangement. Twenty of these bits (DFC 04 + through DFC 23+) are also presented to a twenty bit latch implemented with chips 8202 1G & 2G, which stores this data when an active CDH + (Command Data Here) signal is received from the computer.

It should be explained that when the computer sends a word to a Unit Interface, it really sends two 24 bit words on the same bus in sequence. The first word is called the Command Word and is accompanied by a CDH + pulse (Command Data Here). The second word is the Data Word and is accompanied by the ODH + pulse

(output Data Here). The Command Word contains control information for the peripheral and the Data Word contains data information for the peripheral.

In this manner, twenty bits of the Command Word is stored in the Command Latch. Eight of these bits are sent out to the Digital Interface as the four bit Word Address and the four bit Package Select control bits. The ODH + (Output Data Here) pulse is sent to the Digital Interfaces via line driver chip 109 1E pin 1, as the Computer Load Clock. Both the CDH + and the ODH + pulses are echoed back to the computer via gate chip MC300 1D pin 8, to serve as the DATC + (Data Accepted) pulse which completes the transfer cycle.

The computer initiates a data input sequence (utilizing the Datel Data Acquisition System), by sending a 1 bit Convert Command and a 4 bit Analog Mux Address word in bits DFC-19, 20, 21, 22 & 23 of a Command Word. The Analog Mux Address Word is applied to the DAS-16M and causes it to select one of the 16 possible analog inputs. Specifications for the DAS-16M are included in APPENDIX B; Misc. Data Sheets. The Convert Command enables mono chip 8T22 6D. Meanwhile, mono chip 8T22 5D has been triggered by the same CDH + signal that loaded the Convert Command and has generated a 200 nsec pulse.

The 200 nsec is necessary to allow the Convert Command to propogate through the Command Latch, and the lagging edge of the pulse is used to trigger mono chip 8T22 6D, whenever it is enabled with an active Convert Command. The resultant 5 µsec delay pulse allows the Analog Mux to do its selection and settle down before the DAS-16M receives its Convert Command. At the lagging edge of this 5 µsec pulse, the DAS-16M brings the Busy signal high and commences to make the analog to digital conversion.

After about 16.6 µsec, the conversion is completed and the 10 digital bits are present on the input data lines (DTC 00 + through DTC -9+) to the

computer. The Busy signal is dropped to cause D Flip Flop 3060 2D to toggle, thereby presenting the IDAV + (Input Data Available) signal to the Computer. The Computer responds to the IDAV + by reading the Digitized Data and echoing DATC + (Input Data Accepted) which resets D Flip Flop 3060 2D, thereby removing IDAV +.

Mono chip 8T22 10D and gate chips 7D, 8D & 9D comprise a multiple input priority port to the computer and is no longer used. The Frame Sync interrupt now comes from the Data Ingestion System.

A Master Clear signal is generated by the computer in conjunction with the main frame Master Clear and is sent via the power inverter built up on carrier 2C, to the Digital Interfaces to reset all Subsystem Control Bits.

DIGITAL INTERFACE
Refer to Digital Interface Schematics

GENERAL

The purpose of the Digital Interface is to accept words from the Computer Subsystem via the Unit Interface; hold them until they are updated; and distribute them, bit by bit, to the McIDAS Video Chain. Two Unit Interfaces are included in the McIDAS Video Chain and each one stores up to eight 24 bit computer words. Each bit of each of the sixteen, 24 bit words is routed to a specific component of the McIDAS Video Chain as a control or data bit. Specific bit allocations are given in APPENDIX C; Digital Interface Bit Designations.

The McIDAS Video Chain has a Digital Interface No. 1 and a Digital Interface No. 2. The two units are identical except for the Package Designation Wiring (see below). The Digital Interface Control Schematic shows the basic structure of the Digital Interface and how computer words are loaded into it. The Digital Interface latch Detail schematic shows how computer words are stored and distributed.

CONTROL
See Digital Interface Control Schematic

The Digital Interface consists of eight Computer Word latches each capable of storing and distributing one 24 bit computer word, and the appropriate control to load data into these latches from one of three sources. The normal source of data is the McIDAS Computer via the Unit Interface, but data can also be derived from a set of front panel switches or from an external source. The External Source was originally intended to be used in conjunction with an off-line "Exerciser" package which would be used as a maintenance and checkout test fot the entire Video Chain. However, maintenance of the Video Chain has not been a serious problem to date and the McIDAS Computer has demonstrated the ability to provide all tests

needed, and consequently the "Exerciser" was never built. The front panel, manual entry feature, allows for manual control and exercise of the Digital Interfaces or of any subsystem within the McIDAS System. It is particularly useful to determine whether a system problem is a hardware or a software problem.

The front panel is shown on the Digital Interface Control Schematic and contains a Mode Switch to select the source of the data words; 24 two position toggle switches used for entering the appropriate control data; 3 two position toggle switches labeled Word Address, used to select which of the eight word locations the control data will be loaded into; a Load button which when activated and released loads the control data into the selected word location; and a Reset button which sets all bits of all eight control words to zero (inactive state) when depressed. A red warning light is also included which is on whenever the mode switch is not in the Computer Mode. The front panel wiring is shown on the Digital Interface Control Schematic immediately under the drawing of the front panel.

The mode switch determines the code sent to the digital multiplexer (chips G & H) which in turn selects the Word Address (3 bits) and the Package Select information (4 bits) from the appropriate source (either computer, manual or external). This information is routed to chip 825A where the 3 bit binary Word Address is decoded as one of eight outputs if the appropriate Package Select bit is active.

The mode switch also selects the Load Clock from one of three sources. The computer Load Clock comes from the Unit Interface as the Output Data Available (ODH+) signal and is received by Chip M and formed by Chip 8T22A. The manual Load Clock comes from the panel via non-bounce Flip Flop chip MC3060 pin 9. The Load Clock from the External Source is not wired at this time.

The Load Clock from the Mode Switch is ANDed with the "one of eight" outputs of chip 8250A and thereby routed to the appropriate Computer Word Latch where it results in the 24 bits of data loaded as the appropriate control word.

LATCH DETAIL
    See the Digital Interface Latch Detail Schematic

Digital multiplexer chips 8263A, B, C, D, E, & F select the appropriate 24 bit control word from one of the three sources (computer, manual, or external) in response to the Mode Select signal (S_1 & S_0) from the Mode Switch on the front panel of the Digital Interface package. The selected 24 bit control word is then routed to all eight Control Word latches. However, only one Control Word latch will receive a Load Clock from the Digital Interface Control and will accordingly store the Control Word and present it to the 24 line drivers (chips 109 A thru L) to be distributed as control or data bits to the McIDAS Video Chain.

Some control bits are required to put out a pulse whenever the computer sends out an active state (high) and not a level. These signals are generated with mono chips 8T22A, B, C & D. Mono 8T22A is triggered by the Load Clock signal and generates a delay pulse of 500 nsec, the lagging edge of which toggles the three Control Bit Pulse Monos. The delay is so that the data loaded into the Control Word Latches has adequate time to stabilize. If the control bit which is to produce the pulse is high after the delay, then that mono will be triggered and the pulse will be generated. If it is low, then no pulse will be generated.

When the board is layed out, the three Control Bit Pulse Monos are not designated to any particular bit location. If a bit location is to produce a pulse, then a mono must be designated to that bit location and wired in. The wiring is accomplished as follows:

1. Cut the run just before the line driver (109) between the two pads.

2. Install a jumper from the signal pad (before the cut) to the pad on the input line for the appropriate mono (pins 3 & 4).

3. Connect a jumper from the driver pad (after the cut) to either the pad on the run from the Q output (pin 8) or to the pad on the run from the $\overline{Q}$ output (pin 6) of the same mono.

4. The mono pulse width is set to 1 μsec, but can be adjusted if necessary by varying the external R & C.

Up to three pulse signals can be wired for each 24 bit control word.

TIMING GENERATOR

Refer to Timing Generator Schematic

The Timing Generator supplies all the system timing to the McIDAS Video Chain. It generates the Pixel Clock to be recorded on the DR-10A Video Disk as the Timing Track Signal, and it receives the playback of the Timing Track Signal and processes it to produce the Pixel Clock, Latch Signal and Convert Command signals. It also accepts the Horizontal Drive and Frame Sync from the Tektronix 146 Sync Generator which serves as the McIDAS System station sync, and processes them to produce the Line Clock, Frame Clock and Frame Interrupt Signals.

In order to understand the operation of the Timing Generator, it is necessary to understand the format of the McIDAS image. First of all, the image is in the 525 line format with a 4x3 aspect ratio. Because the image data originally exists within the McIDAS Computer Subsystem as a matrix of data samples , the TV raster must be considered as 525 lines with (4/3 x 525= 700) samples (or pixels) per line. Each data sample occupies a particular location within the TV raster designated by a line number and pixel number.

Standard TV format has timing only for the frame rate, field rate and line rate, and refers to bandwidth instead of pixel rate. The Timing Generator adds this last level of timing by generating a Pixel Clock with exactly 700 cycles during each horizontal sync interval. A crystal oscillator (chip 74S04 A) running at 4 times the required pixel clock frequency and subsequently divided by four, provides the time base stability to preclude the necessity to phase lock the pixel clock generator to the very stable station sync. (Tektronix 146). To eliminate accumulative error between the crystal oscillator and station sync, the ÷ 4 counter (JK Flip Flop chip

74S112 A) is reset during the horizontal interval and released for exactly 700 cycles of the pixel clock for each TV line (via D flip flop chip 3060 B pin 8 and gate chip MC3000 pine 3). The 700 cycle counter is implemented with chips N8285 A & B and N8273 A . In this manner, a very stable pixel clock is generated phase locked to station sync ($\pm$ 1/8 cycle of pixel clock) and providing exactly 700 cycles per TV line. See FIGURE 13; McIDAS Video Chain Timing.

The Pixel Clock could be used as the basic Video Chain Timing except for the requirement that the operator be able to indicate a position within the TV raster to a resolution of one pixel. This requirement, along with the fact that the DR-10A Video Disk locks up to station sync, only to within $\pm$ 2 pixels (resulting in the TV image drifting within the TV raster), led to the use of the DR-10A disk surface as the Pixel Clock reference. One TV frames worth of the above described Pixel Clock is recorded on a special fixed head track on the outside diameter of the disk. This recording is done only once, and from then on it is played back and used as the Pixel Clock for the entire McIDAS Video Chain. In this manner, as the disk servo hunts and drifts, the Pixel Clock shifts accordingly and thereby remains fixed in relationship to the image.

The implementation of this record capability involves D Flip Flop's chip 3060A, 3060B, Gate chip 3000 pin 1 and the Timing Track Record Switch. When the switch (which is an IC switch mounted in a socket on the P.C. board itself) is depressed, D flip flop's 3060 A & B generate an enable gate equal to one TV frame interval in synchronism with the Frame Sync Signal from station sync. The gate allows the Horizontal Drive pulses to get through gate 3000 pin 3 and release the $\div$ 4 counter (74S112 A). The 12 MHz pixel clock is not

recorded directly, but is first divided by two via D Flip Flop 3060C pin 5 in order to be more compatible with the bandwidth of the DR-10A Video Disk. This signal goes directly to the RAPA board via coax driver 0033 A and gets recorded directly. It is not FM encoded. Also, the one TV frame Enable Gate is sent to the DR-10A Video Disk as the Record Enable via line driver 109 C.

After being recorded once, the Pixel Clock is continuously played back from the Timing Track of the DR-10A Video Disk and sent to the Timing Generator where it is amplified and detected to be a 6 MHz square wave by amplifier AM-103. The squared up output is fed to comparator 760C which detects the zero crossings and generates a TTL compatible square wave. This 6 MHz Pixel Clock is then doubled to 12 MHz by the x2 mono (chips 74S00 A, B, & C) to produce the 12 MHz Pixel Clock (chip 74S00 C pin 3). It is important that the 12 MHz pixel clock have a 50% duty cycle at this point because both edges are used later. Trimpot (1) controls the offset of output amplifier AM-103. Because comparator 760 C detects zero crossings referenced to signal ground, adjusting the offset has the effect of adjusting the duty cycle of the 12 MHz Pixel Clock.

For maximum flexibility, the Timing Generator is designed to allow the McIDAS Video Chain to operate in either the Timing Track mode (External) or the oscillator mode (Internal). The Clock Switch located within the Timing Generator Bay, selects between Internal Clock and External Clock. In the External Clock mode, the Timing Generator works as described above and uses the Timing Track of the DR-10A Video Disk. In the Internal mode, one pole of the Clock Switch enables the ÷ 4 counter to be continuously controlled by the ÷ 700 counter and thereby continuously generate the Pixel Clock. The second pole of the Clock Switch selects this Pixel Clock instead of the detected Pixel Clock from the DR-10A Video Disk.

The selected Pixel Clock is sent to the Fast Storage and the Digital Cursor as the Pixel Clock Signal via line driver 109 B Pin 12 & 13. It is also sent to the Enhancement Tables as the Latch Signal via line driver 109 C pin 12 & 13. It is also sent to the Priority Control (which is in the same package) without a line driver. A 30 nsec pulse is generated on the positive going edge of this Pixel Clock (gate .chip 7400) and sent to the high speed analog to digital converters (HS 6-15) as the Convert Commands via coax driver 0033 B.

It is important to understand that the design of the McIDAS Video Chain assumes all timing is referenced to a single source of Pixel Clock. This source is TP-1 (gate chip 74S00 C pins 4 & 5). Proper operation is dependent on the Pixel Clock signal being distributed to the various use areas with a constant, known transmission delay time. Since the Pixel Clock period is about 80 nsec, the transmission time through 10 feet of twisted pair wire and a line driver and receiver is appreciable. In addition, the throughput delay of certain components (such as the HS6-15 ADC's) is greater than one Pixel Clock period, and therefore the concern is for timing being correct in terms of integral numbers of Pixel Clock cycles. For instance, the Convert Command to the H56-15 and the latch signal to the final stage of the Enhancement Table are generated at the same time. However, the first couple of latch signals do nothing useful because the data asked for by the first convert command still has not been generated nor has it worked its way through the Enhancement Table.

In order to facilitate the initial setup of this critical timing, gate 74S00 C pin 6 was added, along with a jumper matrix, to allow either the Pixel Clock or its complement to be sent to the various destinations. This gave a 40 nsec differential delay adjustment which proved sufficient to ensure proper timing.

VIDEO DISK SUBSYSTEM

Refer to FIGURE 12; McIDAS Video Chain Detailed Functional Block
Diagram & FIGURE 2; McIDAS System Detailed Functional Block
Diagram

The purpose of the Video Disk Subsystem is to accept the single
T.V. Lines of data from the Fast Storage and record them in sequence to
produce a recorded T.V. Frame; to record up to 500 of these T.V. images;
and to play them back at the 30 frames per second rate necessary to re-
fresh a standard T.V. monitor.

The Video Disk Subsystem consists of an Ampex DR-10A Video Disc
Recorder, which contains the magnetic surfaces, flying heads & electronics
to do the actual recording and reproduction of the T.V. images; a DR-10A
Interface by which the McIDAS Computer Subsystem controls the operation
of the DR-10A Video Disc Recorder; and a Fail Safe Monitor package which
insures that the DR-10A Video Disc Recorder will not have catastrophic
head-disk interface failures. Detailed information on the DR-10A Interface
and the Failsafe Monitor is not available at this time and will be provided
at a later date.

The DR-10A Video Disc Recorder was purchased from Ampex Corporation
and has not been appreciably modified. Detailed information on the theory
of operation, as well as maintenance procedures, interface criterion, and
schematic detail is available in the Manual. Suffice it to say that it is
because the DR-10A Video Disc Recorder can record a T.V. image one line at
a time over a period of approximately three minutes, store up to 500 of
these images, and then continuously play them back at the T.V. rate of 30
frames per second, that the interactive capabilities of the McIDAS System
are possible.

ENHANCEMENT SUBSYSTEM

GENERAL

The purpose of the Enhancement Subsystem is to accept the analog TV video signals from the Video Disk Subsystem; to perform an enhancement so that a useful range of the 64 input gray levels (dynamic brightness range) can be displayed on the roughly 16 discernable gray levels and the over 200 discernable colors of the video monitor; and to produce the resultant video in a format that is directly compatible with an RGB standard color video monitor. Refer to FIGURE 12; McIDAS Video Chain Detailed Block Diagram.

The basic philosophy is to accept the analog video signals from the DR-10A Video Disk during playback and to digitize them to 6 bits (one part in 64) utilizing the Pixel Clock, so that the enhancement process can be performed on digital data. The advantage of enhancing the data digitally as opposed to working directly with the analog video, is that more interesting types of enhancement can be implemented. Each of the 64 input levels can be uncompromisingly converted to any of the 64 output levels without regard for where it is in the input range or what input or output levels the neighboring pixels might be. This means that useful and difficult functions such as step functions, negative resistance regions, and discontinuities can inherently be performed.

The disadvantage of course, is that the analog video which originally started out as digital data in the computer and was converted to analog in the Fast Storage in order to be recorded on the DR-10A Video Disk, must now be reconverted to digital in order to be enhanced. And, after being enhanced, must be reconverted to analog to be compatible with the standard RGB video format. This digital to analog to digital to analog conversion chain does result in degradation. However, by doing all the conversions in phase with

the same Pixel Clock the degradation is minimized. See FIGURE 14; Resampling Comparisons.

ENHANCEMENT TABLE

The actual enhancement is performed using "lookup tables". Each lookup table within the Enhancement Tables, has digital storage for 64 6 bit words and the digitized video is used as an address for interrogating one of the memory locations. As each 6 bit pixel sample is generated by the ADC, it is applied as an address location to the lookup table, and the 6 bit word stored at this location, is non-destructively read and used as the pixel value instead of the original ADC sample value. This new pixel value is applied to a digital to analog converter (DAC) where it is converted back to an element of an analog video signal. In this manner, and at the pixel rate of 12 MHz, the analog video signal from the DR-10A Video Disk is digitized, enhanced, and reconverted back to the analog video format.

It remains now for the computer to calculate the required transformation to give the required enhancement and to load these values into the lookup table. This loading phase is accomplished via the Address Mux and the Load Sequencer, and need be done only once for each time the enhancement is updated. It is not necessary for the Computer to interact with the data at the pixel rate in order for enhancement to be accomplished in real time.

To produce the three separate signals required for color information (the red, green, and blue components), it is necessary to have three Enhancement Tables each with its own lookup table. All three lookup tables receive the same pixel value from the ADC to be used as the memory address, but each has a different digital value stored at that address location. One represents the value for the red component of the desired color response to that pixel value; the second contains the green component; and the third the blue component.

Colorimetry says that all perceivable colors have unique values of hue, saturation and brightness. The hue indicates the dominant wavelength of the color; saturation is a measure of the relative amount of white light mixed with this wavelength; and brightness is a measure of the intensity (energy per unit area) normalized to the intensity response function of the human eye. The hue and saturation information is contained in the relative values of the red, green and blue components, and the brightness information is contained in the absolute values of the red, green, and blue components. If the red, green, and blue components are always equal, then a black and white image is generated. Consequently, by the straightforward generation of three digital values for each possible input pixel value, a very powerful enhancement capability is defined.

Two lookup tables are provided in each of the red, green and blue Enhancement Tables. This allows two independent video sources to be enhanced simultaneously. The digital outputs of the two lookup tables go through the Digital Mux before they are applied to the DAC. Control signals to the Digital Mux then allow pixel by pixel selection of one video source or the other. Actually the Digital Mux has two other digital inputs which originate in the Computer via the Digital Interface. These digital inputs which originate in the Computer via the Digital Interface. These digital values represent "background" colors which can only be changed at the T.V. frame rate and serve as fill color for the two prioritized overlays known as Grid and Cursor. The Grid overlays both data sources and the Cursor overlays the data sources and the Grid. This prioritized overlay, as well as data source selection, is controlled by the Video Sequencer.

ANALOG DISTRIBUTOR

See Analog Multiplexer Schematic and FIGURE 12; McIDAS Video Chain Detailed Functional Block Diagram

The Analog Distributor consists of two Analog Multiplexer circuits, each with the same set of six inputs. Each Analog Multiplexer selects one of the six analog inputs, and presents it to one of the two high speed analog to digital converters (HS6-15). At the present time only the two analog video outputs of the DR-10A Video Disk are used as inputs to the Analog Distributor, and the input voltage range is 0 to 1 v pp into 75 ohms. The HS6-15 ADC requires a 0 to 2.048 v p-p input for full range digital output. It should be noted that the Analog Multiplexers and the HS6-15 ADC are direct coupled and any signal source which exceeds the prescribed input voltage ranges will result in improper operation of either or both units.

The Analog Multiplexer consists of an operational amplifier wired as an inverting type summing circuit, and consists of operational amplifier unit 103A-I and six Input Stages. Refer to the Analog Multiplexer schematic for the mathematical description. These Input Stages consist of a 15.3k ohm precision resistor (three 5.1k ohm) with a double grounding stage implemented with two enhancement mode FET's and a driving transistor. In normal operation, both FET's in all input stages are in the low impedance state which in turn sets all input signal voltages to zero at the input to the summing amplifier. When a channel is selected by bringing the appropriate channel select signal (from the Digital Interface) high, the two FET's for that channel go to the high impedance state and the signal is applied to the summing amplifier. The gain of the summing amplifier stage is one-third for the signal selected.

The summing amplifier is followed with one stage of inverting gain consisting of operational amplifier unit 103A-II. This circuit re-establishes the proper signal polarity and provides for an overall gain for the Analog

4-59

Multiplexer of four. This gain is necessary in order that a one volt

signal at the input will produce a two volt output into 75 ohm, after the coax

driver unit 0033.

ANALOG TO DIGITAL CONVERTER

The purpose of the two HS6-15 high speed analog to digital converters purchased from Computer Labs Inc., is to digitize the analog outputs of the Analog Distributor to six bits (one parts in 64) at the Pixel Clock rate of 12 MHz; and to provide this digital output to the Address Muxes and thereby to the Enhancement Tables.

The HS6-15 were built by Computer Labs Inc. are not modified in any way. Neither do they require any internal maintenance. A front panel check feature is provided which should be exercised on a routine basis, but because of the state of the art design of these units, they will probably work better and for a longer period of time if they are just left alone.

Further details on the specifications and operation of the HS6-15 can be found in the manuals provided with the units.

ADDRESS MUX

> Refer to Address Multiplexer Schematic and FIGURE 12; McIDAS Video
> Chain Detailed Functional Block Diagram

Two Address Muxes are used and both are physically mounted in the Timing

Generator package. The purpose of the Address Mux is to select the appropriate

address to be sent to the lookup tables within the Enhancement Tables. Each

Address Mux supplies the address for a set of lookup tables consisting of one

table in each of the red, green, and blue Enhancement Tables.

When loading the Enhancement Tables with a new enhancement, the Address

Mux selects the address generated by the Load Sequencer. After the enhance-

ment has been loaded, the Address Mux selects the address generated by the

HS6-15 ADC. The Address Mux serves only as an implementation of the selection

process and does not decide when to make a particular selection. It merely

responds to the direction of the Computer which activates either the Read or

the Write control bit via the Digital Interface. The Read bit causes the

HS6-15 ADC address to be selected, and the Write bit selects the load Sequencer

Address.

The layout of the lookup tables within the Enhancement Tables, requires

a special encoding of the Channel Address. It is not a straight 6 bit

binary code. The four least significant bits (LSB) have straight binary

weights, but the two most significant (MSB) bits are decoded to the one-of-four

format. This is done in the Address Multiplexer with the result that the

channel address is an eight bit address with 64 possible legal states. The

sequence is shown in the Address Multiplexer schematic. Both the multiplexing

function and this decoding function is performed with eight AND-OR-INVERT

gates (3034 A through H).

The Load Sequencer is used to generate the sequential addressing

necessary to load the lookup tables and thereby eliminates the need to send

an address along with each Data Word from the Computer. The Load Sequencer
is located in Address Mux A but its output is supplied to both Address Muxes.
To start a load sequence, the computer first sends a word with the Load
Sequencer Reset bit active (high). In response to this, the Digital Inter-
face sends a zero going reset pulse to the Load Sequencer to initialize it
to the zero state (000000). Then the Computer sends out a word containing
the digital value to be loaded into this zero address location; a one in the
Load Sequencer Clock bit position; and a one in the Write Enable bit position.
This results in the digital value being written and the Load Sequencer being
loaded in the next address location, along with the Write Enable and Load
Sequencer Clock bits high. In this manner the entire lookup table is
loaded.

Keep in mind that to load a lookup table means to load one of the two
lookup tables in each of the three Enhancement Tables (red, green, and blue).
Refer to APPENDIX C: Digital Interface Bit Assignments.

ENHANCEMENT TABLES
    See Enhancement Table Schematics and FIGURE 12; McIDAS Video Chain
    Detailed Functional Block Diagram

    The purpose and general operation of the Enhancement Tables, including

the Digital MUX and the DAC's, is explained above in the General section of

the Enhancement Subsystem.

    The original design of the Enhancement Table provided for three lookup

tables and the printed circuit board is layed out accordingly. At present

however, only two lookup tables have been activated and the third probably

never will be.

    The memory chips used are the Intel P3101 static 64 bit RAM, which has

the quad 16 bit organization and a read cycle time of 35 nsec. Two chips

are operated together to give an eight bit by 16 word organization (only

6 of which are used). Four such sets give the required 64 word locations.

Because of this organization, the four least significant bits of the address

is used to sequence through the 16 states of all eight chips and the two

most significant bits are decoded to select one of the four sets of two

chips at a time, by using the Chip Select (CS) inputs. This decoding is done

in the Address MUX which provides this address to the lookup tables. The

Channel A Address comes from Address Mux A via receiver chips 107 F, G, H & I;

and the Write Enable A pulse comes from the Digital Interface via receiver

chip 107 E pin 4. Likewise, the Channel B Address comes from Address Mux B

via receivers chips 107 X, ZZ, Z and Y and the Write Enable B pulse comes

from the Digital Interface via receiver chip 107 W pin 4.

    The Input Enhancement Data which is to be loaded into the lookup tables,

is received from the Digital Interface via receiver chips 107 J, K, & L and

is applied to both lookup tables within each Enhancement Table. It is loaded

into one or the other or both lookup tables depending on whether Chip

Enable A or Chip Enable B or both is sent.

The Digital Mux section of the Enhancement Tables is implemented with six MC3032 AND-OR-INVERT gates (chips A through F); and three MC3023 AND-OR INVERT gates (chips A, B, & C). It is really a five channel by six bit mux. The five channels are for three data channels and two prioritized overlay channels. It is also a two level mux with the first level having four channels. Three of these first level channels are for the three data channels and the fourth is the overlay channel. Either the cursor or the grid overlay is routed to this overlay channel by the second level of multiplexing which utilizes the three MC3023 chips.

The state of the Digital Mux (i.e. which of the five channels is selected) is determined by the Channel Control signals from the Video Sequencer on a pixel by pixel basis via receiver chips 107 M & N. The selected six bit word is applied to the Latch (D flip flop chips A,B, & C), whose purpose is to present all six bits of each pixel to the DAC simultaneously. Because the six bit word originated in the HS6-15 ADC and propagated through the Address Mux and through the lookup table and the Digital Mux, it cannot be expected that all six bits will present themselves to the DAC at precisely the same time. The DAC is a Datel type DAC-HI with a response time of 25 nsec. If the bits ripple in, improper states will appear on the input of the DAC and it will accordingly produce glitches on the output. The latch is clocked according to the Pixel Clock, with the Latch Signal from the Timing Generator as received via receiver chip 1070 pin 9.

Horizontal Sync from the Timing Generator is also applied to the latch and is used to force the output of the DAC to zero during the horizontal sync interval. This is necessary only to the extent that the horizontal blanking of the T.V. monitor is successful in blanking data during the horizontal flyback time. If the blanking is not complete and if the signal happened to be high for the last pixel of the scan, the picture will look washed out.

The DAC-HI is a current mode output device and is terminated to produce a $\pm$ 1 volt swing into the 0033 coax driver, which means a 1 volt p-p level into 75 ohms.

VIDEO SEQUENCER

Refer to Video Sequencer Schematic and FIGURE 12; McIDAS Video Chain Detailed Functional Block Diagram

The Video Sequencer implements the Computers choice of the various prioritized combinational capabilities of the Digital Mux within the Enhancement tables. The Single Channel Select One mode (receiver chip 107 D pin 9) will activate Channel Control One which in turn will cause the Digital Mux of all three Enhancement Tables (red, green, and blue) to select the outputs from lookup table A. Likewise the Single Channel Select Two will cause lookup table B of all three Enhancement Tables to be presented to the DAC.

In either case, however, this selection is subject to be superceded by either the Cursor Control Bit or the Grid Control Bit. These two selection bits have priority over the Channel Select bits on a pixel by pixel basis, and in addition, the cursor control bit has priority over the Grid Control Bit. This allows for an overlay capability. To date, two sources of overlay is possible. One is from the Digital Cursor Generator and the other is from the Level Discriminator. One or the other can be routed by the computer, to be either the Cursor Control Bit or the Grid Control Bit by means of the Digital Mux.

Both the Cursor Control Bit and the Grid Control Bit force the Video Sequencer to the Channel Control four state. In addition, the Cursor Control Bit forces Channel Control Cursor (4A) and the Grid Control Bit forces Channel Control Grid (4B). These Channel Control signals force the Digital Muxes in the Enhancement Table to present the Computer generated background colors to the DAC and thereby a colored overlay is produced on the image.

With the Matting Select bit active (from the computer via the Digital Interface) the Digital Mux switches between lookup table A and lookup table B on the basis of the state of the Matting Control Bit. This Matting Control Bit is similar to the Cursor and Grid Control Bits in that it can change at pixel rates and is selected from a number of sources via the Digital Mux; and

it generates a sort of overlay. However, in the Matting Mode, the overlay

is filled with a second data source instead of just a background color.

In addition, the Grid & Cursor Control Bits will still overlay the matting

sequence to produce three levels of overlay.

It should be pointed out that the Cursor, Grid, and Matting modes all

produce overlays and not blends. As such, they "punch a hole" in the data and

fill it either with a background color or with other data. However, the

original data is gone in all cases. Blending, implies a mixing effect which

would be useful, but is not directly available with the present Video Chain

design.

Still one more capability is present. This is the Pixel Interlace (2)

mode. When this mode is selected (receiver 107 A pin 9) a signal generated by

dividing the pixel clock by two with D Flip Flop in C3060 B pin 9, is used to

alternatively select Channel Control One and Channel Control Two. In this

way, the data from lookup table A and lookup table B (both at half horizontal

resolution) is simultaneously displayed. In this mode, the Cursor and

Grid overlay capability is active so that two pictures can be simultaneously

viewed with two levels of overlay present.

DIGITAL MULTIPLEXER

Refer to Digital Multiplexer Schematic and FIGURE 12; McIDAS Video
Chain Detailed Functional Block Diagram

The Digital Mux is really three digital multiplexers and is used to
select the Cursor Control Bit, the Grid Control Bit, and the Matting Control
Bit from up to six digital inputs, and to supply them to the Video Sequencer.
The six digital inputs are common to all three digital multiplexers, but
the control lines from the Digital Interface are peculiar to each digital
multiplexer. This means that the Cursor, Grid, and Matting Bits are chosen
from the same sources; but need not all select the same source.

The Digital Mux is implemented using the MC3032 AND-OR-INVERT gate with
type MC3018 expander gates. One set is used for each of the three digital
multiplexers and the output is active when it goes low.

The digital inputs at present are the cursor bit from the Digital Cursor
Generator, the Level Discriminator Bit from the Level Discriminator, and the
Complemented Level Discriminator Bit also from the Level Discriminator.

FAST STORAGE
    Refer to the Fast Storage Schematic and FIGURE 12; McIDAS Video
    Chain Detailed Functional Block Diagram

GENERAL

The Fast Storage provides the sequencing and the data buffering necessary

to allow the McIDAS computer to store digital data on the DR-10A Video Disk

in standard T.V. format.

The McIDAS T.V. image format is 525 lines with 700 pixels per line at

30 frames per second. To the computer this means that to load an image it

must provide a six bit data word for each of the 700 pixels for each of the

525 lines. Each one of these pixels must be recorded on a track at a specific

angular location of the magnetic disc in the DR-10A Video Disk. The specific

angular position for each pixel is defined in the Timing Generator utilizing

the Frame Clock, Line Clock and Pixel Clock.

The computer has no difficulty providing the quantity of data required

for an image (it represents less than 16K of core), however, it cannot output

the data fast enough to allow it to be recorded properly. The average pixel

rate for a T.V. frame is:

525 lines/frame x 700 pixels/line x 30 frames/sec = 11.0 MHz.

The computer would have to output 11×10^6 6 bit words or 2.75×10^6 computer

words per second for 1/30 of a second. The very best the Datacraft 6024/5

can do is 0.33×10^6 words per second.

This difficulty was solved with the Fast Storage. The Fast Storage

accepts the data from the Computer at whatever rate it can be provided; it

stores it in digital form; and then reads it out of memory, converts to it

the analog video format required, and presents it to the DR-10A Video

Recorder properly phased relative to Frame Clock, Line Clock, and Pixel

Clock. In this respect, the Fast Storage acts as a data buffer between the digital realm of the computer and the T.V. format of the DR-10A Video Disk.

The size of the memory required to implement the Fast Storage was greatly reduced when it was realized that an image could be recorded on the DR-10A Video Disk one T.V. line at a time. This means the Fast Storage memory need only store 700 6 bit words.

MEMORY

The Fast Storage Memory is implemented with Signetics Type 2503TA Dual 512 bit Dynamic Shift Registers. These chips have a typical maximum data shift rate of 10 MHz and a measured storage time of about 50 msec. (Specifications for the 2503TA is included in APPENDIX B; Misc. Data Sheets). They are a multiplexed shift register (i.e., each 512 bit section is really two 256 bit sections with the outputs and inputs interleaved on a bit by bit basis) and therefore require a two phase clock. They are also MOS without TTL compatible clock inputs and therefore require a high current clock driver.

The Fast Storage Memory is organized as two 512 8 bit word memories with the outputs and the inputs interleaved on a bit by bit basis quite similar to the 2503TA chips themselves. This provides a memory with 1024 8 bit word capacity with a data rate upwards of 20 MHz and a storage time of approximately 50 msec. This means the 12 MHz word rate is well within chip specification.

Memory chips 2503TA A, B, C, and D comprise one 512 8 bit word memory and chips 2503TA E, F, G, and H comprise the second 512 8 bit word memory. The 6 bit Digital Data to be stored comes from the computer via the Digital Interface on receiver chips 107 E, F, and G and is inverted before being simultaneously presented to both sections of the memory by gate chips 8480 G and H. During unloading, the 6 bit data from the two sections of the memory is interleaved by a two channel digital multiplexer consisting of gate chips

8H80 C, D, E, and F. Gate chips 8H80 A and B provide the final ORing for

the digital multiplexer and present the data to the high speed digital to

analog converter. This DAC is the Patel type DAC-HI, which has a settling

time of 25 nsec. It has a current mode output and is wired to produce a $\pm$ 1

volt output into the 2.32K terminating resistor. This signal is sent to

the DR-10A Video Disk via coax driver 0033 as a 1 volt peak to peak (into

75 ohm) video signal. A specification sheet for both the DAH-HI and the

0033 is included in APPENDIX B: Misc. Data Sheets.

Because the memory is organized as two levels of interleaved data, it

requires a four phase clock. The Fast Storage Four Phase Clock Driver is

unique in that the two opposing clocks do not overlap each other and the

duty cycle of the clocks remains constant over the entire input clock range

of 20 MHz to less than 1 kHz. In addition, it will work over a wide range

of input clock duty cycle variations (10% to 90%). A timing diagram for the

Four Phase Clock Driver is shown on the Fast Storage schematic for both the

Load and the Unload Mode.

The actual driving of the high capacitive load presented by the clock

inputs of the 2503TA shift register, is done by the National Semiconductor

NH0012 MOS Clock Driver chip, which can output a peak current of 1 amp at

repetition rates of 10 MHz. A specification sheet is included in APPENDIX B:

Misc. Data Sheets.

CONTROL

In addition to providing memory for storing one T.V. lines worth of data,

the Fast Storage also provides the control which loads the data into the proper

T.V. line. The 10 bit counter (one part in 1024) consisting of chips 8284

A, B, and C is constantly counting the Line Clock signals as received from the

Timing Generator via receiver 107G pin 9. It is reset every T.V. frame with

the Frame Clock, which comes from the Timing Generator via receiver 107G

pin 4. In this manner the Fast Storage Control knows which T.V. line is

under the record/reproduce head of the DR-10A Video Disk at all times.

The Computer initiates a T.V. line loading process by sending the first

6 bit word along with an active (high) Load Clock, to the Fast Storage via

the Digital Interface. The Load Clock arrives from the Digital Interface as

a pulse at receiver 107 N pin 9. Because the End Loading bit is low,

(receiver 107 N pin 4) this Load Clock pulse is routed to the Four Phase

Clock Driver via gates 8H80 J pin 3 and 8H80 B pin 12. Assume for the

moment that the Four Phase Clock Driver and the latch chips 8202 A and B have

been properly initialized. This clock pulse causes the data word to be loaded

into the first location of the memory. The computer then sends another Load

Clock and the second data word, and it is stored in the second memory location.

This is repeated at a rate determined by the Computer(but greater than 1 KHz)

until all 700 words have been loaded.

Now however, because the Fast Storage memory is 1024 bits deep and has

a first in--first out configuration, the computer must send 324 "fill" words.

These fill words are all zero's and are sent in exactly the same way as the

data words.

When the Computer sends the last fill word, it also sends the End

Loading Bit and a 10 bit word to determine on which T.V. line this data is to

be loaded. This T.V. Line Number arrives via receiver chips 107 A, B, C, D,

and N and is stored in the gated latch consisting of chips 8202 A and B.

Subsequently, it is compared to the state of the T.V. line counter with chips

8242 A, B, and C. When the DR-10A Video Disk is interrogating the area of the

track which corresponds to the T.V. Line Number sent, a coincidence pulse is

generated and applied to D flip flop 8828 F pin 3. The leading edge of the coincidence pulse toggles the D flip flop if the End Loading Bit is active (high). This gates the Pixel Clock to the Four Phase Clock Driver via gate chips 8H80 I pin 6 and 8H70 B pin 12 and sends the Record Enable to the DR-10A Video Disk to put it in the record mode for one T.V. line. It also triggers mono 8162 C pin 11, which generates a 200 nsec pulse which initializes the Four Phase Clock Driver just before the Pixel Clock unloads the memory.

After the T.V. line is loaded, the lagging edge of the coincidence pulse clocks mono 8162 B pin 11 which generates a 200 nsec pulse to initialize the Four Phase Clock Driver so that the memory will be ready to receive another T.V. lines worth of data.

The purpose for the latch (chips 8202 A and B) is so that the Fast Storage can be totally independent of the computer during the Unload mode. As long as the End Loading bit is low, the latch is clocked and loaded with each Load Clock pulse from the computer via gates 8H80 J pins 8 and 3. However, the leading edge of the Load Clock pulse which is sent with the End Loading Bit, loads a high into pin 22 of 8202 A and thereby stops any more Load Clock pulses from effecting the Fast Storage until the latch is reset. This Load Clock disabling, also triggers mono 8162 D which initializes the Four Phase Clock Driver in preparation for the memory unloading. At this point the Fast Storage Control has the T.V. Line Number latched and the Four Phase Clock Driver initialized and the Pixel Clock enabled and is waiting for the coincidence pulse to be generated. After unloading is completed, the lagging edge of the coincidence pulse triggers mono 8162 B pin 11 which resets the latch to make the Fast Storage once more responsive to Computer control.

Note that the latch resetting produces the lagging edge of the Unload
Completed Signal (driver chip 109A pins 1 and 2) which could be sent to the
computer as an interrupt to indicate when the next T.V. line could be sent
out. At the present time this signal is not used. The Computer simply
waits a minimum of 33 msec and assumes the load is complete. A slight
inefficiency results because on the average it should take only 16 msec to
unload the Fast Storage memory. However, the transfer rate through the
Fast Storage is not even close to being the limiting factor in T.V. image
loading time and the additional 16 msec is not important.

DIGITAL CURSOR GENERATOR

Refer to Digital Cursor Generator Schematic and FIGURE 12; McIDAS Video Chain Detailed Functional Block Diagram

The Digital Cursor Generator works in conjunction with the Video Sequencer to produce a cursor superimposed on the McIDAS image at a precise line and pixel position. The type, horizontal size, vertical size, and position of the cursor is determined by the Computer via the Digital Interface. The thickness of the cursor outlines is controlled with internal jumpers. The Digital Cursor Generator uses the Frame Clock, Line Clock, and Pixel Clocks from the Timing Generator to define the position and size of the cursor to one line and one pixel resolution.

Three basic types of cursors can be generated with a fourth type (a combination of two basic types), also being possible. All cursors are of the rectangular shape consisting of either vertical or horizontal lines. The basic cursor shapes are the Solid Rectangle, the Outlined Rectangle, and the Crosshair. Any combination of these basic types is possible, but only one is unique and that is the Outlined Rectangle with centered Crosshair.

In normal operation, the Digital Cursor Generator receives a 10 bit straight binary word from the Computer via the Digital Interface, specifying the vertical position of the upper left-hand corner of the cursor. This binary word indicates the vertical position in terms of the number of T.V. lines of the 525 line raster, which have been scanned since the last Frame Clock.

Note that the Line Clock (Horizontal Sync) is counted in a sequential manner and not in an interlaced manner. This means that line 120 (for instance) is not vertically adjacent to line 121. Line 121 is two raster lines away. The next line vertically adjacent to line 120 is line 262+120 = 382.

Consequently to move the cursor vertically down, one raster line at a time, the Computer must generate a sequence of vertical position words according to the following expression: X; 262+X; X+1; 262+(X+1); X+2; 262 (X+2), etc.

The Computer also sends another 10 bit straight binary word to indicate the pixel position of the upper lefthand corner of the cursor. This word indicates the number of Pixel Clock intervals from the last Line Clock (horizontal sync). In this manner, the cursor is positioned within the T.V. raster to a resolution of one line and one pixel.

If the McIDAS Video Chain is operating in the External Pixel Clock mode, (which means the basic Pixel Clock is derived from the DR-10A Video Disk Timing Track via the Timing Generator) then the cursor is positioned accurately with respect to the image no matter how much the disk servo of the DR-10A Video Disk may be hunting. If the McIDAS Video Chain is operating in the Internal Pixel Clock mode (which means the basic pixel clock is derived from the crystal oscillator within the Timing Generator) then the cursor is positioned accurately within the T.V. raster, but within the image only to the extent that the DR-10A Video Disk servo is locked to Station Sync.

The generation of a cursor begins with the Cursor Line Position counter (binary counter chips 8284 A, B, and C) being reset by the Frame Clock, indicating the beginning of a T.V. raster. On subsequent Line Clocks, this counter advances, until its count is the same as the 10 bit word sent from the Computer representing the upper left band corner vertical position. This "coincidence" state is detected by bit comparator chips 8242 A, B, and C by bringing low the Rectangle Top signal (Chip 8H80 A pin 11). This sets D flip flop chip 8828A to produce the Pixel Enable signal (chip 8828 A pin 5). Note that the Line Clock is a narrow pulse which means that the Cursor Line Position counter is advanced at the very beginning of the line and therefore

the Pixel Enable signal is first generated during the line which is the line wanted; not one before or one after. The Line Position Counter continues counting the Line Clock until it is again reset by the Frame Clock, and therefore the Rectangle Top signal is active for only one T.V. line.

The Pixel Enable signal is used to enable the Vertical Size Counter (chips 8284D and E) which begins to count the Line Clock. This counter determines how many T.V. lines the vertical size of the cursor will be. When the state of this counter is the same as the 8 bit word sent by the Computer as the vertical size the cursor is to be, the 8 bit comparator consisting of chips 8242 D and E, goes low for one line to produce the Rectangle Bottom signal (gate chip 8H80 A pin 8). The lagging edge of this signal (the end of the last line) clocks D flip flop 8828 A pin 5 which removes the Pixel Enable signal. The two signals now generated, Rectangle Top and Rectangle Bottom, are each one T.V. line wide and comprise the vertical boundaries of the cursor.

The state of the Cursor Vertical size counter is also compared to the vertical size word from the Computer by chips 8242 F and G. In this case however, the weights of the vertical size word have been slipped by one bit relative to the Cursor Vertical size counter; i.e., the most significant bit of the vertical size word is compared to the second most significant bit of the cursor vertical size counter. (chips 8242 E pins 8 and 9.) This arrangement has the effect of always producing a coincidence midway between the upper and lower vertical boundaries of the cursor no matter what size is sent from the Computer. This midpoint coincidence pulse is called the Horizontal Crosshair signal and is one T.V. line wide.

In a manner exactly analgous to the above, counter chips 8284 F, G, H, I, and J and digital comparator chips 8242 H, I, J, K, L, M, and N produce the Rectangle Left side, Rectangle Right side and Vertical Crosshair signals. The only differences are that the counters are reset with the Line Start signal and clocked with the Pixel Clock signal. Also, bit comparisons are allowed only within the upper and lower vertical limits of the cursor by means of the Pixel Enable signal as applied to the last two stages of the comparator chip 8242 J pins 9 and 12 (8 and 13). Because this is so, the signal on pin 9 of D flip flop chip 8828 A is active (high) only during that portion of the raster contained within the upper, lower, left and right boundaries of the cursor and is labeled the Rectangular Area signal.

At this point, all the signals necessary to generate the required cursor types have been generated. It remains only to combine and select them. Rectangle Top, Rectangle Bottom, Rectangle Left side and Rectangle Right side are ORed in gate chip 8416 A pin 8 and ANDed with Rectangle Area in gate chip 8H70 A pin 6 to produce the Rectangle Outline cursor if it is selected by the Select Rectangle Outline bit (receiver chip 107L pin 4). Horizontal Crosshair is ANDed with Rectangle Area (8H80 B pin 3) and then ORed with Vertical Crosshair (8H80 B pin 6) to produce the Crosshair cursor (8H80 B pin 8) if it is selected by the Select Crosshair bit (receiver chip 107K pin 9). Rectangle Area is selected (8H80 B pin 11) by the Select Rectangle Area bit (receiver chip 107 K pin 4)to produce the Rectangle Area cursor. The signals to generate the required cursor pass through OR gate (chip 8H16 A pin 6) to transmitter chip 109 A pin 1 and 2, and then on to the Digital Mux.

Before leaving the Cursor Generator, it should be pointed out that the above discussion assumes the width of all vertical and horizontal cursor boundaries are one pixel and one line respectively. This is so because all

coincidences were generated by comparing the counter state to the Computer word on a bit by bit basis, right down to the least significant bit (LSB). If however, the LSB's of the Computer word and the counter state had been forced to be always the same, then the cursor boundaries would be twice as wide (two lines and two pixels). Likewise, if the LSB and the second LSB were forced to always be the same, the boundaries would be four lines and four pixels. The ability to adjust the cursor boundary width is included in the Digital Cursor Generator in order to produce the mose useful cursor possible. On every bit comparator, the four least significant bits come from the receiver chips via a jumper matrix (see chip 8242 A pins 1, 6, 8, and 13). If a jumper is inserted as shown on the schematic; i.e., A to B, then the bit is active in the comparison and the appropriate cursor boundary will be narrow. If the jumper is inserted from A to C, then the two inputs of the comparator are tied together for that bit and the boundary will be wider by the weighting factor of that bit. A table is included on the Digital Cursor Generator schematic indicating how the jumpers should be inserted for specific line widths.

Note that the widths of the Rectangle Top, Rectangle Bottom, Rectangle Left Side, Rectangle Right Side, Horizontal Crosshair, and Vertical Crosshair are all independently adjustable by means of these jumpers. Be aware of the fact that the effective center of the cursor moves vertically and horizontally relative to the upper lefthand corner, a distance equal to half the width of the boundaries as the boundary widths are increased. A drawing insert is included on the Digital Cursor Generator schematic to illustrate this. This effect may or may not be important depending on how the cursor is being used and how wide the boundaries are, but it should be taken into consideration.

LEVEL DISCRIMINATOR

Refer to the Level Discriminator Schematic and FIGURE 12; McIDAS Video Chain Detailed Functional Block Diagram

The Level Discriminator package selects one of six analog video inputs and puts out a digital signal which is active whenever this input video level is between a lower and upper reference level as determined by the McIDAS computer. This digital signal can change on a pixel by pixel basis and is sent to the Digital Mux of the Video Sequencer where it can be used as the Cursor, Grid or Matting Control bits. This Level Discrimination capability is particularly useful in the Matting mode where corresponding areas of a second image can selectively replace the primary image on the basis of the gray scale information of the second image.

The Level Discriminator Package contains three different types of boards. One is a Buffer Board which contains six analog buffer amplifier circuits implemented with the 0033C coax driver chips. The purpose of the Buffer Board is to receive the six analog video signals and to provide them to the two 75 ohm loads represented by the two analog multiplexers. The Analog Multiplexers are the second type of board contained in the Level Discriminator Package and do the actual selection of which analog video signal is applied to the Level Discrimination Modules. The circuit details are shown in the Analog Multiplexer Schematic and a description of its operation is included in the Analog Distributer Detailed Theory of Operation. The third type of board within the Level Discriminator package is the Level Discrimination Modules themselves. The schematic indicates two of these modules in the Level Discriminator Package but to date, only Level Discrimination Module Number One has been implemented.

In addition to the Video Signal from the Analog Multiplexer, the Level

Discrimination Module receives two 6 bit words from the Computer via the Digital Multiplexer. One determines the lower limit of the range to be discriminated and the other determines the upper limit. These two 6 bit words are converted to an analog level with the Datel DAC 19-8BI Digital to Analog Converter and buffered with the 0033C coax driver. The output of the DAC is a current which passes through a selectable fixed resistor (SFR 1) to generate a voltage. This voltage is buffered with a 0033C coax driver and applied to the 760 comparator chip. SFR 1 is set to adjust the gain and SFR 2 is set to adjust the offset, so that the Reference Voltage to the Comparator is 0.0 to 1.0 volt full scale.

Both the Lower Comparator (chip 760 A) and the Upper Comparator (chip 760 B) receives the Video Signal and the appropriate Reference Voltage with a precise 0.0 to 1.0 volt full scale range. The comparator circuits have a hysteresis of about 20 mv determined by the 15K ohm feedback resistors and the 75 ohm input resistors. Hysteresis is desirable to eliminate oscillations due to noise on the video signals. The 20 mv hysteresis selected is more than one bit resolution of the Level Set Words from the computer (1/64 of 1 volt = 15.6mv) but appears to be necessary based on imperical tests of Level Discriminator performance.

The Lower Level Comparator is active whenever the input Video Signal is above the lower limit as established by the Computer. The Upper Level Comparator is active whenever the input Video Signal is above the upper limit as established by the Computer. Gate chip 8H80 A pin 3 AND's these two outputs to produce the desired Discriminator Output signal. Refer to the Timing Diagram on the Level Discriminator package schematic. Both the Discriminator Output and its complement, are transmitted via line driver 109A to the Digital Mux where they can be selected to be the Cursor, Grid or Matting Control Bits to the Video Sequencer.
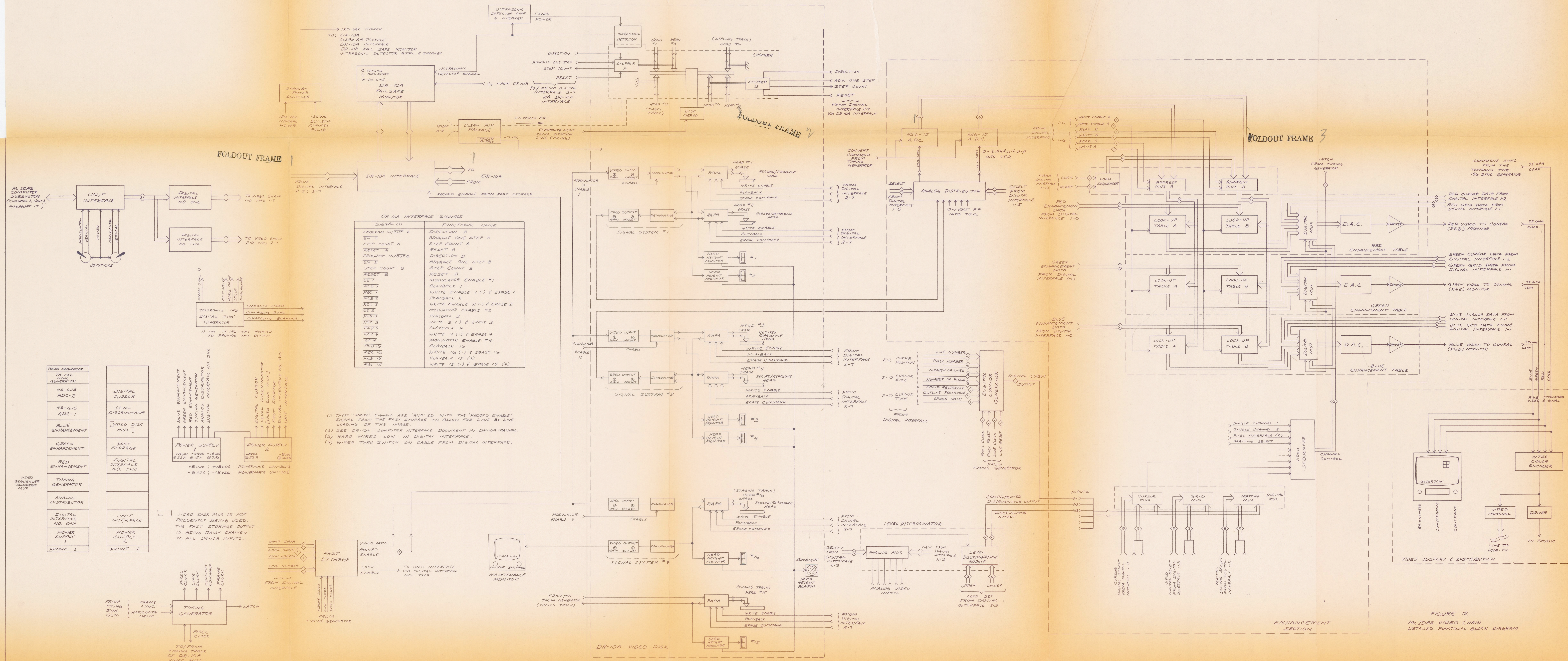
VIDEO DISPLAY & DISTRIBUTION
Refer to FIGURE 12; McIDAS Video Chain Detailed Functional Block
Diagram

The three Enhancement Tables each output a video signal without composite

sync at a level of ± 0.5 volt into 75 ohms. Four lines ,consisting of these

three video signals and composite sync, represent an RGB Standard Video

Signal, and as such,can be used, processed, and distributed utilizing standard

T.V. industry equipment. The stability of the Composite Sync. is determined

by the Tektronix type 146 Color Sync Generator and is very good. The TK 146

is a digital count down type sync generator and has a specified stability

of ± 4 nsec. The quality of the video is largely dependent on the DR-10A

Video Disk because it has the narrowest bandwidth (4.2 mHz) and because it

introduces image instability (in relationship to the T.V. raster) because of

disk servo hunting. However, even with these problems, the RGB Standard

Video Signal output from the McIDAS Video Chain is very acceptable.

The primary use for this Video Signal is to generate a color image for

the McIDAS operator to view. This is done with a studio quality Conrac RHM

video monitor. This 19 inch video monitor is an industry standard and in

no way degrades the image data. It is operated in the underscan mode to

allow the entire image to be viewed. It does require periodic convergence

adjustment, but otherwise is trouble free.

The McIDAS RGB Standard Video Signal is also applied to the Telemation

Model TCE-3000, NTSC Color Encoder. This device converts the signals to the

Color Composite standard format. As a Color Composite Video Signal, it needs

only one coax line to be distributed and is in fact sent to the small T.V.

studio on the 14th floor of the Meteorology & Space Science Building and also

sent to the WHA-TV studio in the Communication Arts Building on the Madison

campus of the University of Wisconsin. At WHA-TV, this signal can and has been put on the air over the Wisconsin State Broadcasting Network.

Although encoding the RGB Standard McIDAS Video Signal to the Color Composite Standard poses no technical problems, many practical operational and aesthetic problems arise which are due primarily to bandwidth limitations and color encoding technique limitations inherent to the Color Composite format. For instance, the Cursor contains very high resolution components in its vertical boundaries because the boundaries are one line and one pixel wide. This poses no display problems for the Conrac Video monitor, but the Color Composite format strips away these high frequencies and displays a cursor with good horizontal boundaries and very poor vertical boundaries.

Color problems are even more severe. First of all the Chromance bandwidth of the Composite Video Format is very much reduced from even its Luminance bandwidth. This means that even when a vertical edge, as generated on the McIDAS System, is made wide enough to appear as a good vertical edge in the composite Video Format, the color associated with that edge will be "splashed" or may even be wrong. Even when resolution limitations are compensated for, the phase encoding techniques used to carry the Chrominance information in the Composite Video Format will produce "fringing" at color boundaries if the boundaries are too sharp or if certain colors are placed side by side.

By using the RGB Standard for the images generated by the McIDAS System and viewed by the McIDAS operator, a high resolution color display is produced which shows exactly what the user wants to see with a minimum number of compromises made for practical reasons.

McIDAS COMPUTER SUBSYSTEM

GENERAL THEORY OF OPERATION
        Refer to FIGURE 2; McIDAS System Detailed Functional Block Diagram
        and FIGURE 15; McIDAS Computer Subsystem Functional Block Diagram.

The McIDAS Computer Subsystem is a Datacraft (Harris) 6024/5 Computer

installation with a modest set of standard peripherals, as can be seen in

FIGURE 2; McIDAS System Detailed Functional Block Diagram and FIGURE 15;

McIDAS Computer Subsystem Functional Block Diagram.

The 6024/5 Computer uses a 24 bit word and has 56K of 1 µsec core. Its

input/output (I/O) structure is flexible and includes direct memory access

channels(IOC Channel) in either 8 bit or 24 bit sizes. Each channel can

have up to 16 separate I/O devices on its bus, each containing a Unit

Interface. The Unit Interface then, is the remotest control point of the

6024/5 and performs the actual data and control transfer between the

Computer and the peripheral. It is at this Unit Interface level that the

McIDAS Computer Subsystem ties into the McIDAS Archive Subsystem and the

McIDAS Video Chain.

Details of the I/O Structure of the Datacraft (Harris) 6024/5 Computer

and the Unit Interface instruction set is available in the Datacraft (Harris)

publication entitled Reference Manual - DC 6024/5 Computer Input/Output

Interface (Publication No. RM 61396-00P). Also, a general organizational

description and the basic instruction set is available in the Datacraft (Harris)

publication entitled Reference Manual, DC 6024/5 Computer System (Publication

No. RM 61397-00).

Two other Datacraft (Harris) publications are useful,especially for

maintenance purposes: Technical Manual, DC 6024/5 Computer System (Publication

No. TM 61388-00); and Drawing Manual, DC 602415 Computer System (Publication

No. DM 61390-00A.

Maintenance of the 6024/5 Computer and peripherals is generally done by the

local Datacraft (Harris) representative. However, the McIDAS Maintenance facility does have standard diagnostic sets for the main frame, the memory, the digital disks, and the 9 track magnetic tape unit. Also, service manuals are provided for all peripherals procured from sources outside of SSEC.

SMS

28 mbit
PRIMARY
LINK

CDA
STATION

1.687 GHz
RETRANSMISSION
LINK

ARCHIVE

McIDAS
ARCHIVE
SYSTEM

DIRECT

McIDAS
COMPUTER
SUBSYSTEM

IMAGE
DATA
CONTROL

ANALYSIS
RESULTS

OPERATOR
SELECTION
INFORMATION

McIDAS
VIDEO
CHAIN

RGB STANDARD
COLOR TV
VIDEO

OPERATORS
CONSOLE

FIGURE 1 ; McIDAS SYSTEM FUNCTIONAL
BLOCK DIAGRAM.

1.687 GHz RETRANSMISSION LINK

DUS ANTENNA SUBSYSTEM

ARCHIVE SUBSYSTEM

ARCHIVE

MSU SUBSYSTEM

REAL TIME

SERIAL DIGITAL DATA
1.74 MBIT VISIBLE
0.52 MBIT IR
MODE A @ 100 rpm

McIDAS ARCHIVE SUBSYSTEM

DIGITAL SMS DATA

SYNCHRONOUS MODEM

DATA INGESTION

TELETYPE

CARD READER

LINE PRINTER

⟹ DIGITAL DATA

→ ANALOG DATA

INTERFACE

IMAGE DATA & CONTROL

DATACRAFT 6024/5 COMPUTER

DIGITAL DISK

DIGITAL DISK

MAG TAPE

FAST STORAGE

CURSOR GENERATOR

McIDAS COMPUTER SUBSYSTEM

OPERATOR SELECTION & CONTROL INFO

ANALYSIS RESULTS

VIDEO DISK SUBSYSTEM

ENHANCEMENT SUBSYSTEM

McIDAS VIDEO CHAIN

RGB STANDARD COLOR TV MONITOR

CRT TERMINAL DISPLAY

JOYSTICKS

CRT TERMINAL KEYBOARD

OPERATORS CONSOLE

FIGURE 2; McIDAS SYSTEM DETAILED FUNCTIONAL BLOCK DIAGRAM

FIGURE 3
McIDAS ARCHIVE SYSTEM DETAILED
FUNCTIONAL BLOCK DIAGRAM

DIRECTION OF TAPE TRAVEL

17.5625" (43.7 cm)

LOCATION OF AUDIO 2
RECORDING HEAD RELATIVE
TO START OF VIDEO ▷

13.75" (34.2 cm)

LOCATION OF
CONTROL TRACK AND AUDIO 1
RECORDING HEAD
RELATIVE TO
START OF VIDEO ▷

12.011 (30.6 cm)
TAPE TRAVEL FOR 1 VIDEO FIELD

1" Tape (2.54 cm)

12.053 (30.7 cm) TRUE LENGTH
OF VIDEO TRACK FOR ONE VIDEO FIELD

OXIDE SIDE

START OF VIDEO TRACK

A

Edge of tape

25° *

0.100"
(2.5 mm)

Audio 1

39 MIL (1.0 mm)

B

6 MIL (0.190 mm)
Horizontal sync
Pulse line-up

Video Track
Guard band

4° 45'

3.5 MIL (0.094 mm)

C

25°
*

0.115
(3.45 mm)

39 MIL
(1.0 mm)

Control
Track

0.100"
(2.5 mm)

Audio 2 (Cue Track)

0.003" (0.1 mm)
13 MIL (0.3 mm)
Edge of tape

✱ ANGLE OF RECORDING HEAD GAP

NOTE:
Dimensions in inches for 60 Hz recorders.
Dimensions in parenthesis (metric) for 50 Hz recorders.

FIGURE 4.; SLANT TRACK VIDEO RECORDER
TAPE FORMAT

FIGURE 5; Documentation Data Format

First Record

   All 192 bits are a recurrent 0101 pattern.

Second Record

Bits 1 thru 7	Seven bit straight binary number which represents how many Frame Code (zero to one) transitions have been decoded by the DUS/Archive Interface since the counter was last reset. Reset is manual via keyed switch on the front panel of the Archive Bay labeled "New Day Reset".
Bits 8 thru 24	Seventeen bit straight binary number which represents how many tracks have been recorded with actual data since the counter was last reset. Reset is manual via keyed switch on the front panel of the Archive Bay labeled "New Tape Reset".
Bits 25 thru 48	Twenty-four bits containing a "1" or a "0" depending upon the setting of 24 switches on the front panel of the Archive Bay.
Bits 49 thru 72	Twenty-four bits of "1"'s. This was designated to encode time from a time code generator which was to be included in the Documentation Generator but which was never implemented.
Bits 73 thru 93	Twenty bits of "1"'s. Unused locations.
Bits 93 thru 96	Four bits known as the Sector Identifier which indicate which sector is presently being received by the DUS/ Archive Interface.

                      0000 = IR
                      0001 = visible 1   0101 = visible 5
                      0010 = visible 2   0110 = visible 6
                      0011 = visible 3   0111 = visible 7
                      0100 = visible 4   1000 = visible 8

                      Note: within the DUS/Archive Interface, IR forces
                      state 0000 and the visible states are generated by
                      counting the Sector Code Signal.

Bits 97 thru 192 Unused. All "0"'s.

LOAD A
VISIBLE X

LOAD B
VISIBLE X+1

LOAD C
VISIBLE X+2

|←— 15,800 WORDS —→| |←— 1,672 WORDS
                          INITAL SYNC
                          (PN SEQUENCE)

|←——— 54.22 msec ———→|

|←——— 59.96 msec ———→|

A THIRD
BUFFER IS NEEDED

WORST CASE
JUST MISSED

SKIPPED
TRACK

16.67
msec

UNLOAD
A

|←——— 50 msec ———→|
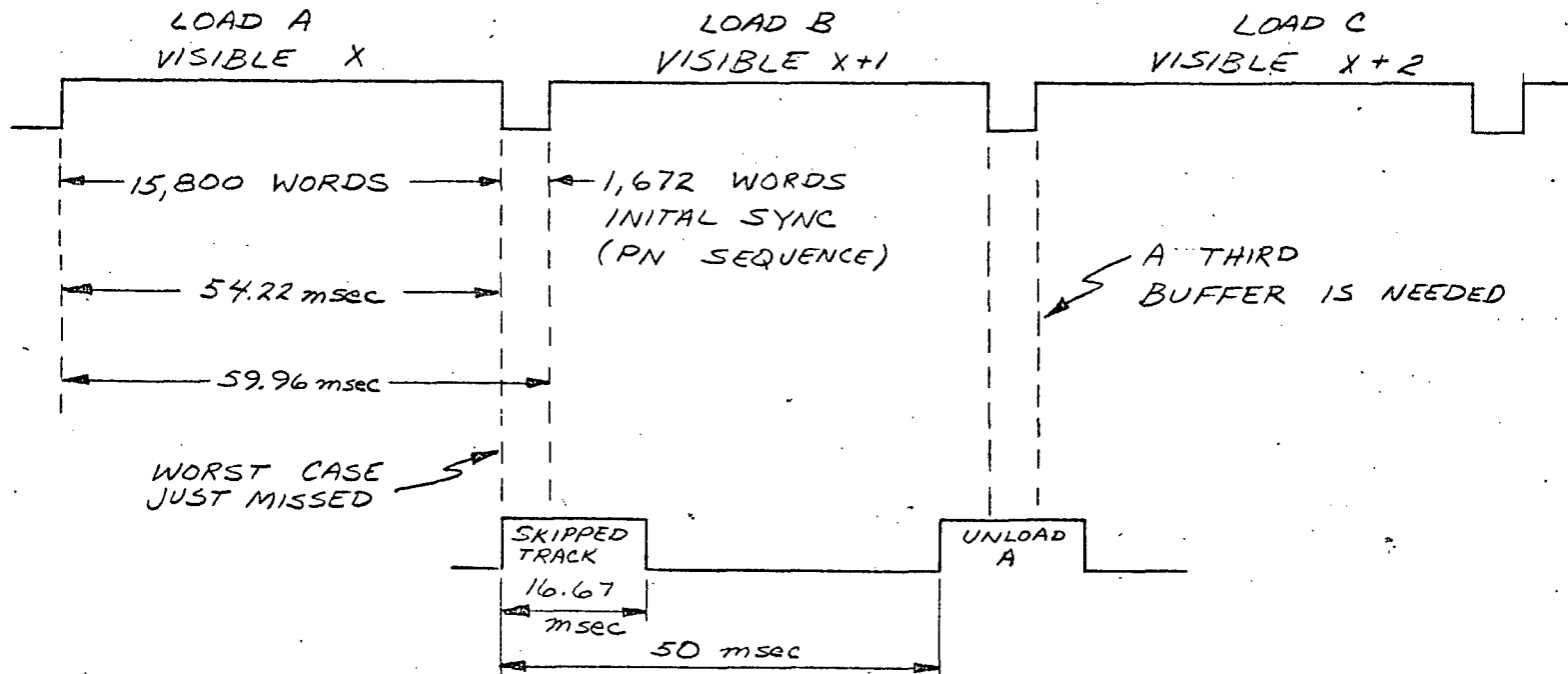
@ 100 rpm   VISIBLE BIT RATE = 1.747 m BITS

=> 0.572 μ sec PERIOD

15,800 × 6 × .572 = 54.22 msec

1,672 × 6 × .572 = $\underline{5.74}$ msec

59.96 msec

FIGURE 6 ; DATA BUFFER LOAD/UNLOAD SEQUENCE

DATA INPUTS

ROW ENABLES

8

2

1

MK 4008-9

1

2

3

16

ROW ADDRESS, COLUMN ADDRESS
& R/W ARE ROUTED TO ALL CHIPS.

SENSE AMP.

SENSE AMP.

DATA OUTPUTS

FIGURE 7;   DATA BUFFER FUNCTIONAL LAYOUT

CLOCK

÷16 CNTR STATE | 13 | 14 | 15 | 16→0 | 1 | 2 |

14 PIN 11   50 nsec

21 PIN 4   50 nsec

22 PIN 6

20 PIN 10
PARALLEL LOAD (READ)

21 PIN 5   600 nsec

5 PIN 13 ($\overline{R/W}$)   500 nsec

ROW ADDRESS STATE   X   X + 1

22 PIN 9   H => NO   FOR OTHER THAN LOAD (UNLOAD & STANDBY);—
            CHIPS ENABLED $\overline{R/W}$ => REFRESH

22 PIN 9   L => APPROPRIATE
            CHIPS ENABLED   FOR LOAD ONLY;—$\overline{R/W}$ => WRITE
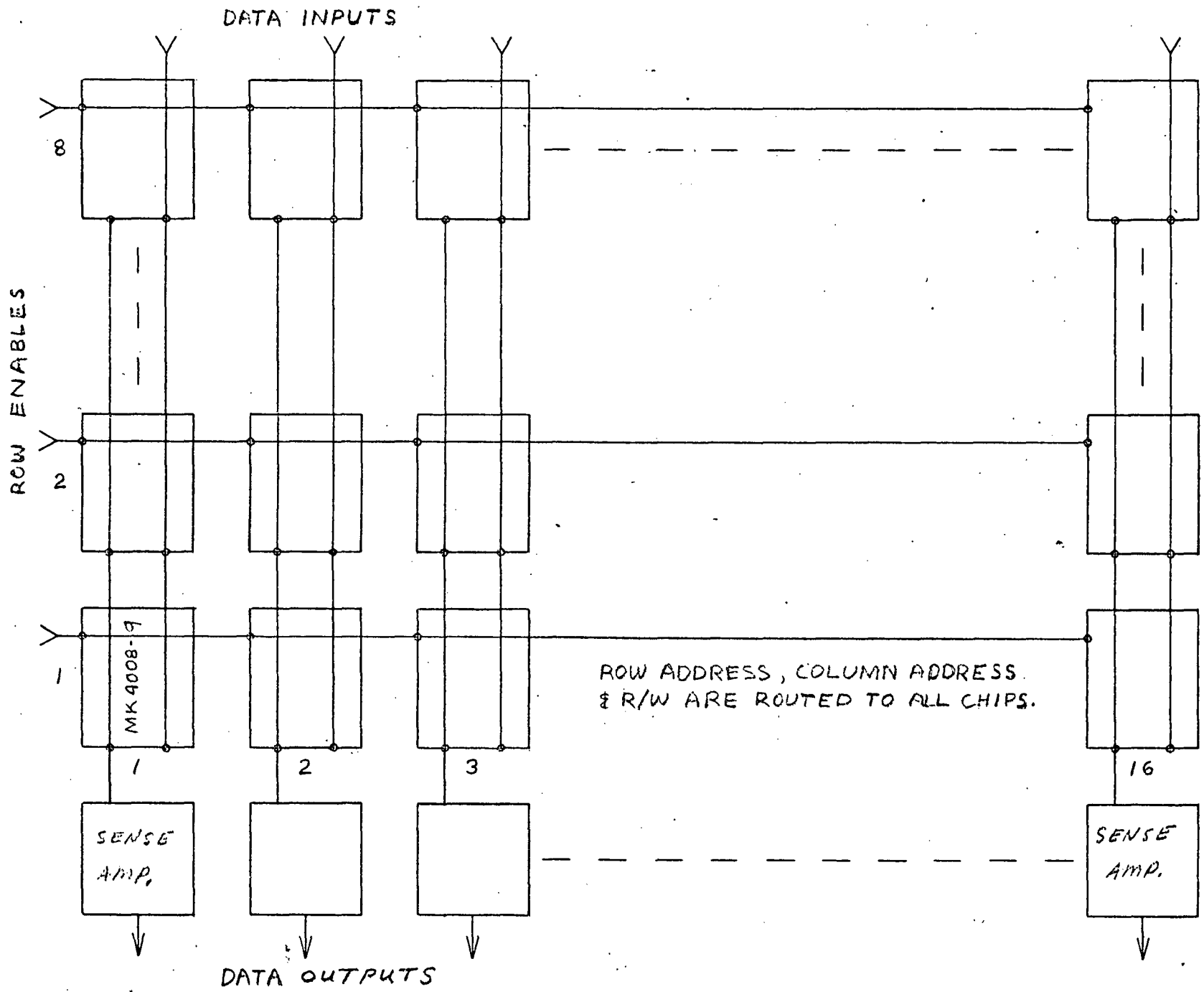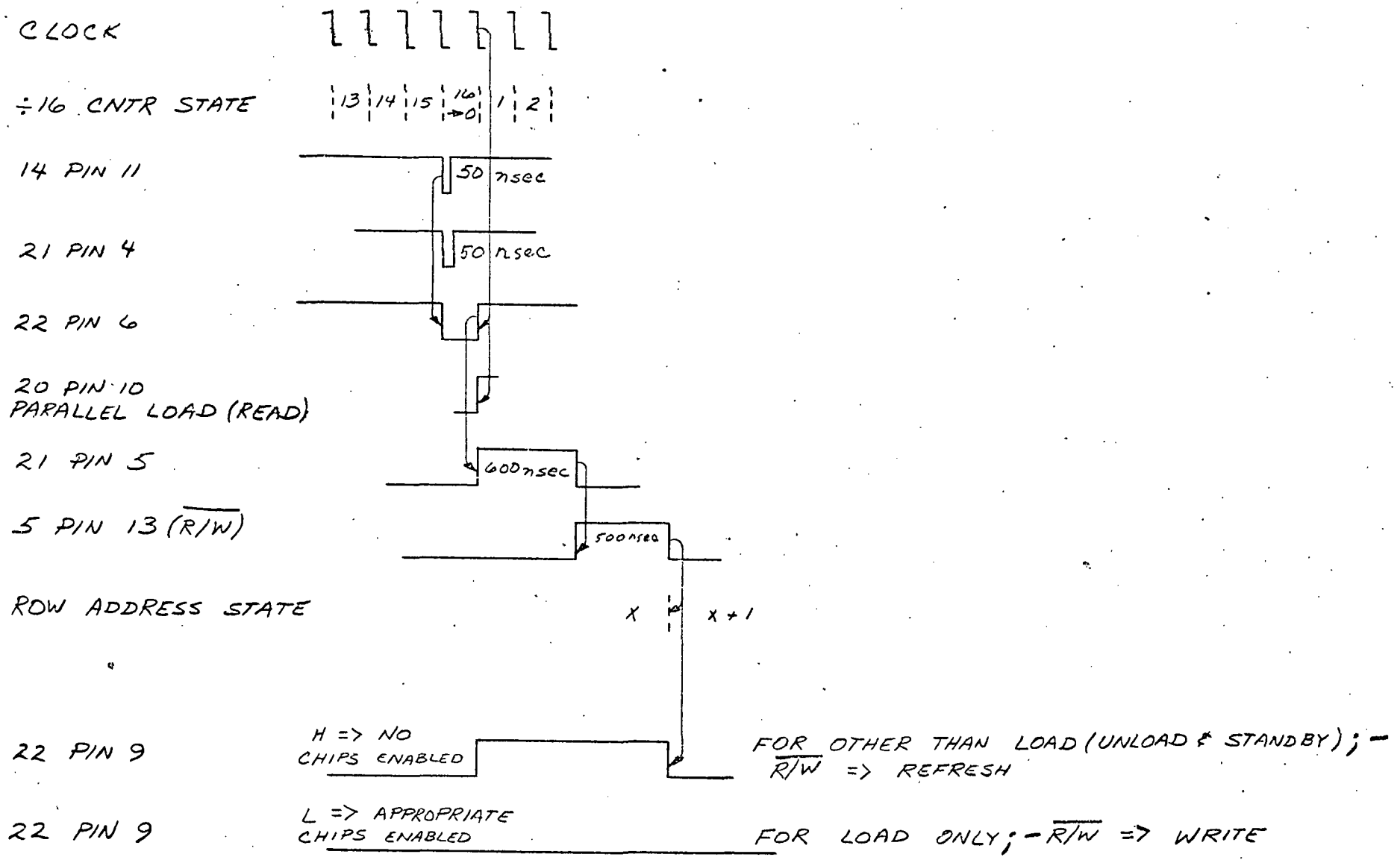
FIGURE 8a; DATA BUFFER TIMING
READ-WRITE/REFRESH CYCLE

START SLANT

1 μsec

START DOCUMENT

DOCUMENT COMPLETED.

250 nsec

UNLOAD ENABLE

UNLOAD (A, B, or C)

SLANT TRACK
DATA CLOCK

UNLOAD CLOCK (A, B, or C)
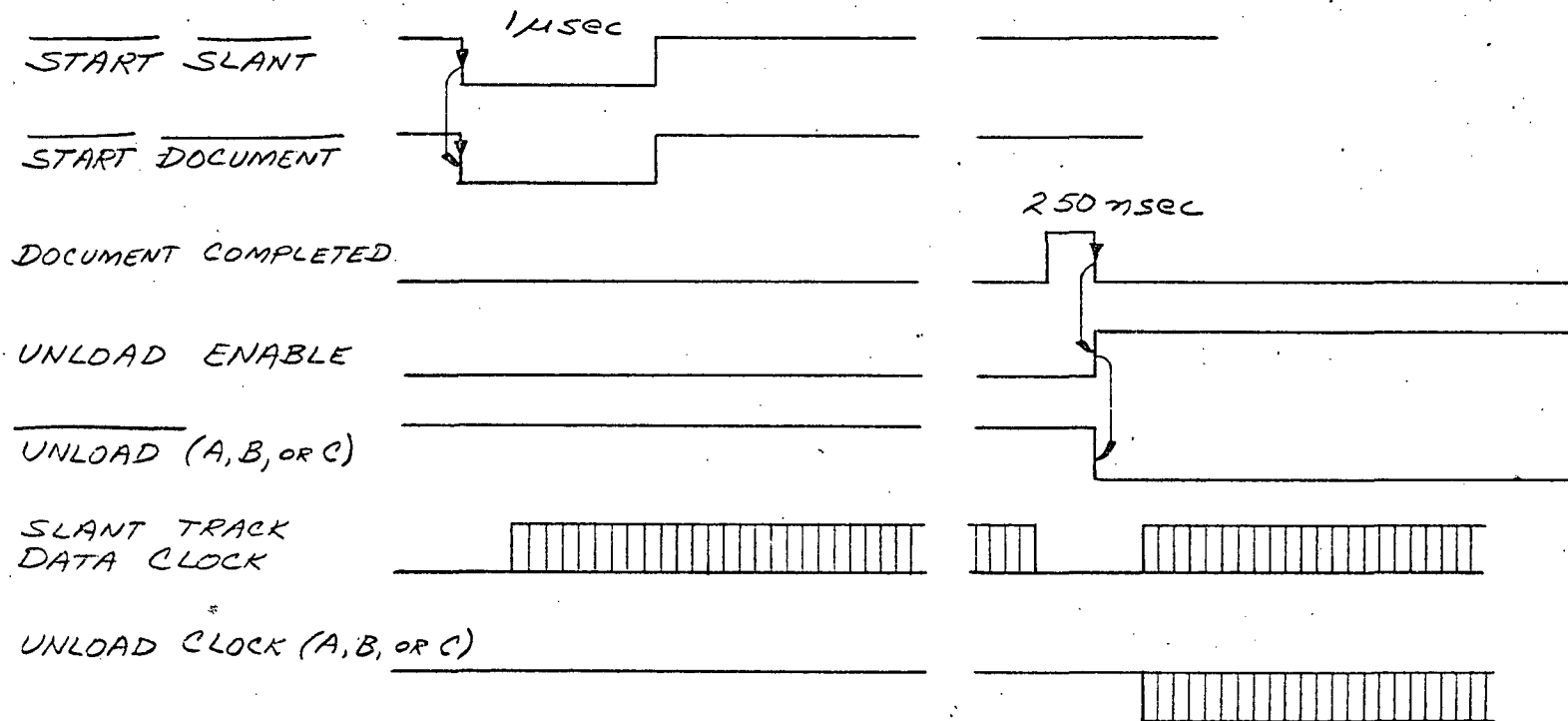
FIGURE 8b ; DATA BUFFER TIMING
DOCUMENTATION VS DATA

590 nsec

DATA CLOCK

60 nsec

SECTOR CLOCK

LOAD ENABLE
(3 PIN 9)

LOAD CLOCK

$\overline{LOAD}$ (A, B, OR C)

(A)

16 X .6 μsec = 9.6 μsec
ADDRESS CLOCK
PERIOD

$\overline{LOAD}$

150 nsec

MONO (A)
(35 PIN 4)

50 nsec

MONO
(35 PIN 12)

REFRESH DISABLE

REFRESH CLOCK

GATED REFRESH

MONO
(5 PIN 12)

3 μsec

ADDRESS RESET

÷ 16
COUNTER RESET
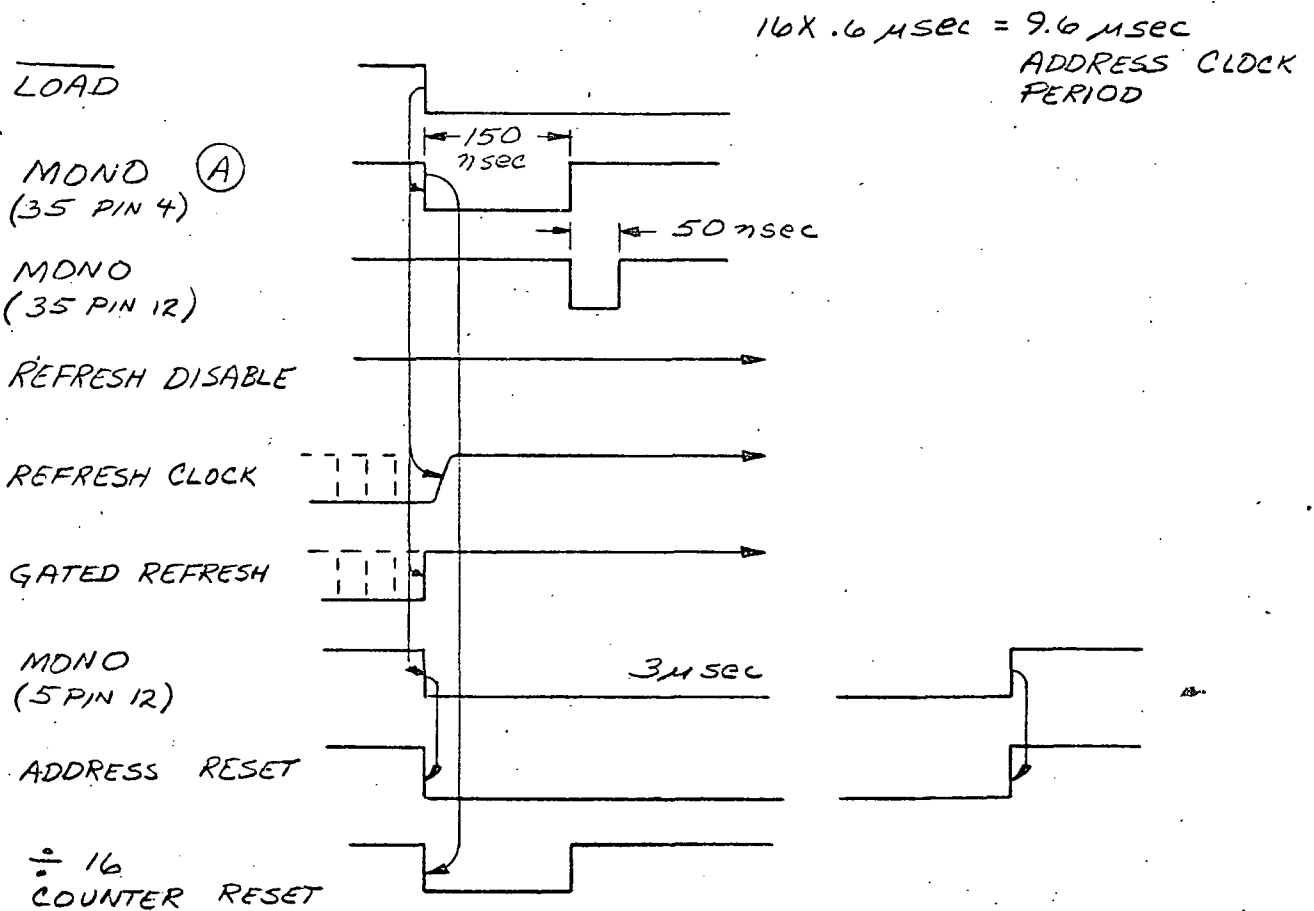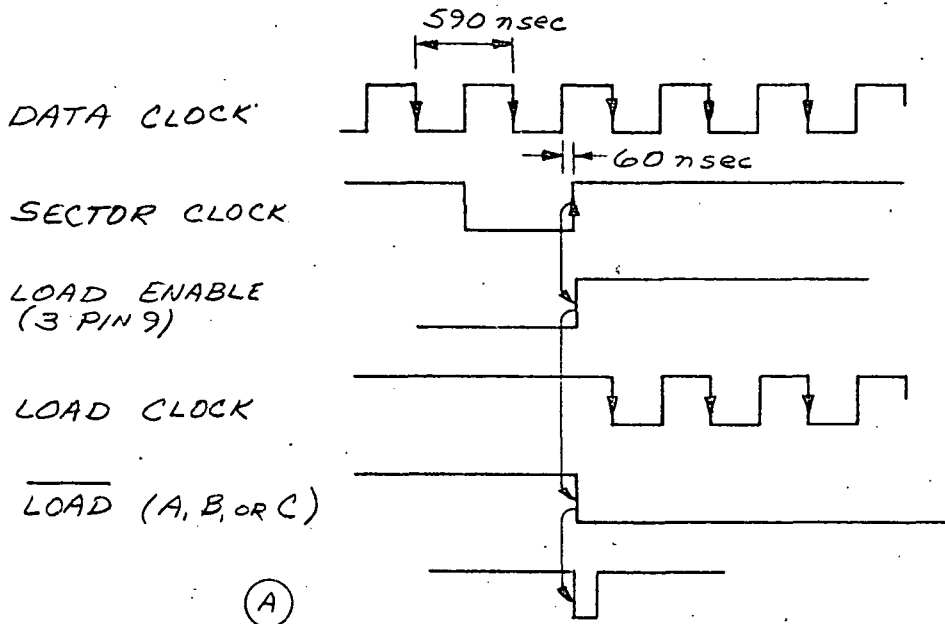
FIGURE 8c ; DATA BUFFER TIMING
LOAD TIMING

START DOCUM.

1 μs.

REFRESH DISABLE

≈2.7μs.

DOCUM. COMPLETED

250ns.

REFRESH ENABLE LEADING EDGE
RESETS ADDRESS TO 0.

DELAY ÷16 COUNTER RESET (50ns.)
→ 11 TO SERIAL CONVERTER LOAD
PULSE DOES NOT ADVANCE COUNTER.
ie. USE 50 ns. PULSE TO RESET ÷16
COUNTER.

DOCUM. COMPLETED

250ns.

REFRESH DISABLE

UNLOAD

35 PIN 4 MONO (A)

150ns.

35 PIN 12 MONO

50ns.

REFRESH 3 PIN 12

CLAMP
ENABLE

IF NOT CLAMPED BY
UNLOAD

GATED REFRESH

LOADS FIRST 16 BIT WORD INTO
PARALLEL TO SERIAL CONVERTER.

UNLOAD CLOCK

COMPOSITE
UNLOAD CLOCK

ADDRESS RESET

MUST HOLD COUNTER RESET DURING THIS
ACTIVE EDGE.

÷16 COUNTER RESET

FIGURE 8d ; DATA BUFFER TIMING

UNLOAD TIMING

BITS   1 1 0 0 0 1 0 1 1 0 1 SYNC 0 1 0

RECORDED
WAVEFORM

BIT INTERVAL OF 140 nsec
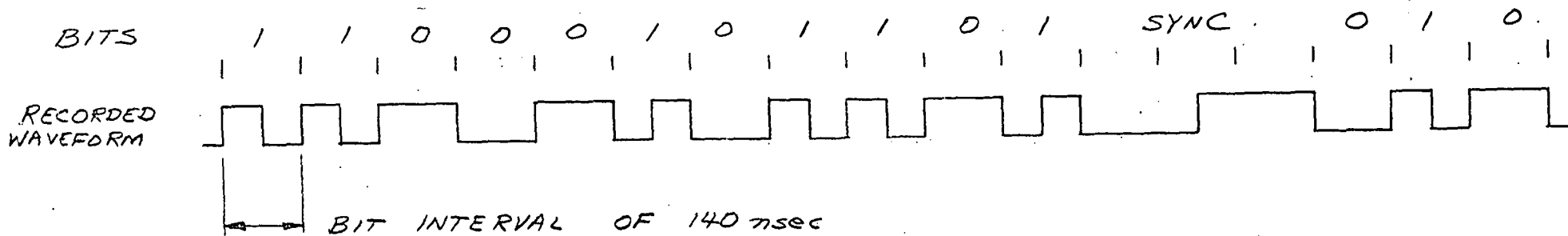
A LOGICAL "ONE" IS ENCODED AS ONE COMPLETE
CYCLE OF A SQUARE WAVE WHOSE PERIOD IS
140 nsec. A LOGICAL "ZERO" IS ENCODED AS
ONE HALF CYCLE OF A SQUARE WAVE WHOSE
PERIOD IS 280 nsec. A FURTHER CONDITION IS
THAT A TRANSITION MUST ALWAYS OCCUR
BETWEEN 140 nsec BIT INTERVALS.

FIGURE 9; BIPHASE ENCODING FORMAT

Beginning of track

Multiple Sync Word	24	Bit	Intervals
Record 1 Fill Pattern	192	"	"
Sync Word	3	"	"
Record 2 Documentation	192	"	"
Sync Word	3	"	"
Record 3 Data (Documentation)	192	"	"
Sync Word	3	"	"
Record 4 Data (Documentation)	192	"	"
Sync Word	3	"	"

For IR Only.
Data Documentation Ends
with record 18 for visible
Mode A.

Record 8 Data (Documentation)	192	"	"
Sync Word	3	"	"
Record 9 Data	192	"	"
Sync Word	3	"	"
Record 548 Data	192	"	"
Multiple Sync Word	24	"	"

End of Track

FIGURE 10; Archive Track Format
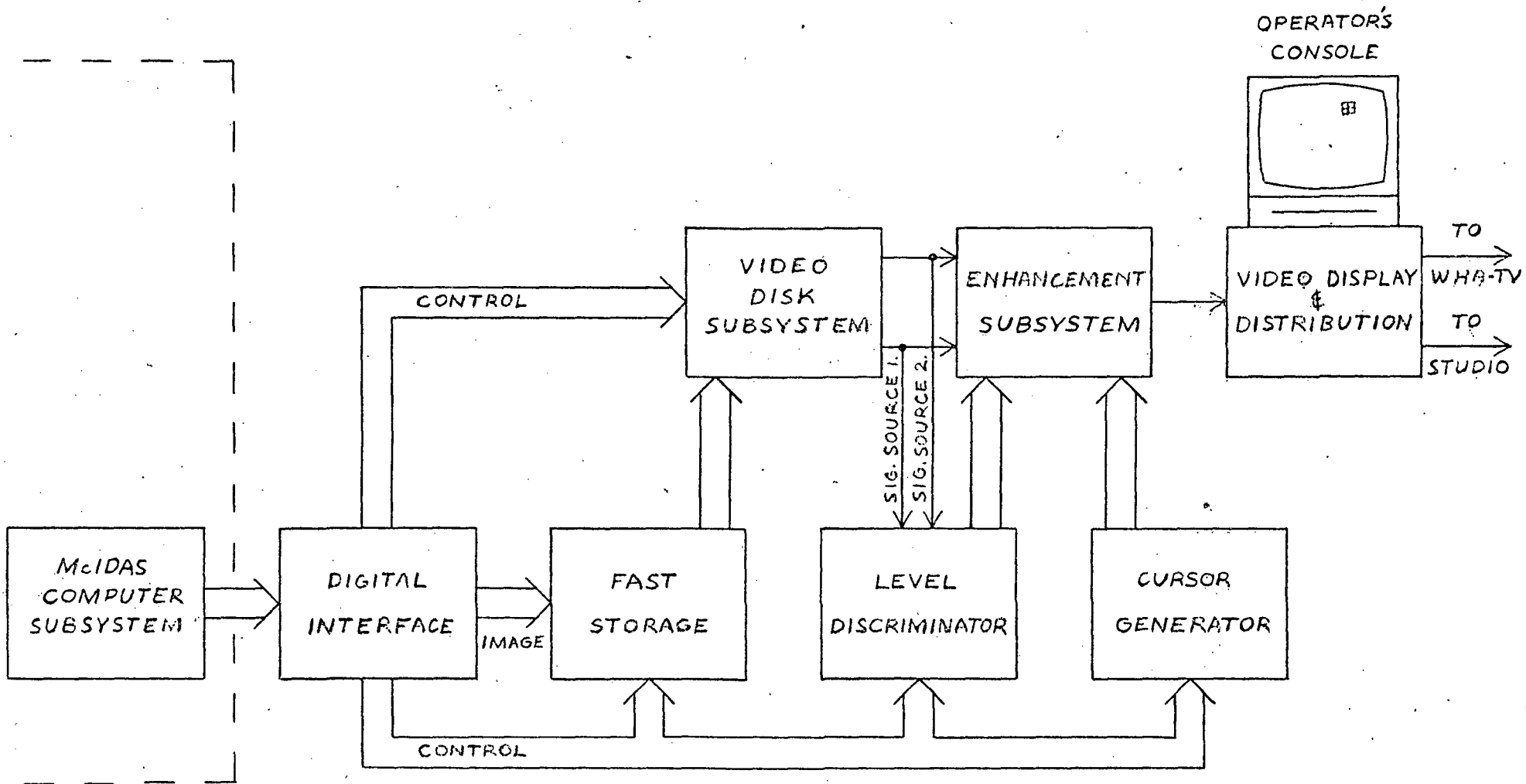
FIGURE 11; McIDAS VIDEO CHAIN
FUNCTIONAL BLOCK DIAGRAM

FIGURE 12
MIDAS VIDEO CHAIN
DETAILED FUNCTIONAL BLOCK DIAGRAM

FOLDOUT FRAME 1

FOLDOUT FRAME 2

FOLDOUT FRAME 3

CRYSTAL OSCIL. ACTIVE
EDGES (74S04A PIN 8) ||| ||||||||||||||||||||| |||||||||||||||| FREQ. = 4 x PIXEL CLOCK

HORIZONTAL DRIVE ≈ 6µsec

PIXEL CLOCK STATE RESET | 1 | 2 | 3 | 4 | | 699 | RESET

63.5µsec
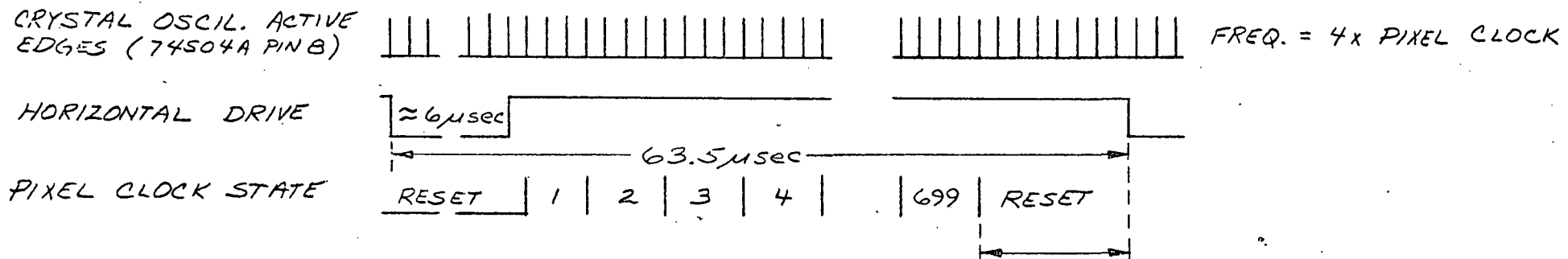
THIS INTERVAL DEPENDS ON THE
EXACT FREQUENCY OF THE CRYSTAL
OSCILLATOR & THE EXACT PHASE AT
THE LAGGING EDGE OF THE HORIZONTAL
DRIVE. APPROX. 1 µsec

PIXEL FREQUENCY IS SUCH THAT 700 CYCLES OCCUR IN
63.5 - 6 -1 = 56.5µsec => 12.39 MHz

FIGURE 13; McIDAS VIDEO CHAIN TIMING FORMAT
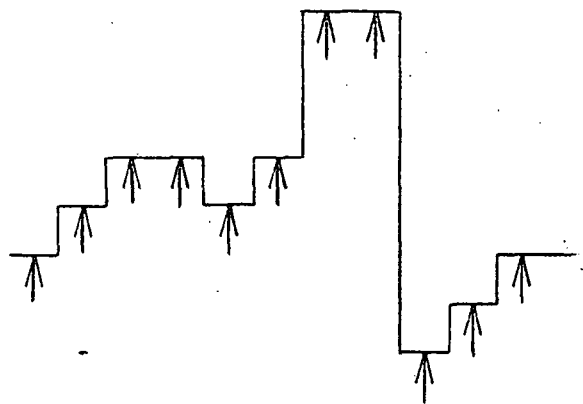
SYNCHRONOUS RESAMPLING
WHEN PHASED PROPERLY,
RECONSTRUCTS ORIGINAL
WAVEFORM W/O GLITCHES.
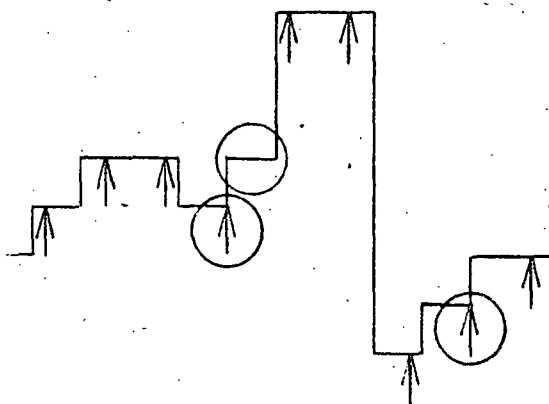
ASYNCHRONOUS RESAMPLING
WILL CAUSE GLITCHES AT
THE BEAT FREQUENCY.
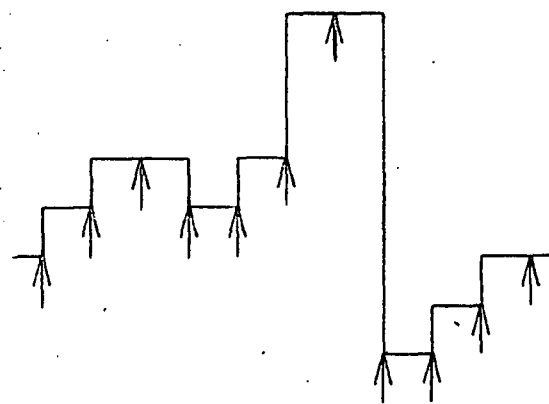
SYNCHRONOUS RESAMPLING
IMPROPERLY PHASED CAN
CAUSE ALMOST ALL SAMPLES
TO BE GLITCHED.
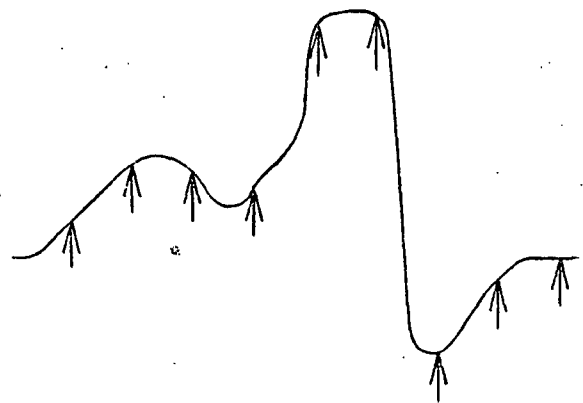
ASYNCHRONOUS RESAMPLING
ON BANDLIMITED DATA WILL
NOT CAUSE NOTICEABLE
GLITCHES.
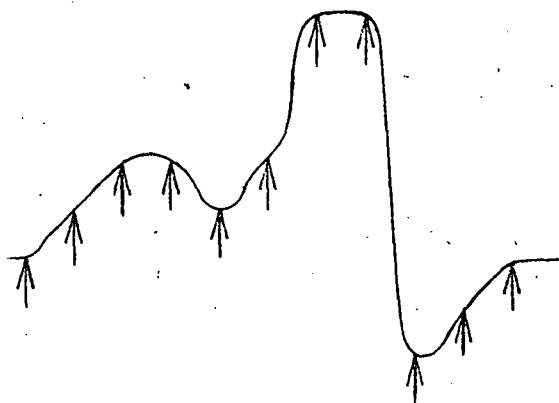
THE ENHANCEMENT SUB-
SYSTEM USES SYNCHRONOUS
RESAMPLING ON BAND-
LIMITED DATA,

FIGURE 14; RESAMPLING COMPARISONS
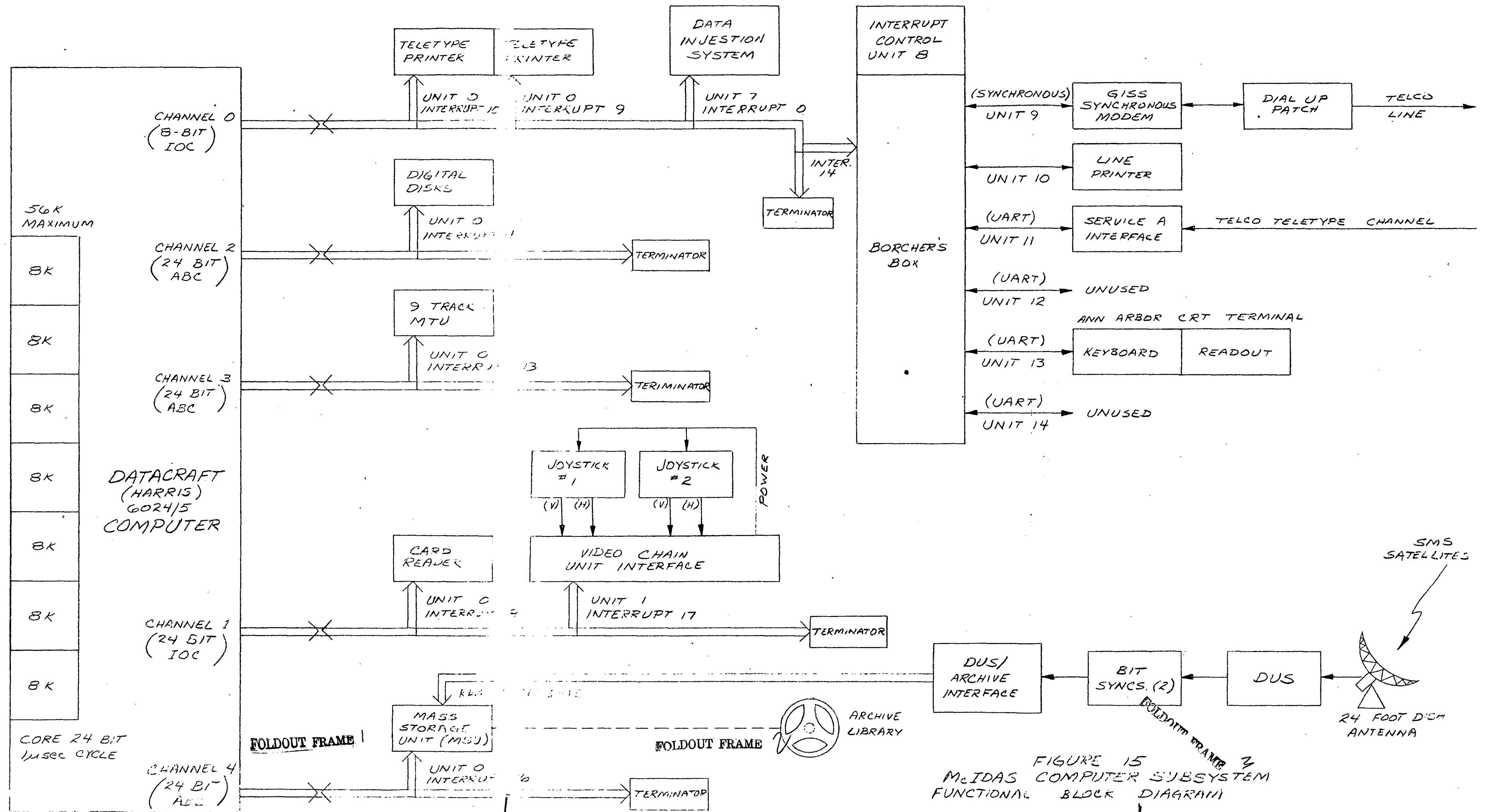
FIGURE 15
McIDAS COMPUTER SUBSYSTEM
FUNCTIONAL BLOCK DIAGRAM

APPENDIX A

SMS VISSR DATA FORMAT

SMS VISSR Data-Format

The DUS Receiver accepts the digital VISSR data in any one of four different data formats. In each of these formats two separate images are received. In three formats (Modes A, B, and C) an image from visible spectrum sensors is time multiplexed with an image from an infrared (IR) sensor. In the fourth format (Mode D), the same IR information is received in two different resolutions.

The images arrive at the DUS Receiver in units of information derived from a single scan (i.e., revolution) of the spacecraft. A series of 1821 scans is required to generate a complete image. Since the visible image is obtained from eight parallel sensors, up to eight lines of a visible image can be received during a single scan period. The IR sensor generates only a single line of an image for each spin of the spacecraft.

The details of these formats are shown for a single scan in Table A-1. Table A-1 shows how data from a single scan is time multiplexed. All time intervals are dependent on satellite spin rate and unless otherwise noted are given for the 100 RPM rate. In all modes the first time block has a duration of 45 milliseconds and is indicated by the notation EV. This period contains the raw sensor data (at a 28-megabit rate) which is received only at the CDA station and is treated as noise at the DUS Receiver.

The next block (again in all modes) contains a single line of IR data. Each word (sample) of this line of IR data contains nine bits. Eight bits represent the intensity value. The ninth bit contains the grid information (a "one" indicates that a user desiring grids should replace this sample with a grid point). The interval between samples along a line at 100 RPM at the satellite subpoint nominally corresponds to a two-mile displacement. The corresponding displacement line-to-line is four miles. Hence, the resolution of the IR is denoted as 4 x 2 miles.

In Mode A, eight lines of visible data are contained in each scan. The resolution is 1/2 x 1/2 mile. In Mode B there are four 1 x 1 mile resolution visible lines per scan and in Mode C there is only one 4 x 4 resolution visible line per scan. Mode D differs from Mode C only in that there is no visible data but instead the IR data is repeated in a 4 x 4 mile resolution format.

No grid information is contained in the Modes A and B visible data. In Modes C and D (4 x 4 data only) the grids are implanted (i.e., sensor data is replaced with appropriate grid data).

Table A-2 gives characteristics of the data contained within each line.

Tables A-3 through A-6 show the definitions of the documentation words (these definitions are not completely self-explanatory but should be sufficient for sectorizer bid preparation).

VISSR   DATA   FORMATS

MODE A

EV	IR	V1	V2	V3	V4	V5	V6	V7	V8
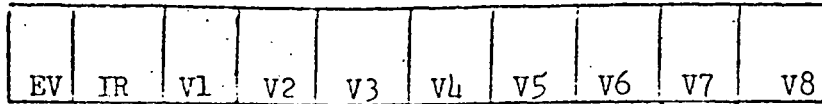
Resolution (VXH)	4 x 2 miles	½ x ½ miles
Time Interval	75 msec	60 msec
bits/sample	9 bits	6 bits
bit rate	524,160 bits/sec	1,747,200 bits/sec

MODE B

EV	IR	V1	V2	V3	V4
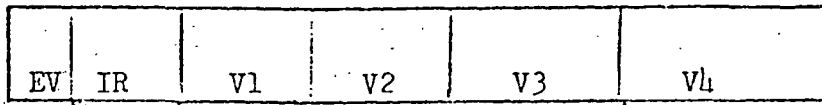
Resolution (VXH)	4 x 2 miles	1 x 1 miles
Time Interval	75 msec	120 msec
bits/sample	9 bits	6 bits
bit rate	524,160 bits/sec	436,800 bits/sec

MODE C

EV	IR	V1

Resolution (VXH)	4 x 2 miles	4 x 4 miles
Time Interval	75 msec	480 msec
bits/sample	9 bits	8 bits (implanted grids)
bit rate	524,160 bits/sec	33,280 bits/sec

MODE D
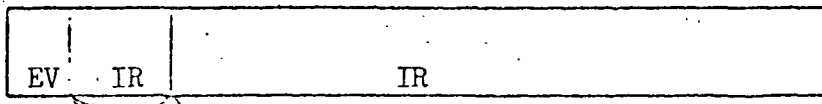
EV	IR	IR

Resolution (VXH)	4 x 2 miles	4 x 4 miles
Time Interval	75 msec	480 msec
bits/sample	9 bits	8 bits (implanted grids)
bit rate	524,160 bits/sec	33,280 bits/sec

NOTE: Bit rates and time intervals are dependent on spacecraft
spin rate. Values shown are for a spin rate of 100 RPM.
Actual spin rate may vary from 50 to 110 RPM.

TABLE A-2 VISSR DATA CHARACTERISTICS

		4 x 2 IR	Mode A Visible	Mode B Visible	Mode C Visible	Mode D 4 x 4 IR
Bits/word		9	6	6	8	8
Words per Line	Initial Sync	418	1,672	836	69	69
	Documentation	128	512	256	16	16
	Video Data	3,822	15,288	7,644	1,911	1,911
	Total	4,368	17,472	8,736	1,996	1,996
Bit rate 100 RPM (bits per second)		5.2416×10^5	1.7472×10^6	4.368×10^5	3.328×10^4	3.328×10^4
Bit rate 110 RPM (bits per second)		5.7658×10^5	1.8219×10^6	4.805×10^5	3.661×10^4	3.661×10^4
Line time interval 100 RPM (milliseconds)		75	60	120	479.8	479.8
Line time interval 110 RPM (milliseconds)		68.1	54.5	109	436.1	436.1
Bits per Sector		39,312	104,832	52,416	15,968	15,968

Data	Position
Retrace (Note 1)	word 1

ONE indicates scanner retrace

Spacecraft Name	word 2

Scan Mode	word 3

```
MSB           LSB
0 0 1 1 0 0 1 0 0   A
0 0 1 0 1 1 0 0 1   B
0 1 0 1 1 0 0 1 0   C
0 1 0 0 0 1 1 1 1   D
```

Frame code (Note 1)	word 4

ONE indicates picture transmission

Change code (Note 1)	word 5

ONE indicates first line of picture if frame

code is ONE or last line plus one of

picture if frame code is ZERO.

Step code (Note 1)	word 6

ONE indicates normal line transmission;

ZERO indicates that this line is not to be

used to expose film and facsimile recorder

line is not to be incremented (stepped).

Line Delay	word 7

This number (1-8) denotes the delay to be

introduced by the user; expressed in bit

intervals.

IR Selection	word 8

```
MSB           LSB
0 0 0 0 0 0 0 0 1   IR1
0 0 0 0 0 0 0 1 0   IR2
0 0 0 0 0 0 1 0 0   AVG
```

Gray Scale Status (Note 1)	word 9

ONE indicates gray scale information
retransmission.

Data	Position
Direct Transmission Mode (Note 1)	word 10

    ONE indicates 28 Mb/sec; ZERO indicates
    14 Mb/sec

Scan Count

    BCD value split into 2 characters/word

2 most significant BCD characters	word 11
2 least significant BCD characters	word 12
Scan Mode	word 13

    MSB   LSB

    0 0 0 0 0 0 0 0 1   A
    0 0 0 0 0 0 0 1 0   B
    0 0 0 0 0 0 1 0 0   C
    0 0 0 0 0 1 0 0 0   D

Beta Count

    MSB   LSB

0 8 MSB	word 14
0 8 BITS	word 15
0 8 LSB	word 16
Grid/No Grid (Note 1)	word 17

    ZERO indicates no grid info

Sync Error

    MSB   LSB

0 8 MSB	word 18
0 7 LSB 0	word 19

Bit Error Count

    MSB   LSB

0 8 MSB	word 20
0 5 LSB 0 0 0	word 21
Setup Error (Note 1)	

    ONE indicates setup error   word 22

Data		Position
Computer Error Messages		
LSB Transfer Reject Errors	- Time Input	word 23
	- Execute Output	
	- NESS Output	
	- S/C Output	
	- S/C Input	
High Rate I/O Errors	- NESS Transfer	
	- Output Transfer	
MSB	- Input Transfer	
LSB Interrupt Sequence Error	- NESS Output	word 24
	- 4 x 4 Output (C/D only)	
	- S/C Input	
	- NESS Pre Sync	
	- 4 x 2 Output	
Miscellaneous Errors	- Undefined	
	- Mag Tape Output	
MSB	- Beta Output	
Undefined		word 25
Undefined		word 26
Time - BCD		
Year - 2 MSD		word 27
Year - 2 LSD		word 28
Day of Year - 2 MSD		word 29
Day of Year - 2 LSD		word 30
Hour		word 31
Minute		word 32
Second		word 33
Millisecond *10		word 34

Data .   **Position**

Black Enable (Note 1)   word 35

      ONE indicates annotation transmission

Mode C - Calibrate   word 36

      ONE (Note 1) indicates that C-Cal is not

      used; otherwise: MSB

V1	0 0 0 0 0 0 0 1
V2	0 0 0 0 0 0 1 0
V3	0 0 0 0 0 1 0 0
V4	0 0 0 0 1 0 0 0
V5	0 0 0 1 0 0 0 0
V6	0 0 1 0 0 0 0 0
V7	0 1 0 0 0 0 0 0
V8	1 0 0 0 0 0 0 0

Bit/Frame Sync Lock   word 37

    MSB   LSB

    0 0 0 0 0 0 0 1   Bit Lock
    0 0 0 0 0 0 1 0   Frame Lock
    0 0 0 0 0 1 0 0   Bit/Frequency Lock

Limited Scan Mode Indicator (Note 1)   word 38

      ONE indicates limited scan mode

Sample Control Mode   word 39

    (LSB)   IR-2PT

            IR-1PT

            IR-EAT

            Visible - 4 PT

            Visible - 2 PT

            Visible - 1 PT

            Visible - EAT

Data   Position

Visible Channel Connection   word 40

      (LSB)   V1

              V2

              V3   Coding for each channel

              V4   is as follows;

              V5   0 = normal; 1 = patched

              V6   input used

              V7

              V8

Scan Direction (Note 1)   word 41

     ONE indicates normal north-south

     direction (may not be used).

Bi-phase Modulator On/Off (Note 1)   word 42

Unused Location   word 43

PLL Error Light (Note 1)   word 44

     ONE indicates error condition

Test Data   word 45

     MSB   LSB

     0 0 0 0 0 0 0 0 0   Normal
     0 0 0 0 0 0 0 0 1   Local
     0 0 0 0 0 0 0 1 0   Remote
     0 0 0 0 0 0 1 0 0   Comp Gen IR

Data	Position
Data Randomization (Note 1)	word 46
ONE indicates ON	
Sun Pulse Select (Note 1)	word 47
ONE indicates Digital;	
ZERO indicates Analog	
NESS Mode Select	word 48

MSB LSB	
0 0 0 0 0 0 0 0	4 x 4 IR
0 0 0 0 0 0 0 1	MAX SV
0 0 0 0 0 0 1 0	4 x 2 IR

Data	Position
Limited Scan COMMAND ENCODER Enable	word 49
ONE indicates ON	
Digital Sun Pulse	word 50
8 LSB's contain the digital sun pulse	
Bit Error Light	
ONE indicates ON	word 51
Mean IR Difference	word 52
RMS IR Difference	word 53
Correction Table ID	words (54-55)
Unused Locations	words (56-125)

Note 1 - ZERO = 1_{16}
        ONE = FE_{16}

Table A-4 - Mode A Visible Documentation

Data	Position
Sector Code*	words 1-3

Uses three words; each word represents a
zero or a ONE. The most significant word is first
The sectors (i.e., visible lines) have numbers
000, 001, ----111.

Frame Code*	
ONE indicates picture transmission	word 4
Change Code*	Word 5

ONE indicates start of picture if frame code
is ONE or end of picture if frame code is Zero.

Step Code*	word 6

ONE indicates normal line transmission; ZERO
indicates that this line is not to be used to
expose film and facsimile recorder line is not
to be incremented (stepped).

Line Offset	word 7

This is a three bit word from the line offset logic
inserted into the last three bit positions with zeros
inserted into the first three positions (i.e., 000 xxx)

Unused	words 8-512

----

*All but the last bit in each code word are identical;
e.g., 0 0 0 0 0 1 (ZERO)
1 1 1 1 1 0 (ONE)

Table A-5 - Mode B Visible Documentation

Data	Position
Sector Code*	words 1-3

Uses three words; each word represents
a ZERO or a ONE. The most significant
word is first. The sectors (i.e., visible
lines) have numbers 000,001, 010 and 011.

Frame Code*	word 4

ONE indicates picture transmission

Change Code*	word 5

ONE indicates start of picture if frame is
ONE; end of picture if frame code is ZERO.

Step Code*	word 6

ONE indicates normal line transmission;
ZERO indicates that this line is not to be
used to expose film and facsimile recorder is not
to be incremented (stepped).

Line Offset	word 7

This is a three-bit word from the line offset
logic inserted into the last three-bit positions
with zeros inserted into the first three positions.
(i.e., 000XXX)

Unused	words 8-512

---

*All but the last bit in each word are
 identical; e.g., 000001 (ZERO)
               111110 (ONE)

Table A-6 - Modes C and D 4 x 4 Documentation

Data	Position
Unused	word 1
C/D Mode (Note 1)	word 2

ONE indicates mode C; ZERO indicates

mode D

C/D Data	word 3

In mode C, a ONE (Note 1) denotes that

C-Cal is not used. Otherwise only one of

the eight bits will be ONE denoting the

channel (V1-V8) used for C-Cal; V1 will

use the LSB, etc.

In mode D, this is the mean value of

1R1-1R2.

Frame code (Note 1)	word 4

ONE indicates picture transmission.

Change code (Note 1)	word 5

ONE indicates first line of picture if Frame

Code is ONE or last line plus one of picture

if Frame code is ZERO.

Step code (Note 1)	word 6

ONE indicates normal line transmission;

ZERO indicates that this line is not to be

used to expose film and facsimile recorder

line is not to be incremented (stepped).

Data		Position
Scan Count		
BCD value split into 2 chars/word		
2 most significant BCD chars		word 7
2 least significant BCD chars		word 8
Bit Error Count		

MSB   LSB

0 8 MSB		word 9
0 5 LSB 0 0 0		word 10
Computer Error Messages		words 11-12
Unused Locations		words 13-16

Note 1 - ZERO = 1_{16}

         ONE = FF_{16}

APPENDIX B

MISCELLANEOUS DATA SHEETS

APPENDIX B

LISTING OF MISCELLANEOUS DATA SHEETS

2503TA Dynamic RAM Signetics

MK 4008-9P Dynamic RAM Mostek

P3101A Static RAM

N0033C Coax Driver

NH0012C Mos Clock Driver (National)

075107 & 75109 Digital Line Driver & Receiver

DAC-HI High Speed DAC

DAC 19-8BI Economy DAC

AM-103A Wide Band OP AMP

DAS-16M Data Acquisition System

Harris Triple Line Transmitter & Receiver

Power Supplies UNI Series

Model 525 Joystick

MC 1468 $\pm$ 15 Volt Regulator

LM 109 +5 Volt Regulator

DAC -19-8BI

C-3

FEATURES

Fast Settling Times
8, 10, & 12 Bit Resolutions
Binary & BCD Input Codes
Internal Stable References
Unipolar & Bipolar Outputs
Voltage & Current Outputs
Prices from $14.95

These low cost converters feature an excellent choice of parameters for a wide variety of applications. The economy prices of this line make them ideally suited for OEM applications. Both current and voltage output versions are available with 8, 10, and 12 binary bit resolution and 2 or 3 digit BCD input coding. Current output units have settling times of 300 and 500 nsec. while voltage output units have settling times of 5 and 20 μsec. The current output units may be used to develop a voltage output directly using a resistive load. Voltage output models can be operated to give either ±5Volts out or 0 to +10 volts out by simple external pin connection. The DAC-98BI and DAC-98DI models derive their reference from the ±15Volt supply but may be ordered with an internal reference at slightly higher cost.

This miniature series of converters features moderate cost high performance voltage output models. Either unipolar or bipolar operation can be selected by external pin connection. Output voltage settling time is 5 μsec.

SA Special Item No. 66-12b

SPECIFICATIONS (25°C)	MODEL	INPUT RESOLUTION	TYPE OUTPUT	OUTPUT	OUTPUT SETTLING TIME	
	DAC-98BI	8 Binary Bits	Current	0 to +2.6mA @ +1.2V nom. (1)	500 nsec. to ±0.2% of FS	±½
	DAC-98DI	2 Digit BCD	Current	0 to +1.6mA @ +1.2V nom.		
DAC-9	DAC-198B	8 Binary Bits	Voltage	±5V @ ±5mA (3)	20 μsec. to ±0.2% of FS	
SERIES →	DAC-198BI	8 Binary Bits	Current	0 to +2.5mA @ +1.2V nom. (1)	300 nsec. to ±0.2% of FS	±½
	DAC-198D	2 Digit BCD	Voltage	0 to +10V @ 5mA	20 μsec. to ±0.2% of FS	
	DAC-198DI	2 Digit BCD	Current	0 to +1.54mA @ 1.2V nom.	300 nsec. to ±0.2% of FS	
ECONOMY	DAC-298B	8 Binary Bits	Voltage	±5V @ ±5mA (3)	5 μsec. to ±0.2% of FS	±½
GENERAL	DAC-298D	2 Digit BCD	Voltage	0 to +10V @ 5mA		
PURPOSE	DAC-4910B	10 Binary Bits	Voltage	±5V @ ±5mA (3)	5 μsec. to ±0.1% of FS	
	DAC-4910BI	10 Binary Bits	Current	0 to +2.5mA @ +1.2V nom. (1)	300 nsec. to ±0.1% of FS	±½
	DAC-4912D	3 Digit BCD	Voltage	0 to +10V @ 5mA	5 μsec. to ±0.1% of FS	
	DAC-4912DI	3 Digit BCD	Current	0 to +1.54mA @ +1.2V nom. (1)	300 nsec. to ±0.1% of FS	
	DAC-6912B	12 Binary Bits	Voltage	±5V @ ±5mA (3)	20 μsec. to ±.05% of FS	±½
	DAC-6912BI	12 Binary Bits	Current	0 to +2.5mA @ +1.2V nom.	300 nsec. to ±.05% of FS	
DAC-HB	DAC-HB8B	8 Binary Bits				
DAC-I	DAC-HB10B	10 Binary Bits	Voltage	±5V @ ±5mA (3)	5 μsec. to ±.025% of FS	±½
DAC-V	DAC-HB12B	12 Binary Bits				
SERIES	DAC-HB12D	3 Digit BCD				
	DAC-I8B	8 Binary Bits				
	DAC-I10B	10 Binary Bits	Current	±1mA @ ±1.2V nom. (2)	150 nsec. to ±.025% of FS	±½
HIGH	DAC-I12B	12 Binary Bits				
PERFORMANCE	DAC-I8D	2 Digit BCD		+1.25mA @ +1.2V nom.		
MODERATE	DAC-I12D	3 Digit BCD				
COST	DAC-V8B	8 Binary Bits				
	DAC-V10B	10 Binary Bits	Voltage	±10V @ ±10mA (4)	2 μsec. to ±.025% of FS	±½
	DAC-V12B	12 Binary Bits				
	DAC-V8D	2 Digit BCD		0 to +10V @ 10mA		
	DAC-V12D	3 Digit BCD				
DAC-VR	DAC-VR8B	8 Binary Bits				
SERIES	DAC-VR10B	10 Binary Bits	Voltage	±10V @ ±10mA (4)	2 μsec. to ±.025% of FS	±½
(WITH INPUT	DAC-VR12B	12 Binary Bits				
STORAGE REGISTER)	DAC-VR8D	2 Digit BCD		0 to +10V @ 10mA		
	DAC-VR12D	3 Digit BCD				

NOTES:

(1) Bipolar output can be obtained by external pin connection.

(2) Unipolar output can be obtained by external pin connection.

(3) Unipolar output of 0 to +10V @ 5mA can be obtained by external pin connection.

(4) Other optional output voltage ranges are: 0 to +5V FS, 0 to +10V FS, and ±5V FS. See Specification Guide.

(5)

(6)

Operational Amplifiers

LH0033/LH0033C high speed buffer

general description

The LH0033/LH0033C is a very high speed, high input impedance, unity gain buffer. It is intended to fulfill buffer applications such as high speed line driving, and interface to fast A to D converters or high speed comparators. Outstanding typical design features include:

- Very high slew rate, greater than 1500V/μs
- Low propagation delay: 1.2 ns
- Low output offset voltage: 25°C, 5.0 mV; maximum -55°C to +125°C, 15.0 mV
- Low input bias current: 25°C, 50 pA; maxi-

mum -55°C to +125°C, 1 nA
- Large output voltage range: ±13V
- High input impedance: $10^{11}\Omega$
- Wide bandwidth: dc to 100 MHz
- Low output impedance: 6Ω

The LH0033/LH0033C is capable of operation over the voltage range ±5V $\leq$ V$_S$ $\leq$ ±20V. The LH0033 is guaranteed over the temperature range -55°C to +125°C; whereas, the LH0033C is guaranteed over the temperature range 0°C to 85°C.

connection diagrams

12 PIN TO-8
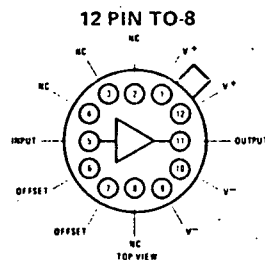
Order Number LH0033G or LH0033CG
See Package 6

Dual-In-Line Package
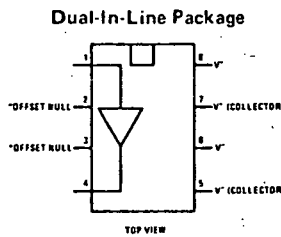
Order Number LH0033CJ
See Package 15

typical applications
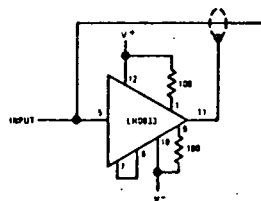
Instrumentation Shield/Line Driver
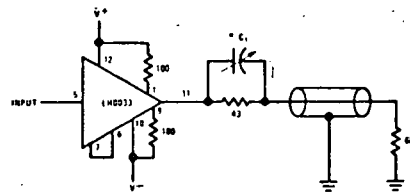
Coaxial Cable Driver
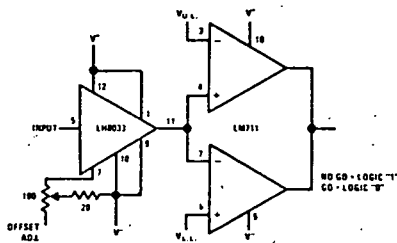
High Input Impedance Comparator
With Offset Adjust
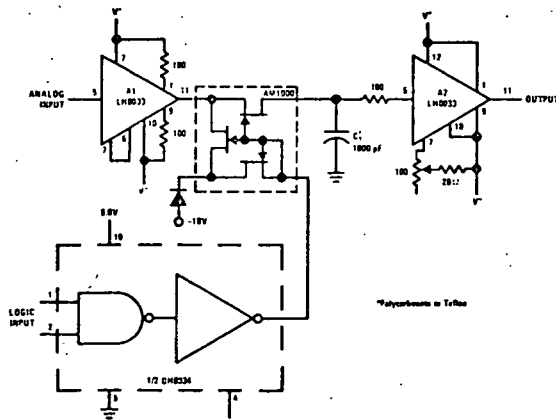
High Speed Sample & Hold

absolute maximum ratings

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation	1.5W
Input Voltage	Equal to Supply Voltage
Maximum Output Current	±100 mA
Operating Temperature Range LH0033	−55°C to +125°C
LH0033C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics

PARAMETER	CONDITIONS	LH0033			LH0033C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Offset Voltage	$R_S = 100\ k\Omega$, $T_A = 25°C$		5.0	10.0		12.0	20.0	mV
	$R_S = 100\ k\Omega$			15.0			25.0	mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\ k\Omega$, $-55°C \leq T_A \leq 125°C$		25			25		μV/°C
Input Bias Current	$T_A = 25°C$		50	100		50	150	pA
				1.0			1.5	nA
Voltage Gain	$V_{IN} = 1.0V$ rms, $f = 1.0\ kHz$, $R_L = 1\ k\Omega$, $R_S = 100\ k\Omega$	.97	0.98		.96	.98		V/V
Input Impedance	$V_{IN} = 1.0V$ rms, $f = 1.0\ kHz$, $R_L = 1\ k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = 1.0V$ rms, $f = 1.0\ kHz$, $R_S = 100\ k\Omega$ $R_L = 1\ k\Omega$		6	10		6	10	Ω
Output Voltage Swing	$R_S = 100\ k\Omega$, $R_L = 1\ k\Omega$	±12	±13		±12	±13		V
Output Voltage Swing	$V_{IN} = ±10.0V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.5			±9.5			V
Propagation Delay	$V_{IN} = ±10V$, $R_S = 50\Omega$, $R_L = 1\ k\Omega$		1.2			1.5		ns
Slew Rate	$R_S = 50\Omega$, $R_L = 1\ k\Omega$ $T_A = 25°C$	1000	1500		1000	1400		V/μs
Bandwidth	$V_{IN} = 1.0V$ rms, $R_S = 50\Omega$ $R_L = 1\ k\Omega$		100			100		MHz
Supply Current	$V_{IN} = 0V$		20	22		21	24	mA

Note 1: Unless otherwise noted, these specifications apply for +15.0V applied to pins 1 & 12, −15.0V applied to pins 9 & 10, pin 6 shorted to pin 7 over the temperature range −55°C to +125°C for the LH0033 and 0°C to +85°C for the LH0033C.

Note 2: Unless otherwise noted, typical values are for $T_A = 25°C$.
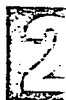
typical performance characteristics

Power Dissipation

POWER DISSIPATION (W)

1.5
1.25
1.00
.75
.50
.25

0   25   50   75   100   125   150
TEMPERATURE (°C)
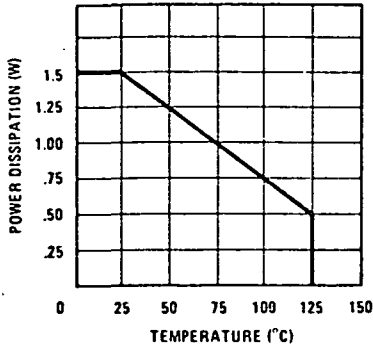
Supply Current vs Supply Voltage

SUPPLY CURRENT (mA)

21
20
19
18
17

$T_A = -55°C$
$T_A = +25°C$
$T_A = +125°C$

5   10   15   20
SUPPLY VOLTAGE (±V)
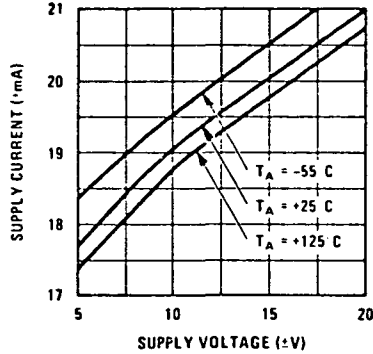
Output Voltage vs Supply Voltage

OUTPUT VOLTAGE (±V)

18
16
14
12
10
8
6
4

$R_L = 1 k\Omega$
$R_S = 100 k\Omega$
$T_A = +25°C$

5   10   15   20
SUPPLY VOLTAGE (±V)

Positive Pulse Response

INPUT/OUTPUT VOLTAGE (V)

12
10
8
6
4
2
0

$V_S = \pm15V$
$R_L = 1 k\Omega, R_S = 50\Omega$
$T_A = +25°C$

INPUT
OUTPUT

0   10   20   30   40   50   60
TIME (ns)

Negative Pulse Response

INPUT/OUTPUT VOLTAGE (-V)

0
-2
-4
-6
-8
-10
-12

$V_S = \pm15V$
$R_S = 50\Omega$
$R_L = 1 k\Omega$
$T_A = +25°C$

INPUT
OUTPUT

0   10   20   30   40   50   60
TIME (ns)

Frequency Response

VOLTAGE GAIN (V/V)

1.0
0.8
0.6
0.4
0.2

PHASE LAG (DEGREES)

40
35
30
25
20
15
10
5

$V_S = \pm15V$
$R_S = 50\Omega$
$R_L = 50\Omega$
$V_{IN} = 1.0V$ rms

Av
ϕ

1.0   2.0   5.0   10.0   20.0   50   100
FREQUENCY (MHz)
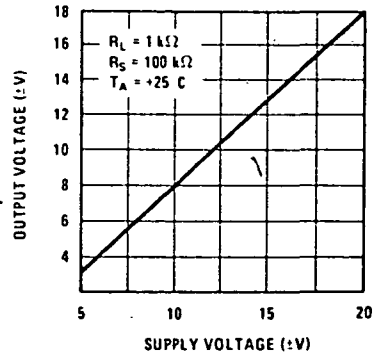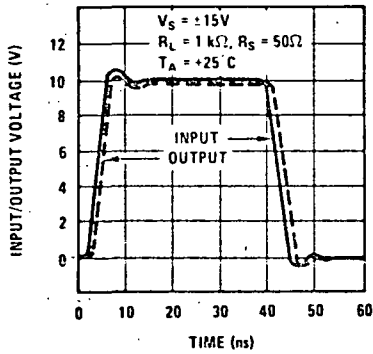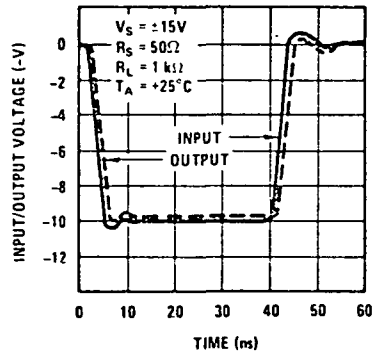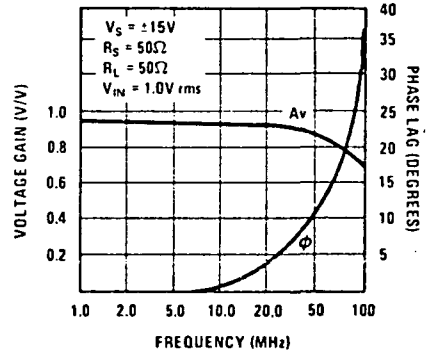
Rise and Fall Time vs Temperature

RISE AND FALL TIME (ns)

8.0
6.0
4.0
2.0
0

$V_S = \pm15V$
$R_S = 50\Omega$
$R_L = 1 k\Omega$

t_f
t_r

-50   0   50   100   150
TEMPERATURE (°C)
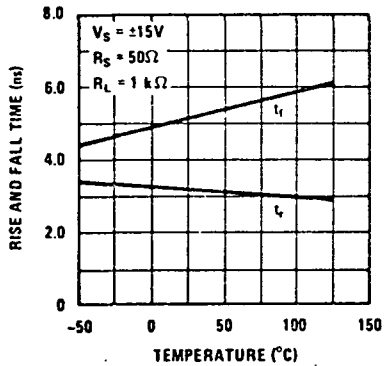
Input Bias Current vs Temperature

INPUT BIAS CURRENT (nA)

1.00
0.100
.010
.001

$V_S = \pm20V$
$V_S = \pm15V$
$V_S = \pm10V$

0   25   50   75   100   125
TEMPERATURE (°C)
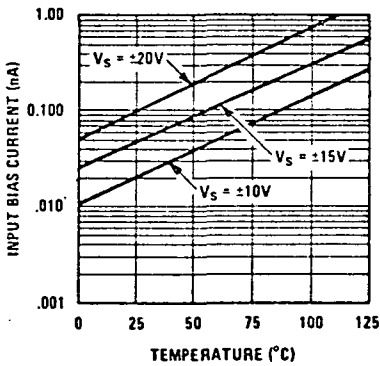
Output Offset Voltage vs Temperature

OUTPUT OFFSET VOLTAGE (±mV)

8.0
6.0
4.0
2.0
0

$V_S = \pm15.0V$
$R_S = 100 k\Omega$

-50   0   50   100   150
TEMPERATURE (°C)
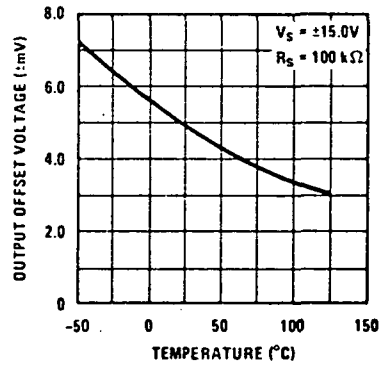
applications information

1. Offset Adjustment

The LH0033 provides two terminals to adjust the output offset voltage. Offset null may be accomplished by connection a 100 ohm pot between pin 7 and V⁻. In non-critical or ac coupled applications pin 5 should be shorted to pin 7. The resulting output offset is typically 5 mV at 25°C.

2. Operation with Asymmetrical Supplies

The LH0033 may be readily used in applications where symmetrical supplies are unavailable or may not be desirable. A typical application might be an interface to an MOS shift register where V⁺ = 5.0V and V⁻ = -25V. In this case, an apparent output offset occurs. In reality, the output voltage is due to the

applications information (cont.)

LH0033's voltage gain of less than unity. The output voltage shift due to asymmetrical supplies may be predicted by:

$$\Delta V_O \cong (1 - Av)\frac{(V^+ - V^-)}{2} = .005\ (V^+ - V^-)$$

where: Av = No load voltage gain, typically. 0.99
V$^+$ = Positive Supply Voltage.
V$^-$ = Negative Supply Voltage.

For the foregoing application, ΔV_O would be −100 mV. This apparent "offset" may be adjusted to zero as outlined above.

3. Capacitive Loading
The LH0033 has been designed to drive heavy capacitive loads such as coaxial cables and the like. Pin 1 has been brought out separately from pin 12 (V$^+$) and pin 9 from pin 10 (V$^-$). This provision allows insertion of damping resistors between V$^+$ and pin 1 and V$^-$ and pin 9. Values of resistance between 47 and 100 ohms work well for capacitive loads to 1000 pF. For nonreactive loads, pin 12 should be shorted to pin 1 and pin 10 shorted to pin 9.

4. Operation Within an Op Amp Loop
Obviously, the LH0033 may be used as a current booster within a closed loop with an LM108, LM741, or NH0022 operational amplifier. An isolation resistor of no less than 47 ohms should be used between the op amp output and the input to the LH0033. The resistor will assure stability. The LH0033's high input impedance guarantees that the operational amplifier will not be loaded.

5. Short Circuit Protection
The LH0033/LH0033C may be protected from an output short circuit by inserting the appropriate limiting resistor between pin 12 (V$^+$) and pin 1, and between pin 10 (V$^-$) and pin 9. The value for the resistor is given by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: I_{SC} = output current under short circuit conditions $\leq$ 100 mA

The inclusion of a limiting resistor will, by necessity, limit the output voltage swing. However, decoupling pins 1 and 9 through disc capacitors to ground, will allow near full output swing and slew rate.

Interface Circuits

MH0012/MH0012C high speed MOS clock driver

general description

The MH0012/MH0012C is a high performance clock driver that is designed to be driven by the DM7830/DM8830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

features

- High output voltage swings—12 to 30 volts
- High output current drive capability—1000 mA peak
- High repetition rate—10 MHz at 18 volts into 100 pF
- Low standby power—less than 30 mW

schematic and connection diagrams

12-lead TO-8 Package

TOP VIEW
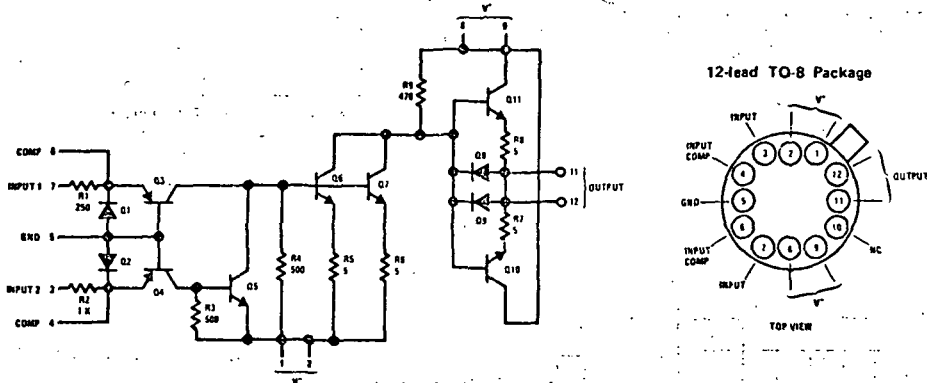
typical application (ac test circuit)

timing diagram

UNITS
ns
.ns
ns
ns
ns
ns
ns
ns

MH0012/MH0012C
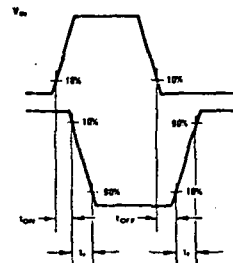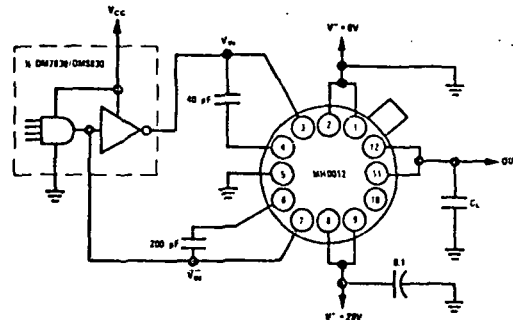
absolute maximum ratings

V⁻ Supply Voltage: Differential (Pin 1 or 2 to Pin 5)   −40V
V⁺ Supply Voltage: Differential (Pin 8 or 9 to Pin 1 or 2)   30V
Input Current: (Pin 3 or 7)   ±75 mA
Peak Output Current   ±1000 mA

Maximum Output Load—See Figure 2
Power Dissipation—See Figure 1   1.5W
Storage Temperature   −65°C to +150°C
Operating Temperature: MH0012   −55°C to +125°C
    MH0012C   0°C to +85°C
Lead Temperature (Soldering, 10 sec)   300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} < V^- + 2V$		1.0	2.0	V
Logic "0" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} > V^+ - 1.5V$	0.4	0.6		V
Logic "1" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = 1mA$, $V_{IN} = 2.0V$		$V^- + 1.0$	$V^- + 2.0$	V
Logic "0" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = -1mA$, $V_{IN} = 0.4V$	$V^+ - 1.5$	$V^+ - 0.7$		V
I_{DC} (V⁻ Supply)	$V^+ - V^- = 20V$, $V_{IN} = 2.0V$		34	60	mA

ac electrical characteristics

PARAMETER	CONDITIONS (Note 3)	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})	$V^+ - V^- = 20V$, $V_{CC} = 5.0V$		10	15	ns
Rise Time (t_r)	$C_L = 200 pF$, $f = 1.0 MHz$		5	10	ns
Turn-Off Delay (t_{OFF})	$T_A = 25°C$		35	50	ns
Fall Time (t_f)			35	45	ns

Note 1: Characteristics apply for circuit of Figure 1. Min and max limits apply from −55°C to +125°C for the MH0012 and from 0°C to +85°C for the MH0012C. Typical values are for $T_A = 25°C$.
Note 2: Due to the very fast rise and fall times, and the high currents involved, extremely short connections and good by passing techniques are required.
Note 3: All conditions apply for each parameter.

Power Dissipation
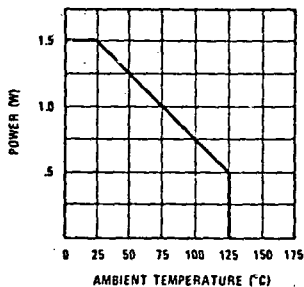
Figure 1.

Maximum Output Load vs Voltage Swing vs Rise Times
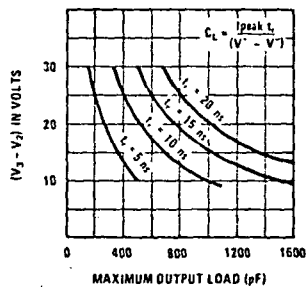
Figure 2.

Rise and Fall Times vs Load Capacitance
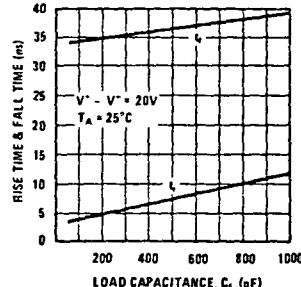
applications information

Power Dissipation Considerations

The power dissipated by the MH0012 may be divided into three areas of operation = ON, OFF and switching. The OFF power is approximately 30 mW and is dissipated by R_2 when Pin 3 is in the logic "1" state. The OFF power is negligible and will be ignored in the subsequent discussion. The ON power is dissipated primarily by O_3 and R_9 and is given by:

$$P_{ON} \cong [V^- I_{IN} + \frac{(V^+ - V^-)^2}{R_9}] \ DC \quad (1)$$

Where:

$$DC = Duty\ Cycle = \frac{ON\ Time}{ON\ Time\ \&\ OFF\ Time}$$

I_{IN} is given by $\frac{V_{IN} - V_{BE3}}{R_1}$ and equation (1) becomes:

$$P_{ON} = \left[\frac{(V_{IN} - V_{BE3})|V^-|}{R_1} + \frac{(V^+ - V^-)^2}{R_9} \right] DC \quad (2)$$

For $V_{IN} = 2.5V$, $V_{BE3} = 0.7V$, $V^+ = 0V$, $V^- = -20V$, and DC = 20%, $P_{ON} \cong 200\ mW$.

The transient power incurred during switching is given by:

$$P_{AC} = (V^+ - V^-)^2 \ C_L f \quad (3)$$

For $V^+ = 0V$, $V^- = -20V$, $C_L = 200$ pF, and $f = 5.0$ MHz, $P_{AC} = 400$ mW.

The total power is given by:

$$P_T = P_{AC} + P_{ON} \quad (4)$$
$$P_T \leq P_{MAX}$$

For the above example, $P_T = 600$ mW.

(right column partially visible)

MH0013/M

general desc

schematic a

typical applic

8-108
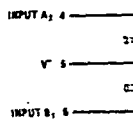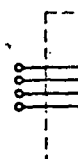
intel® Schottky Bipolar 3101, 3101A

HIGH SPEED FULLY DECODED
64 BIT MEMORY

- **Fast Access Time -- 35 nsec. max.**
  over 0-75° C Temperature Range.
  (3101A)

- **Simple Memory Expansion through**
  Chip Select Input -- 17 nsec. max.
  over 0-75° C Temperature Range.
  (3101A)

- **DTL and TTL Compatible -- Low**
  Input Load Current: 0.25mA. max.

- **OR-Tie Capability --**
  Open Collector Outputs.

- **Fully Decoded -- on Chip Address**
  Decode and Buffer.

- **Minimum Line Reflection -- Low**
  Voltage Diode Input Clamp.

- **Ceramic and Plastic Package --**
  16 Pin Dual In-Line Configuration.

The Intel® 3101 and 3101A are high speed fully decoded 64 bit random access memories, organized 16 words by 4 bits. Their high speed makes them ideal in scratch pad applications. An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices with gold diffusion processes.

The Intel 3101 and 3101A are packaged in either hermetically sealed 16 pin ceramic packages, or in low cost silicone packages, and their performance is specified over a temperature range from 0°C to 75°C.

The storage cells are addressed through an on chip 1 of 16 binary decoder using four input address leads.

A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied.

In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.
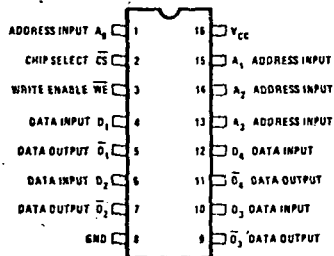
PIN CONFIGURATION   LOGIC SYMBOL   BLOCK DIAGRAM
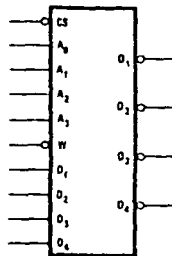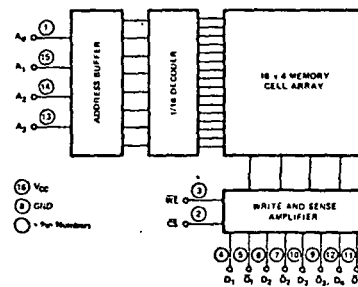
PIN NAMES

D_1-D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0-A_3	ADDRESS INPUTS	$\overline{O}_1$-$\overline{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	-	HIGH
HIGH	HIGH	-	HIGH

Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		100 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.25	mA	$V_{CC} = 5.25V$, $V_A = 0.45V$
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_{CC} = 5.25V$, $V_D = 0.45V$
I_{FW}	WRITE INPUT LOAD CURRENT		−0.25	mA	$V_{CC} = 5.25V$, $V_W = 0.45V$
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.25	mA	$V_{CC} = 5.25V$, $V_S = 0.45V$
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT		10	μA	$V_{CC} = 5.25V$, $V_A = 5.25V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		10	μA	$V_{CC} = 5.25V$, $V_D = 5.25V$
I_{RW}	WRITE INPUT LEAKAGE CURRENT		10	μA	$V_{CC} = 5.25V$, $V_W = 5.25V$
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT		10	μA	$V_{CC} = 5.25V$, $V_S = 5.25V$
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−1.0	V	$V_{CC} = 4.75V$, $I_A = -5.0$ mA
V_{CD}	DATA INPUT CLAMP VOLTAGE		−1.0	V	$V_{CC} = 4.75V$, $I_D = -5.0$ mA
V_{CW}	WRITE INPUT CLAMP VOLTAGE		−1.0	V	$V_{CC} = 4.75V$, $I_W = -5.0$ mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−1.0	V	$V_{CC} = 4.75V$, $I_S = -5.0$ mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	$V_{CC} = 4.75V$, $I_{OL} = 15$ mA, Memory Stores "Low"
I_{CEX}	OUTPUT LEAKAGE CURRENT		100	μA	$V_{CC} = 5.25V$, $V_{CEX} = 5.25V$, $V_S = 2.5V$
I_{CC}	POWER SUPPLY CURRENT		105	mA	$V_{CC} = 5.25V$, $V_A = V_S = V_D = 0V$
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	$V_{CC} = 5.0V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$

Typical Characteristics

OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE

INPUT CURRENT VS. INPUT VOLTAGE

INPUT THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE

Switching C!

Conditions of Tes:

Input Pulse am:

Input Pulse ris:
5 nanosec:
and 2 vol:

Speed measure-

Output loading

READ CYCLE
Address to Output De:

A_0, A_1, A_2, A_3

CHIP SELECT INPUT

O_1, O_2, O_3, O_4

Chip Select to Outpu:

A_0, A_1, A_2, A_3

CHIP SELECT INPUT

O_1, O_2, O_3, O_4

NOTE 1: t_{SR} is associa:

A.C. Characte:

SYMBOL	PARAM:
t_{S+}, t_{S-}	Chip Selec: Delay
t_{A-}, t_{A+}	Address to : Delay

CAPACITANCE [2]

C_{IN}	INPUT (All Pi
C_{OUT}	OUTP\

Switching Characteristics

Conditions of Test:

Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

Output loading is 15mA and 30 pF

15 mA Test Load

READ CYCLE
Address to Output Delay
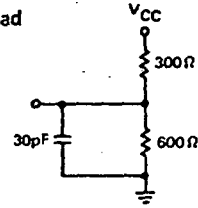
Chip Select to Output Delay
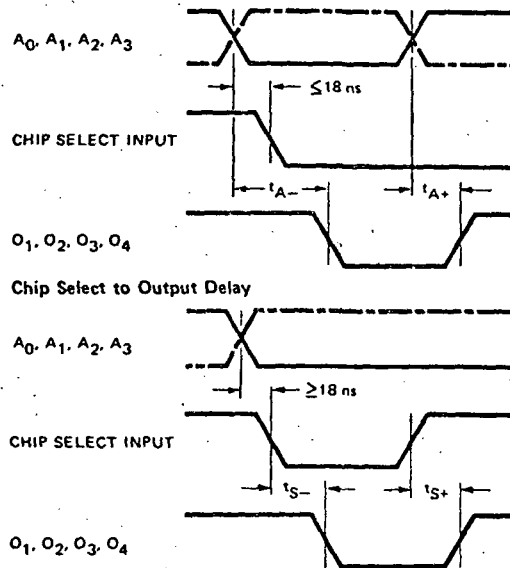
WRITE CYCLE
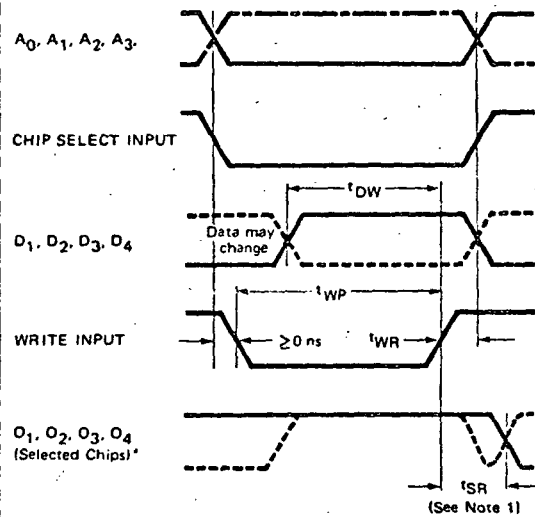
*Outputs of unselected chips remain high during write cycle.

NOTE 1: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

READ CYCLE		3101A		3101	
SYMBOL	PARAMETER	LIMITS (ns)		LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	17	5	42
t_{A-}, t_{A+}	Address to Output Delay	10	35	10	60

CAPACITANCE[2] T_A = 25°C

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

WRITE CYCLE		3101A		3101	
SYMBOL	TEST	LIMITS (ns)		LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		35		50
t_{WP}	Write Pulse Width	25		40	
t_{DW}	Data-Write Overlap Time	25		40	
t_{WR}	Write Recovery Time	0		5	

NOTE 2:   This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

2-103
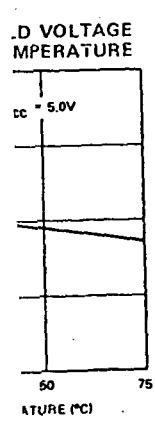
Typical A.C. Characteristics

**ADDRESS TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE**

$V_{CC} = 5.0V \pm 5\%$
$C_L = 30\,pF$

t_{A+}
t_{A-}

ADDRESS TO OUTPUT DELAY (ns)

AMBIENT TEMPERATURE (°C)

**CHIP SELECT TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE**

$V_{CC} = 5.0V \pm 5\%$
$C_L = 30\,pF$

t_{S-}
t_{S+}
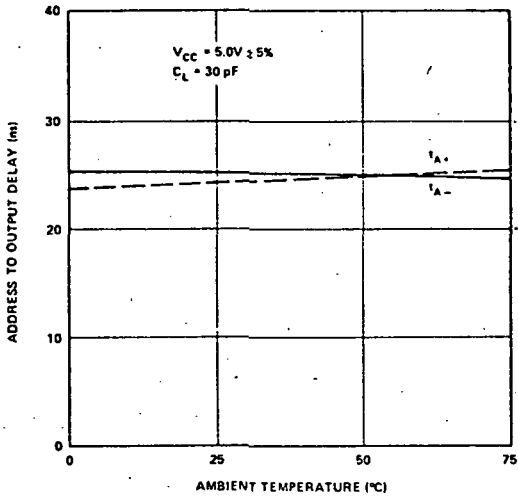
CHIP SELECT TO OUTPUT DELAY (ns)

AMBIENT TEMPERATURE (°C)
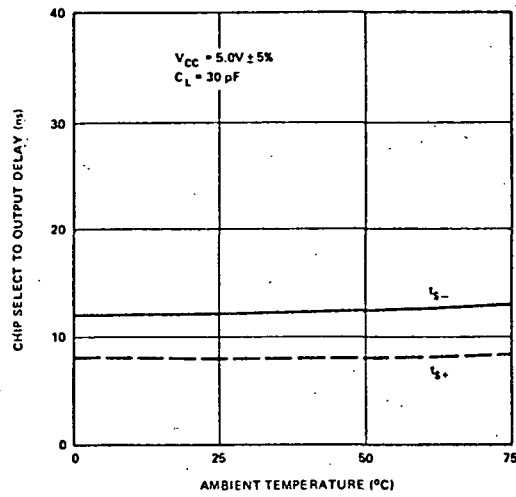
**ADDRESS & CHIP SELECT TO OUTPUT DELAY
VS.
LOAD CAPACITANCE**

$V_{CC} = 5.0V \pm 5\%$
D.C. LOAD = 15 mA
$T_A = 25°C$

t_{A+}
t_{A-}
t_{S+}
t_{S-}

ADDRESS AND CHIP SELECT DELAY (ns)

LOAD CAPACITANCE (pF)
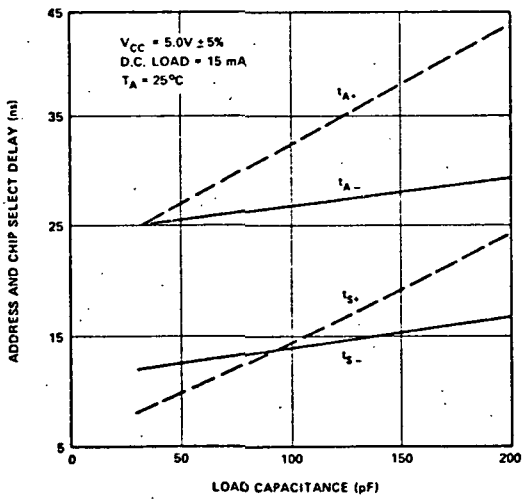
**WRITE PULSE WIDTH & SENSE
AMPLIFIER RECOVERY TIME
VS. AMBIENT TEMPERATURE**
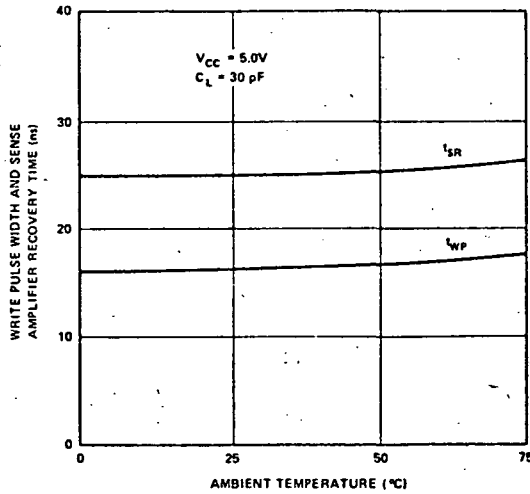
$V_{CC} = 5.0V$
$C_L = 30\,pF$

t_{SR}
t_{WP}

WRITE PULSE WIDTH AND SENSE
AMPLIFIER RECOVERY TIME (ns)

AMBIENT TEMPERATURE (°C)

---

intel

HIG

■ Militar
  −55°C

□ Fast A
  Maxim

The M3101 and M310
ideal in scratch pad a
rier diode clamped tr
process.

PIN CONFIGU

ADDRESS INPUT A_0 ☐ 1
CHIP SELECT $\overline{CS}$ ☐ 2
WRITE ENABLE $\overline{WE}$ ☐ 3
DATA INPUT D_1 ☐ 4
DATA OUTPUT $\overline{O}_1$ ☐ 5
DATA INPUT D_2 ☐ 6
DATA OUTPUT $\overline{O}_2$ ☐ 7
GND ☐ 8
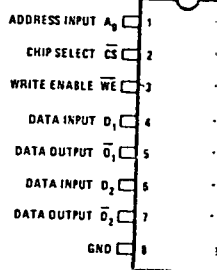
CHIP SELECT	WRITE EN
LOW	LOW
LOW	HIGH
HIGH	LOW
HIGH	HIGH

D. C. and Ope

Symbol	
I_{FA}	Address I
I_{FD}	Data Input
I_{FW}	Write Inpu
I_{FS}	Chip Select
I_{RA}	Address In
I_{RD}	Data Input
I_{RW}	Write Input
I_{RS}	Chip Select
V_{CA}	Address In
V_{CD}	Data Input
V_{CW}	Write Input
V_{CS}	Chip Select
V_{OL}	Output "Lo
I_{CEX}	Output Lea
I_{CC}	Power Sup
V_{IL}	Input "Low
V_{IH}	Input "High

DESCRIPTION

The LM109 and LM309 are complete 5 volt regulators fabricated on a single silicon chip. These regulators are designed for local "on card" regulation to eliminate many of the noise and ground loop problems associated with single-point regulation. They employ internal current limiting, thermal shutdown, and safe-area compensation which makes the circuitry essentially blow-out proof. If adequate heat sinking is provided, the devices can deliver output currents in excess of 200mA from the TO-5 package, and 1A from the TO-3 package. In addition to their use as fixed 5 volt regulators, these devices may be used with external components to obtain adjustable output levels. They may also be used as the power pass element in precision regulators.

FEATURES

- OUTPUT CURRENTS IN EXCESS OF 1 amp
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL CURRENT LIMITING
- NO EXTERNAL COMPONENTS REQUIRED

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM109	-55°C to 150°C
LM309	0°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATIONS

H PACKAGE
(Bottom View)
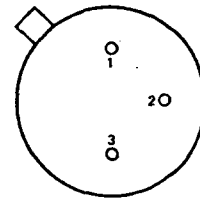
1. Input
2. Output
3. Ground

ORDER PART NOS. LM109H/LM309H

K PACKAGE
(Bottom View)
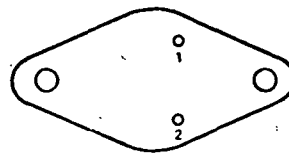
1. Input
2. Output

Case is connected to ground.

ORDER PART NOS. LM109K/LM309K

EQUIVALENT CIRCUIT
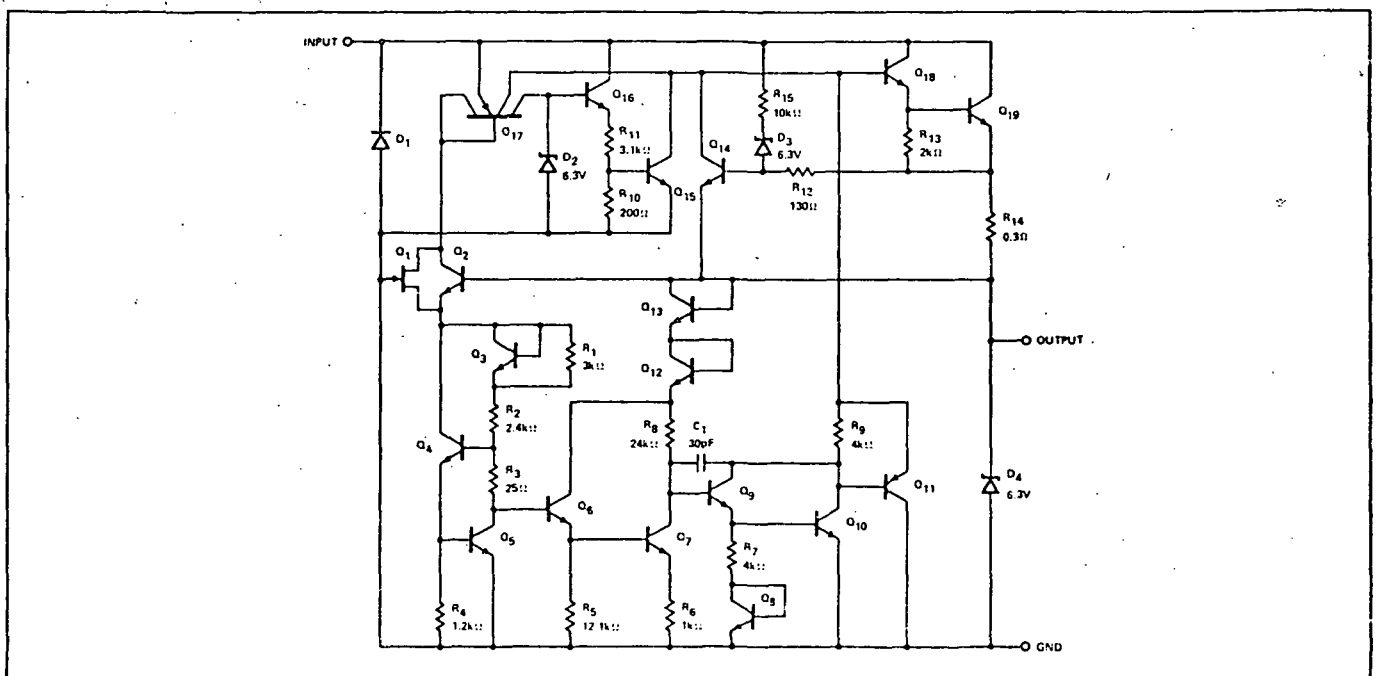
ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	LM109			LM309			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$							
	$7V \leqslant V_{IN} \leqslant 25V$		4	50		4	50	mV
Load Regulation	$T_j = 25°C$							
TO-5	$5mA \leqslant I_{OUT} \leqslant 0.5A$		20	50		20	50	mV
TO-3	$5mA \leqslant I_{OUT} \leqslant 1.5A$		50	100		50	100	mV
Output Voltage	$7V \leqslant V_{IN} \leqslant 25V$							
	$5mA \leqslant I_{OUT} \leqslant I_{max}$							
	$P < P_{max}$	4.6		5.4	4.75		5.25	V
Quiescent Current	$7V \leqslant V_{IN} \leqslant 25V$		5.2	10		5.2	10	mA
Quiescent Current Change	$7V \leqslant V_{IN} \leqslant 25V$			0.5			0.5	mA
	$5mA \leqslant I_{OUT} \leqslant I_{max}$			0.8			0.8	mA
Output Noise Voltage	$T_A = 25°C$							
	$10Hz \leqslant f \leqslant 100 \text{ kHz}$		40			40		μV
Long Term Stability				10			20	mV
Thermal Resistance								
Junction to Case (Note 2)								
TO-5			15			15		°C/W
TO-3			3			3		°C/W

NOTES:

1. Unless otherwise specified, these specifications apply for $-55°C \leqslant T_j \leqslant 150°C$ for the 5109 or $0°C \leqslant T_j \leqslant 125°C$ for the 5309, $V_{IN} = 10V$ and $I_{OUT} = 0.1A$ for the TO-5 package or $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-5 package, $I_{max} = 0.2A$ and $P_{max} = 2.0W$. For the TO-3 package, $I_{max} = 1.0A$ and $P_{max} = 20W$.

2. Without a heat sink, the thermal resistance of the TO-5 package is about $150°C/W$, while that of the TO-3 package is approximately $35°C/W$. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

TYPICAL APPLICATIONS

FIXED 5V REGULATOR
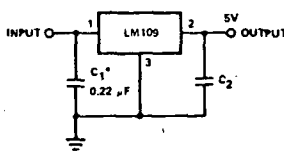
NOTES: *Required if regulator is located an appreciable distance from power supply filter.

†Although no output capacitor is needed for stability, it does improve transient response.

PRECISION VOLTAGE REGULATOR
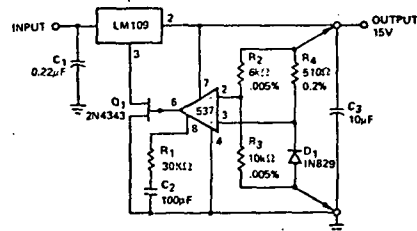
NOTES: *Regulation better than 0.01% load, line and temperature, can be obtained.

†Determines zener current. May be adjusted to minimize thermal drift.

‡Solid tantalum.

ADJUSTABLE OUTPUT REGULATOR
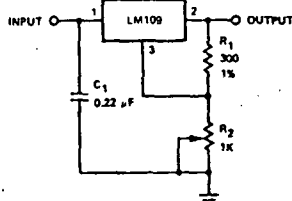
CURRENT REGULATOR
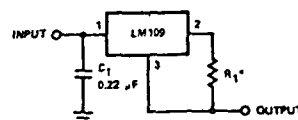
NOTES: *Determines output current.

TYPICAL CHARACTERISTIC CURVES

MAXIMUM AVERAGE POWER DISSIPATION LM109 (TO-3)
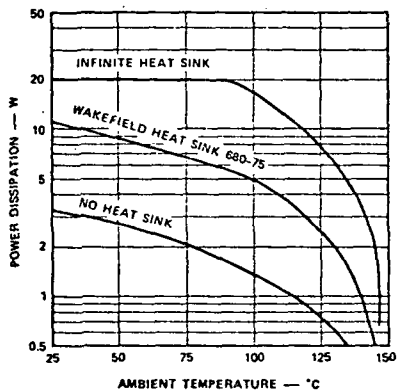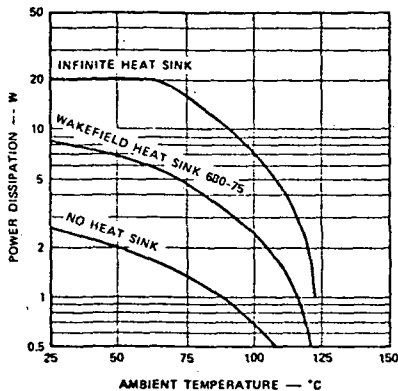
INFINITE HEAT SINK
WAKEFIELD HEAT SINK 680-75
NO HEAT SINK

POWER DISSIPATION — W
AMBIENT TEMPERATURE — °C

MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-3)

INFINITE HEAT SINK
WAKEFIELD HEAT SINK 680-75
NO HEAT SINK

POWER DISSIPATION — W
AMBIENT TEMPERATURE — °C

MAXIMUM AVERAGE POWER DISSIPATION LM109 (TO-5)

INFINITE HEAT SINK
WAKEFIELD HEAT SINK 207
NO HEAT SINK

POWER DISSIPATION — W
AMBIENT TEMPERATURE — °C

MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-5)

INFINITE HEAT SINK
WAKEFIELD HEAT SINK 207
NO HEAT SINK

POWER DISSIPATION — W
AMBIENT TEMPERATURE — °C

OUTPUT IMPEDANCE

$V_{IN} = 10V$
$T_A = 25°C$
$I_L = 20mA$
$I_L = 500mA$
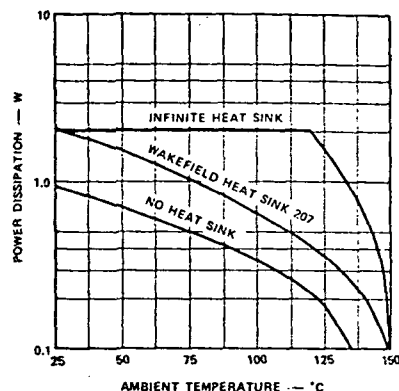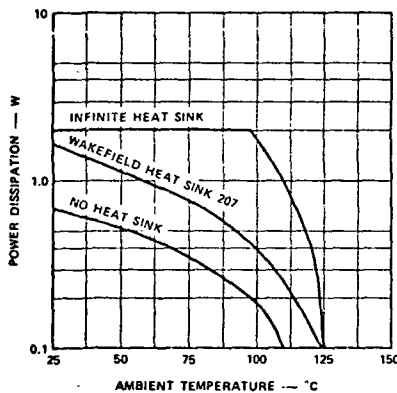
OUTPUT IMPEDANCE — Ω
FREQUENCY — Hz
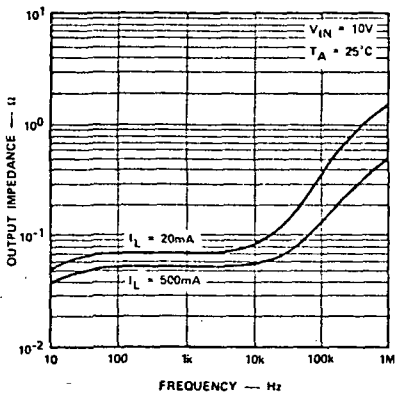
PEAK OUTPUT CURRENT K PACKAGE (TO-3)

$V_{OUT} = 4.5V$
$T_j = -55°C$
$T_j = 25°C$
$T_j = 125°C$
$T_j = 150°C$

OUTPUT CURRENT — A
INPUT VOLTAGE — V
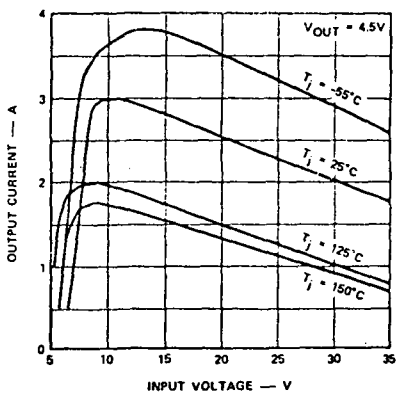
PEAK OUTPUT CURRENT H PACKAGE (TO-5)

$V_{OUT} = 4.5V$
$T_j = -55°C$
$T_j = 125°C$
$T_j = 25°C$
$T_j = 150°C$

OUTPUT CURRENT — A
INPUT VOLTAGE — V

RIPPLE REJECTION

$I_L = 200mA$
$V_{IN} = 10V$
$\Delta V_{IN} = 3V$ p-p
$T_j = 25°C$
$T_j = -55°C$
$T_j = 125°C$
$T_j = 150°C$

RIPPLE REJECTION — dB
FREQUENCY — Hz

TYPICAL CHARACTERISTIC CURVES (Cont'd.)

DROPOUT VOLTAGE

DROPOUT VOLTAGE

DROPOUT CHARACTERISTIC

OUTPUT VOLTAGE

OUTPUT VOLTAGE

OUTPUT NOISE VOLTAGE

QUIESCENT CURRENT

QUIESCENT CURRENT

Signetics

1024 BIT CAPACITY MULTIPLEXED DYNAMIC SHIFT REGISTERS

SILICON GATE MOS 2500 SERIES

2502 2503 2504

DESCRIPTION

These Signetics 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

FEATURES

- 10 MHz TYPICAL DATA RATE
- THREE CONFIGURATIONS—QUAD 256, DUAL 512, SINGLE 1024
- LOW POWER DISSIPATION—40 μW/bit at 1 MHz DATA RATE
- LOW CLOCK CAPACITANCE—140 pF
- TTL, DTL COMPATIBLE
- STANDARD PACKAGES – 8 LEAD TO-99, 8-PIN AND 16-PIN SILICONE DUAL IN-LINE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (10 MHz typical) while reducing power dissipation and and clock input capacitance dramatically as compared to conventional technologies.
The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

The data inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

PIN CONFIGURATIONS (Top View)

2502B

1. OUT 1	16. IN 4
2. NC	15. NC
3. IN 1	14. OUT 4
4. ϕ1	13. NC
5. V_{CC}	12. V_{DD}
6. OUT 2	11. ϕ2
7. NC	10. IN 3
8. IN 2	9. OUT 3

2503V

1. OUT$_2$	8. V_{CC}
2. IN$_2$	7. ϕ_1
3. ϕ_2	6. IN$_1$
4. V_{DD}	5. OUT$_1$

2503TA

1. OUT 1	5. OUT 2
2. IN 1	6. IN 2
3. ϕ1	7. ϕ2
4. V_{CC}	8. V_{DD}

2504V

1. OUT	8. V_{CC}
2. ϕ_2	7. NC
3. NC	6. ϕ_1
4. V_{DD}	5. IN

2504TA

1. NC	5. OUT
2. IN	6. NC
3. ϕ1	7. ϕ2
4. V_{CC}	8. V_{DD}

PART IDENTIFICATION TABLE

TYPE	FUNCTION	PACKAGE
2502B	Quad 256-bit	16-Pin DIP
2503TA	Dual 512-bit	TO-99
2503V	Dual 512-bit	8-Pin DIP
2504TA	Single 1024-bit	TO-99
2504V	Single 1024-bit	8-Pin DIP

DATEL SYSTEMS, INC.

HIGH SPEED DIGITAL-TO-ANALOG CONVERTERS

DAC-FI SERIES
DAC-GI SERIES
DAC-HI SERIES

GENERAL DESCRIPTION

This series of D/A converters are miniature ultra high speed devices offering the user state-of-the-art output settling time. Twenty-five nanoseconds for DAC-HI, fifty nanoseconds for DAC-GI and one hundred nanoseconds for DAC-FI series. Standard versions are available with either eight bit or ten bit resolution. Accuracy specifications include ±1/2 LSB linearity, ±15ppm/°C temperature coefficient, and ±0.05% full scale accuracy.

Bipolar operation is achieved by externally connecting the built-in offsetting reference. Input coding can be straight binary for unipolar output or a choice of offset binary or two's complement for bipolar output.

:h D/A is completely self-contained requiring only ±15 volts D.C. power. Packaged in 2" x 2" x 0.4", low profile modules, they are readily soldered or plugged directly into P.C. cards or other mother board hardware. Included in each module is digital interface logic, a precision resistor ladder network, high speed electronic switches, and a temperature compensated precision voltage reference source.

One of the many prime features is the output flexibility — 5 ma current output can be fed directly into an external resistor to develop a 1.2V maximum output or by external pin strapping a bipolar output of ±1.2V maximum can be generated across the output load resistor. The output current can also be fed into an operational amplifier for those who require sign inversion, scaling, etc. This amplifier can be selected to suit a particular application.

Applications for these devices are numerous, graphic generators, computer displays, high speed A/D converters, test equipment, etc.

FOR ULTRA-HIGH SPEED APPLICATIONS

FEATURES

- ☐ Fastest settling time available . . . . . . 25 nanosec's to 0.1% of FS.
- ☐ High Resolution . . . . Up to 10 Binary bits
- ☐ Small Size . . . . 2" x 2" x 0.4" — will mount directly on P.C. boards having 0.5" centers.
- ☐ Low Temperature coefficient . . . . . . ± 15 ppm/°C of FS (±0.0015%)
- ☐ Ultra linear . . . . ± 1/2 LSB (± 0.05%)
- ☐ Adjustment-Free operation . . . . . . Over temperature range of 0°C to +70°C
- ☐ Hardware compatible . . . . Conforms to dual in-line packaging. All pins are .020" dia. @ .100" centers.
- ☐ Inputs compatible to either DTL or TTL logic.
- ☐ Completely repairable . . . . One Year Guarantee
- ☐ Self contained . . . . Simply apply D.C. power.
- ☐ Low Cost . . . . See enclosed price list
- ☐ Externally Programmable . . . . Unipolar or Bipolar Output

BLOCK DIAGRAM
MODEL DAC-FI,GI,HI

MECHANICAL LAYOUT

BOTTOM VIEW

SIDE VIEW
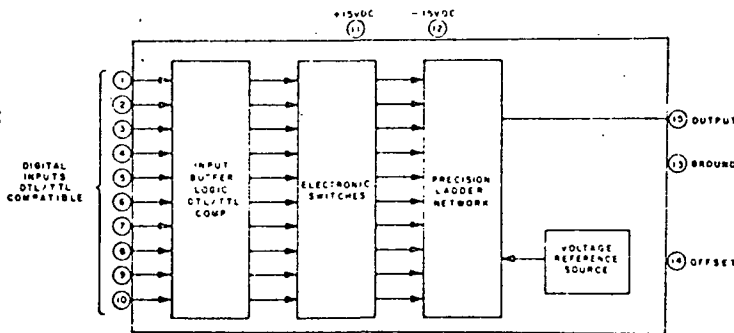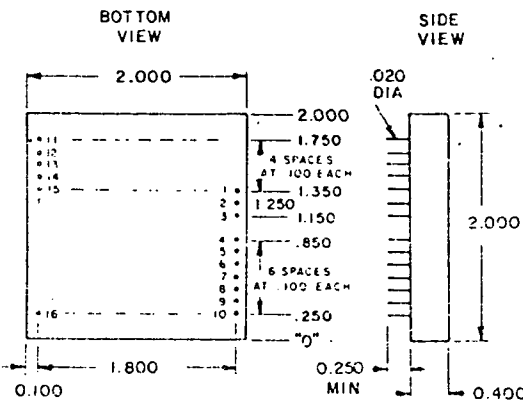
DAC-FI SERIES
DAC-GI SERIES
DAC-HI SERIES
MODULE INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Bit 1 input (MSB)	9	Bit 9 input
2	Bit 2 input	10	Bit 10 input (LSB)
3	Bit 3 input	11	+15V Power input
4	Bit 4 input	12	-15V Power input
5	Bit 5 input	13	Common ground
6	Bit 6 input	14	Offset
7	Bit 7 input	15	Analog output
8	Bit 8 input	16	No connection

PARAMETERS	DAC-FI SERIES	DAC-GI SERIES
DIGITAL INPUTS		
RESOLUTION	Optional 8 or 10 Binary Bits	Optional 8 or 10 Binary Bits
CODING (Parallel Data in the following Formats)	Straight Binary (Unipolar Output) Offset Binary (Bipolar Output) Two's Complement (Bipolar Output)	Straight Binary (Unipolar Output) Offset Binary (Bipolar Output) Two's Complement (Bipolar Output)
DATA INPUTS	DTL or TTL Compatible Positive Logic Loading: 2 standard TTL loads	DTL or TTL Compatible Positive Logic Loading: 2 standard TTL loads

INPUT CODE	V INPUT MIN.	MAX.	BIT STATUS
"0"	0V	+0.8V	OFF
"1"	+2.0V	+5.5V	ON

PARAMETERS	DAC-FI SERIES	DAC-GI SERIES
ANALOG OUTPUT (@ 25°C)		
ACCURACY	Adj. to ±0.05%	Adj. to ±0.05%
TYPE OF OUTPUT	Current	Current
FULL SCALE OUTPUT	5 ma @ +1.2V max. (Unipolar) ±2.5 ma @ ±1.2V max. (Bipolar)(1)	5 ma @ +1.2V max. (Unipolar) ±2.5 ma @ ±1.2V max. (Bipolar) (1)
OUTPUT IMPEDANCE	600 Ohms ±1%	600 Ohms ±1%
OUTPUT ZERO OFFSET	15 na	15 na
OUTPUT LOADING	300 ohms for 0 to +1V Output 2.325K for ±1.0V Output	300 ohms for 0 to +1V Output 2.325K for ± 1.0V Output
OUTPUT SETTLING TIME	100 nsec to ±0.1% of FS	50 nsec to ±0.1% of FS
OUTPUT RESOLUTION	1 LSB (5 μa for 10 Binary Bits)	1 LSB (5μa for 10 Binary Bits)
LINEARITY	±½ LSB (±2.5 μa for 10 Binary Bits)	±2.5 μA (1/2 LSB)
TEMPERATURE COEFFICIENT	±50 ppm/°C of FS	±30 ppm/°C of FS
LONG TERM STABILITY	±0.5%/Yr.	±0.5%/Yr.
REFERENCE SOURCE	Internal	Internal
INPUT POWER REQUIREMENTS	+15VDC, ±0.5V @ 40 ma -15VDC, ±0.5V @ 20 ma	+15VDC, ±0.5V @ 40 ma -15VDC, ±0.5V @ 20 ma
POWER SUPPLY REJECTION RATIO	0.05%/V	0.05%/V
PHYSICAL – ENVIRONMENTAL		
OPERATING TEMPERATURE RANGE	0° to +70°C	0° to +70°C
STORAGE TEMPERATURE RANGE	−55°C to +85°C	−55°C to +85°C
RELATIVE HUMIDITY	Up to 100% Non-Condensing	Up to 100% Non-Condensing
SIZE	2"L x 2"W x 0.4"H Plug-in Module	2"L x 2"W x 0.4"H Plug-in Module
PINS	0.020" Round Gold Plated 0.250" Long Min.	0.020" Round Gold Plated 0.250" Long Min.
CASE MATERIAL	Black Diallyl Phthalate	Black Diallyl Phthalate
WEIGHT	2 oz.	2 oz.
ORDERING INFORMATION	DAC-FI ⊤ Number of Bits 8 B = 8 Binary Bits 10 B = 10 Binary Bits	DAC-GI ⊤ Number of Bits 8 B = 8 Binary Bits 10 B = 10 Binary Bits

Note: (1) Two's complement bipolar output can be achieved when $\overline{MSB}$ from external storage register or counter, is provided.

Note: (1) Two's complement bipolar output can be achieved when $\overline{MSB}$ from external storage register or counter, is provided.

:-HI SERIES

)ptional
or 10 Binary Bits

traight Binary (Unipolar Output)
)ffset Binary (Bipolar Output)
wo's Complement (Bipolar Output)

)TL or TTL Compatible
ositive Logic
oading: 2 standard TTL loads

.dj. to ±0.05%

urrent

rna @ +1.2V max. (Unipolar)
2.5 ma @ ±1.2V max. (Bipolar) (1)

)0 Ohms ±1%

5 na

)0 ohms for 0 to +1V Output
.325K for ± 1.0V Output

·sec to ±0.1% of FS

LSB (5µa for 10 Binary Bits)

2.5 µA (1/2 LSB)

15 ppm/°C of FS

).5%/Yr.

iternal

15VDC, ±0.5%V @ 40 ma
15VDC, ±0.5%V @ 20 ma

).05%/V

° to +70°C

55°C to +85°C

lp to 100% Non-Condensing

"L x 2"W x 0.4"H
lug-in Module

.020" Round Gold Plated
.250" Long Min.

lack Diallyl Phthalate ·

oz.

DAC-HI
| umber of Bits |
| $B = 8$ Binary Bits |
| 10 B = 10 Binary Bits |

vo's complement bipolar output
an be achieved when $\overline{MSB}$ from
xternal storage register or counter,
5 provided.

CURRENT EQUIVALENT CIRCUIT
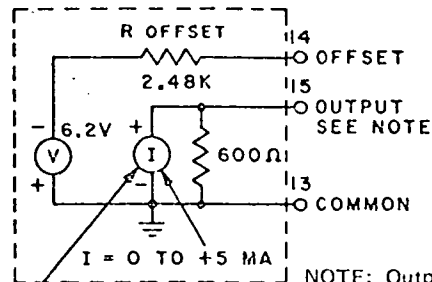
CURRENT CONTROLLED BY
INPUT DIGITAL CODE
I = 0 TO +5 MA

NOTE: Output Voltage
Limited to ±1.2V max.

Figure 1

VOLTAGE EQUIVALENT CIRCUIT
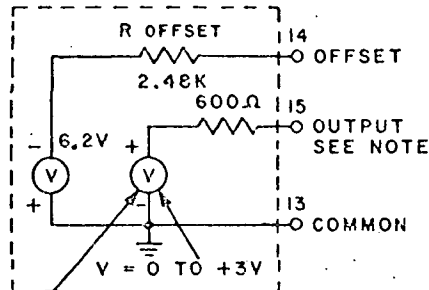
VOLTAGE CONTROLLED BY
DIGITAL INPUT CODE
V = 0 TO +3V

Figure 2

UNIPOLAR CURRENT OUTPUT
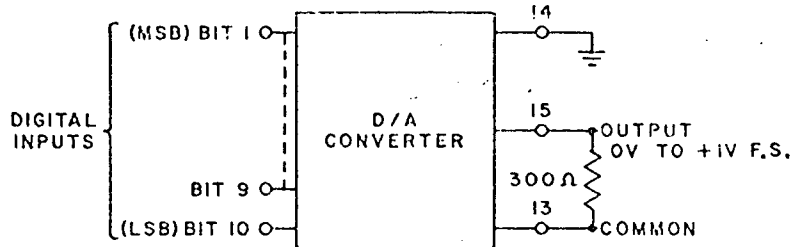
Figure 3

BIPOLAR CURRENT OUTPUT

Connect external
load resistor of 2.32K
Ohms across pins 13
& 15.

Connect a 500 Ohm
potentiometer
between pins 14
& 15 and with input
code of 1000000000,
adjust for zero volts
output.
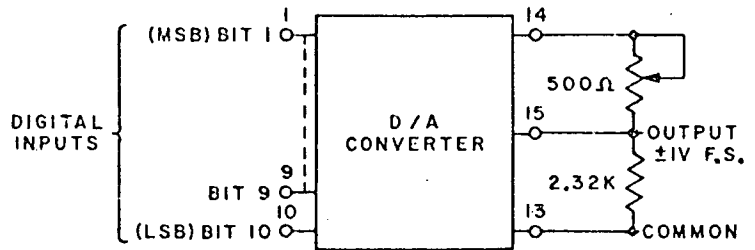
FIGURE FOUR

UNIPOLAR OR BIPOLAR VOLTAGE OUTPUT

For Unipolar voltage
output connect jumper
between pins 13 & 14.
For Bipolar voltage
output connect a 500
Ohm potentiometer
between pins 14 & 15.
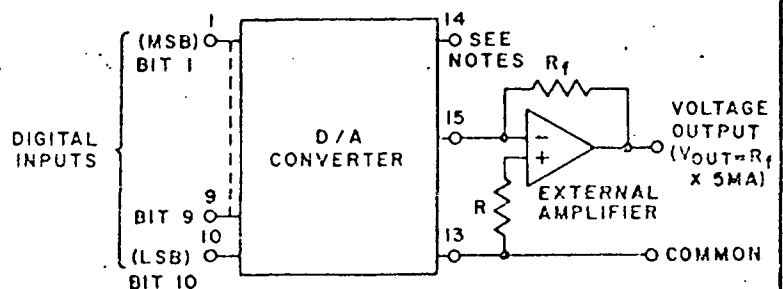
FIGURE FIVE

Input Coding for DAC-FI, DAC-GI and DAC-HI Series

Analog Output Range (±2.5 ma FS)	Offset Binary	2's Complements	Analog Output Range (0 to +5ma FS)	Straight Binary
+2.495	1111111111	0111111111	+4.995	1111111111
+2.187	1111000000	0111000000	+4.375	1110000000
+1.875	1110000000	0110000000	+3.750	1100000000
+1.250	1100000000	0100000000	+2.500	1000000000
0.000	1000000000	0000000000	+1.250	0100000000
−1.250	0100000000	1100000000	+0.625	0010000000
−1.875	0010000000	1010000000	0.000	0000000000
−2.187	0001000000	1001000000		
−2.495	0000000001	1000000001		
−2.500	0000000000	1000000000		

MEASURING OUTPUT SETTLING TIME

Because of the phenomenal output settling time of these devices, great care must be taken when measuring the output performance. Model 454 Tektronix Oscilloscope with low capacitance probe and probe ground lead is recommended for measuring output settling time. Input/Output connections should be made as close as possible to the "DAC" pins. Best results occur when the digital input source has a time skew of less than 5 nanoseconds.

Output settling time for these devices can be defined as that time between application of an input digital word and the analog output settling to ±0.1% of full scale, it includes switch delay, slewing time and final exponential decay time.
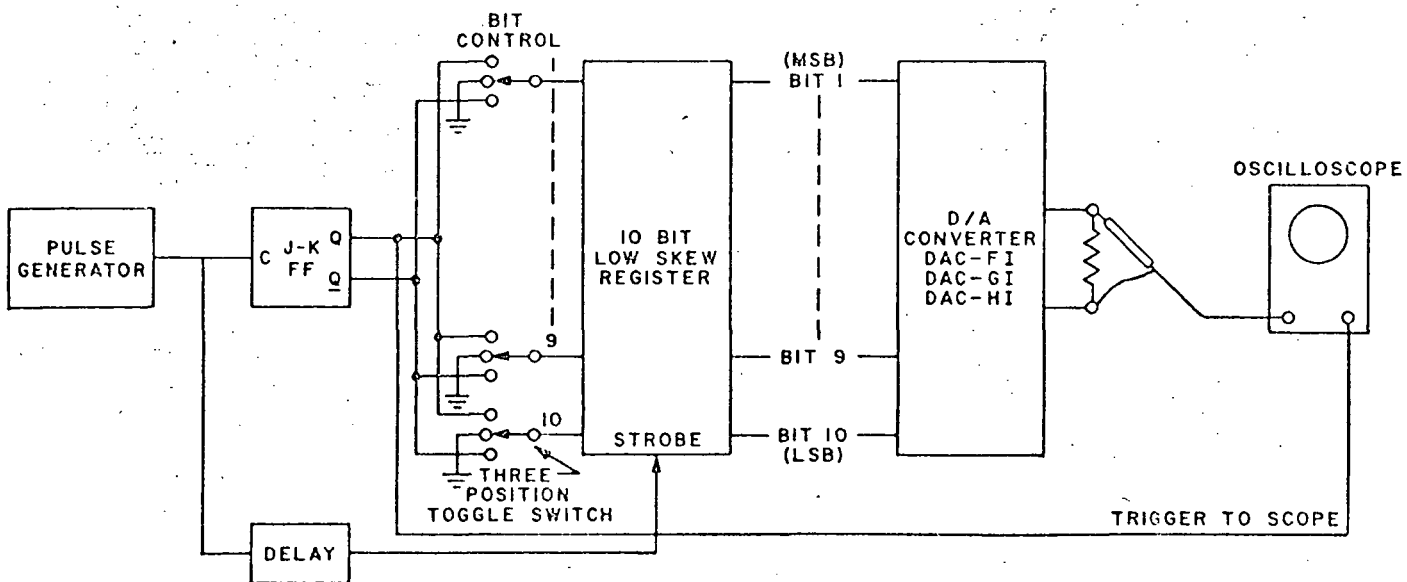
Typical Test Set Up For Measuring Output Settling Time.

MEASUREMENT SYSTEMS, INCORPORATED

X-Y POTENTIOMETER JOYSTICK
Model 525
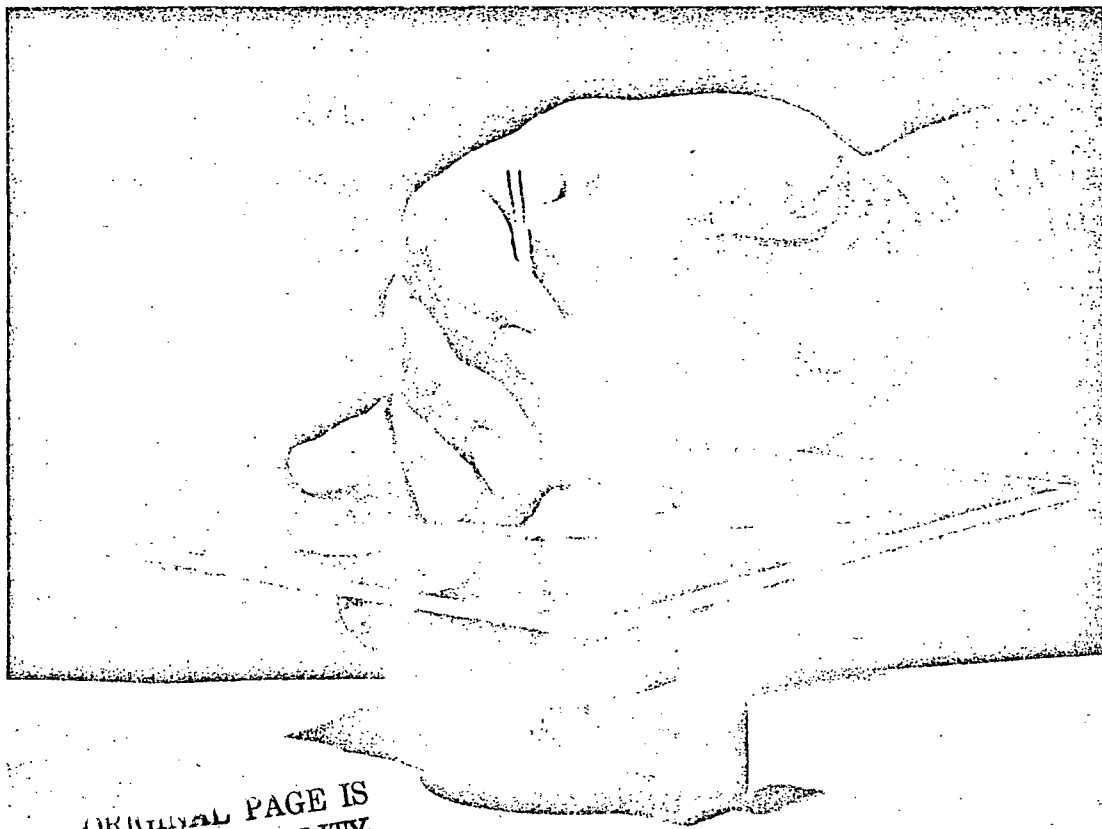
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The Model 525 is a displacement (Isotonic) joystick with potentiometer pick-offs. It is used to control the output of any 2 axis or 2 channel device with electrical inputs. When the control handle is released, the joystick remains in place. It does not return to zero. Actual tracking performance is better than that attainable with geared controls at any price.

ADVANTAGES

Light Weight	High Resolution
Inexpensive	Resistant to Shock and Vibration
Small Size	Corrosion Resistant
Low Static Friction and Backlash	MIL-R-94 Potentiometers

MONOLITHIC DUAL LINE RECEIVERS

The MC55107/MC75107 and MC55108/MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC55107/MC75107 circuit features an active pull-up (totem-pole) output. The MC55108/MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC55108/MC75108 receivers). Thus a level of logic is implemented without extra delay. Both receivers feature double-protected input stages to guard against line loading under zero value supply conditions.

The MC55107/MC75107 and MC55108/MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Diode-Protected Input Stage
- Differential Input Common-Mode Voltage of More Than ±15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins

DUAL LINE RECEIVERS

MONOLITHIC SILICON INTEGRATED CIRCUITS

(top view)

L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

P SUFFIX
PLASTIC PACKAGE
CASE 646
(TO-116)
(MC75107, MC75108 only)

CIRCUIT SCHEMATIC

Components shown with dashed lines are applicable to the MC55107 and MC75107 only.
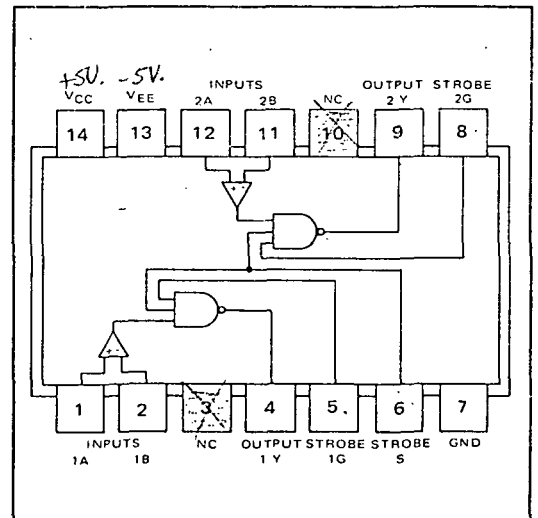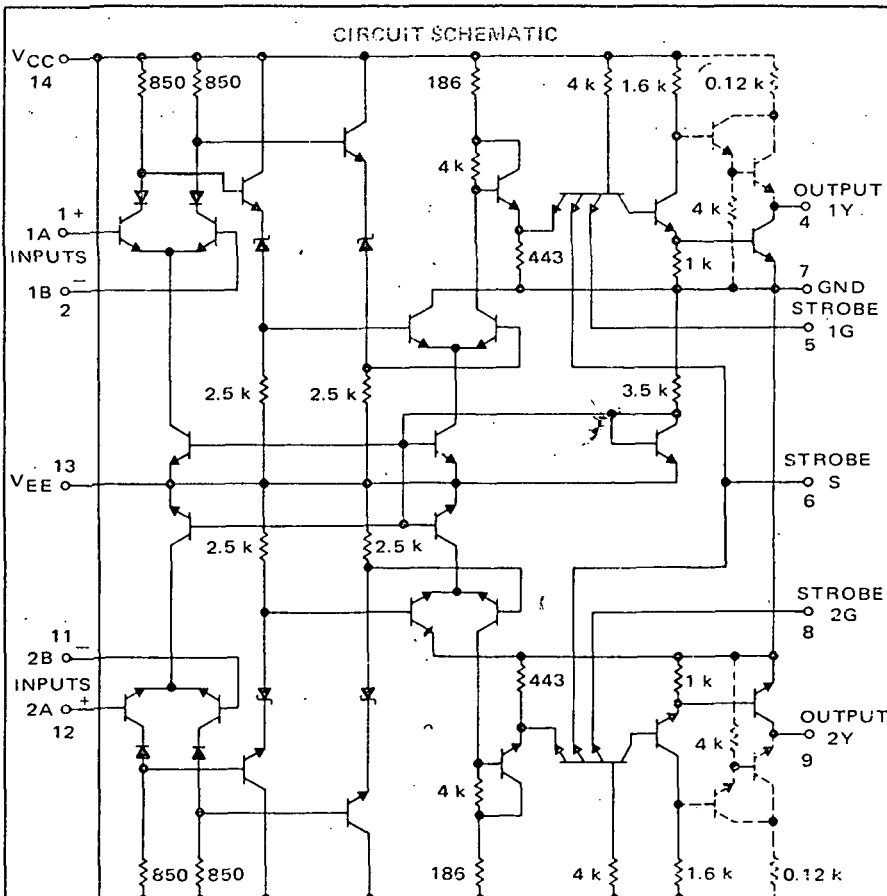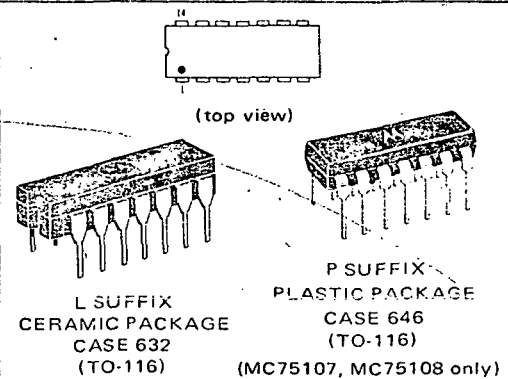
TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25$ mV	L or H	L or H	H
	L or H	L	H
-25 mV $< V_{ID} < 25$ mV	L	L or H	H
	H	H	INDETERMINATE
	L or H	L	H
$V_{ID} \leq -25$ mV	L	L or H	H
	H	H	L

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DS 9192

MAXIMUM RATINGS ($T_A = T_{low}^*$ to T_{high}^* unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 −7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Plastic and Ceramic Dual-In-Line Packages		575	mW
Derate above $T_A = +25^oC$		3.85	mW/^oC
Operating Temperature Range MC55107, MC55108 MC75107, MC75108	T_A	−55 to +125 0 to +70	^oC
Storage Temperature Range	T_{stg}	−65 to +150	^oC

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	MC55107, MC55108			MC75107, MC75108			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltages	V_{CC} V_{EE}	+4.5 −4.5	+5.0 −5.0	+5.5 −5.5	+4.75 −4.75	+5.0 −5.0	+5.25 −5.25	Vdc
Output Sink Current	I_{OS}	−	−	−16	−	−	−16	mA
Differential-Mode Input Voltage Range	V_{IDR}	−5.0	−	+5.0	−5.0	−	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	−3.0	−	+3.0	−3.0	−	+3.0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	−5.0	−	+3.0	−5.0	−	+3.0	Vdc
Operating Temperature Range	T_A	−55	−	+125	0	−	+70	^oC

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0.025	5.0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	−5.0†	−0.025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2.0	5.5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL}).

ELECTRICAL CHARACTERISTICS ($T_A = T_{low}^*$ to T_{high}^* unless otherwise noted)

Characteristic	Symbol	Test Fig.	MC55107,MC75107			MC55108,MC75108			Unit
			Min	Typ #	Max	Min	Typ #	Max	
High-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = 0.5 V, V_{IC} = −3.0 V to +3.0 V) ‡	I_{IH}	2	−	30	75	−	30	75	µA
Low-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = −2.0 V, V_{IC} = −3.0 V to +3.0 V) ‡	I_{IL}	2	−	−	−10	−	−	−10	µA
High-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V) ‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max) ‡	I_{IH}	4	− −	− −	40 1.0	− −	− −	40 1.0	µA mA
Low-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V) ‡	I_{IL}	4	−	−	−1.6	−	−	−1.6	mA
High-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V) ‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max) ‡	I_{IH}	4	− −	− −	80 2.0	− −	− −	80 2.0	µA mA
Low-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V) ‡	I_{IL}	4	−	−	−3.2	−	−	−3.2	mA
High-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{load} = −400 µA, V_{IC} = −3.0 V to +3.0 V) ‡	V_{OH}	3	2.4	−	−	−	−	−	V
Low-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{sink} = 16 mA V_{IC} = −3.0 V to +3.0 V) ‡	V_{OL}	3	−	−	0.4	−	−	0.4	V
High-Level Leakage Current (V_{CC} = Min, V_{EE} = Min, V_{OH} = V_{CC} Max) ‡	I_{CEX}	3	−	−	−	−	−	250	µA
Short-Circuit Output Current # # (V_{CC} = Max, V_{EE} = Max) ‡	I_{OSC}	5	−18	−	−70	−	−	−	mA
High Logic Level Supply Current from V_{CC} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25^oC) ‡	I_{CCH^+}	6	−	18	30	−	18	30	mA
High Logic Level Supply Current from V_{EE} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25^oC) ‡	I_{CCH^-}	6	0	−8.4	−15	0	−8.4	−15	mA

‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

#All typical values are at V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = +25^oC.

#Not more than one output should be shorted at a time.

*T_{low} = −55^oC for MC55107 and MC55108, T_{high} = +125^oC for MC55107 and MC55108
= 0 for MC75107 and MC75108 = +70^oC for MC75107 and MC75108

## SWITCHING CHARACTERISTICS (V$_{CC}$ = +5.0 V, V$_{EE}$ = −5.0 V, T$_A$ = +25°C)

Characteristic	Symbol	Test Fig.	MC55107, MC75107			MC55108, MC75109			Unit
			Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time, low-to-high level from differential inputs A and B to output	tPLH(D)	7							ns
(R$_L$ = 390 Ω, C$_L$ = 50 pF)			−	17	25	−	−	−	
(R$_L$ = 390 Ω, C$_L$ = 15 pF)			−	−	−	−	19	25	
Propagation Delay Time, high-to-low level from differential inputs A and B to output	tPHL(D)	7							ns
(R$_L$ = 390 Ω, C$_L$ = 50 pF)			−	17	25	−	−	−	
(R$_L$ = 390 Ω, C$_L$ = 15 pF)			−	−	−	−	19	25	
Propagation Delay Time, low-to-high level, from strobe input to G or S output	tPLH(S)	7							ns
(R$_L$ = 390 Ω, C$_L$ = 50 pF)			−	10	15	−	−	−	
(R$_L$ = 390 Ω, C$_L$ = 15 pF)			−	−	−	−	13	20	
Propagation Delay Time, high-to-low level, from strobe input G or S to output	tPHL(S)	7							ns
(R$_L$ = 390 Ω, C$_L$ = 50 pF)			−	8.0	15	−	−	−	
(R$_L$ = 390 Ω, C$_L$ = 15 pF)			−	−	−	−	13	20	

Symbols conform to JEDEC Bulletin No. 1 when applicable.

TEST CIRCUITS

FIGURE 1 – V$_{IDH}$ and V$_{IDL}$
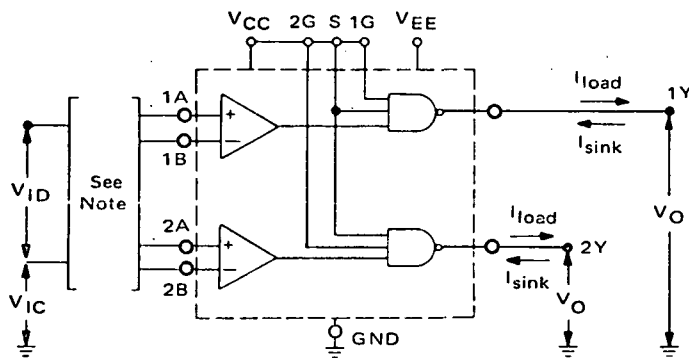
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I$_{IH}$ and I$_{IL}$
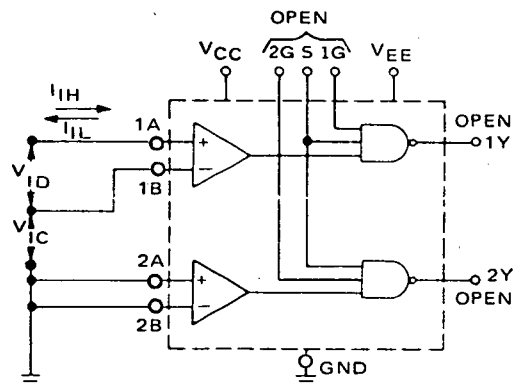
NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded

FIGURE 3 – V$_{IH(S)}$, V$_{IL(S)}$, V$_{OH}$, V$_{OL}$, and I$_{OH}$
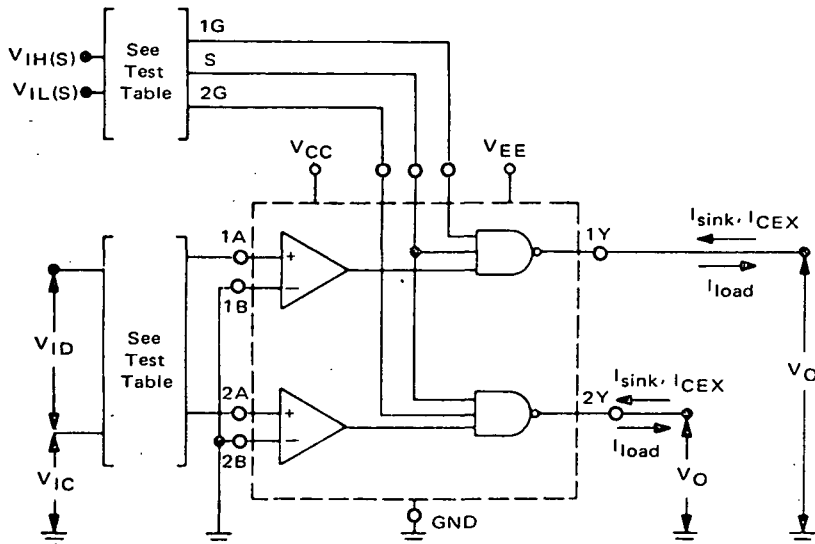
MC55107 MC75107	MC55108 MC75108	V$_{ID}$	STROBE 1G or 2G	STROBE S
TEST			APPLY	
V$_{OH}$	I$_{CEX}$	+25 mV	V$_{IH(S)}$	V$_{IH(S)}$
V$_{OH}$	I$_{CEX}$	−25 mV	V$_{IL(S)}$	V$_{IH(S)}$
V$_{OH}$	I$_{CEX}$	−25 mV	V$_{IH(S)}$	V$_{IL(S)}$
V$_{OL}$	V$_{OL}$	−25 mV	V$_{IH(S)}$	V$_{IH(S)}$

NOTES: 1. V$_{IC}$ = −3.0 V to +3.0 V.
2. When testing one channel, the inputs of the other channel should be grounded.

MOTOROLA Semiconductor Products Inc.

TEST CIRCUITS (continued)
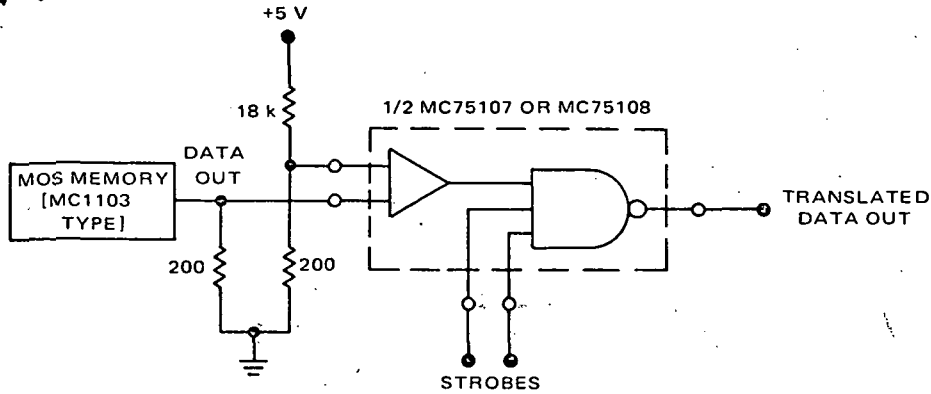
FIGURE 7 — PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
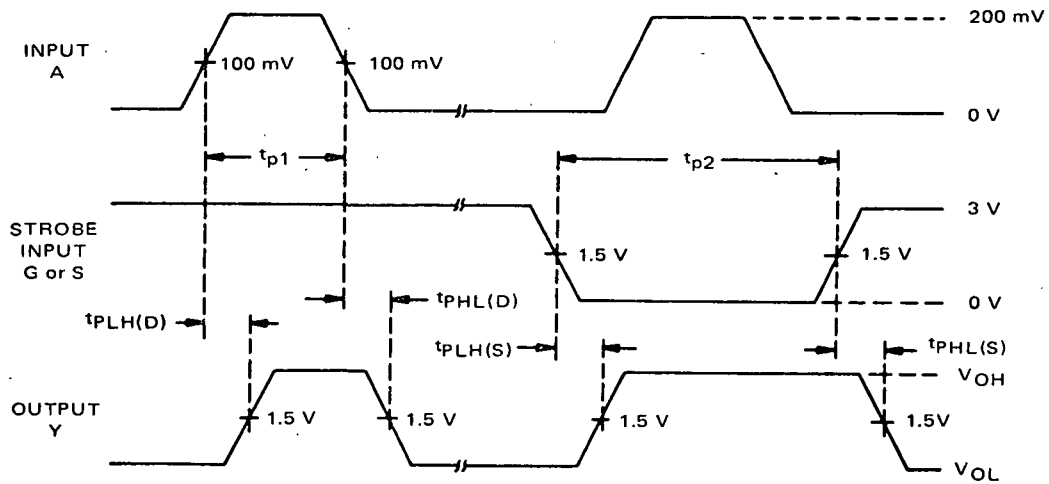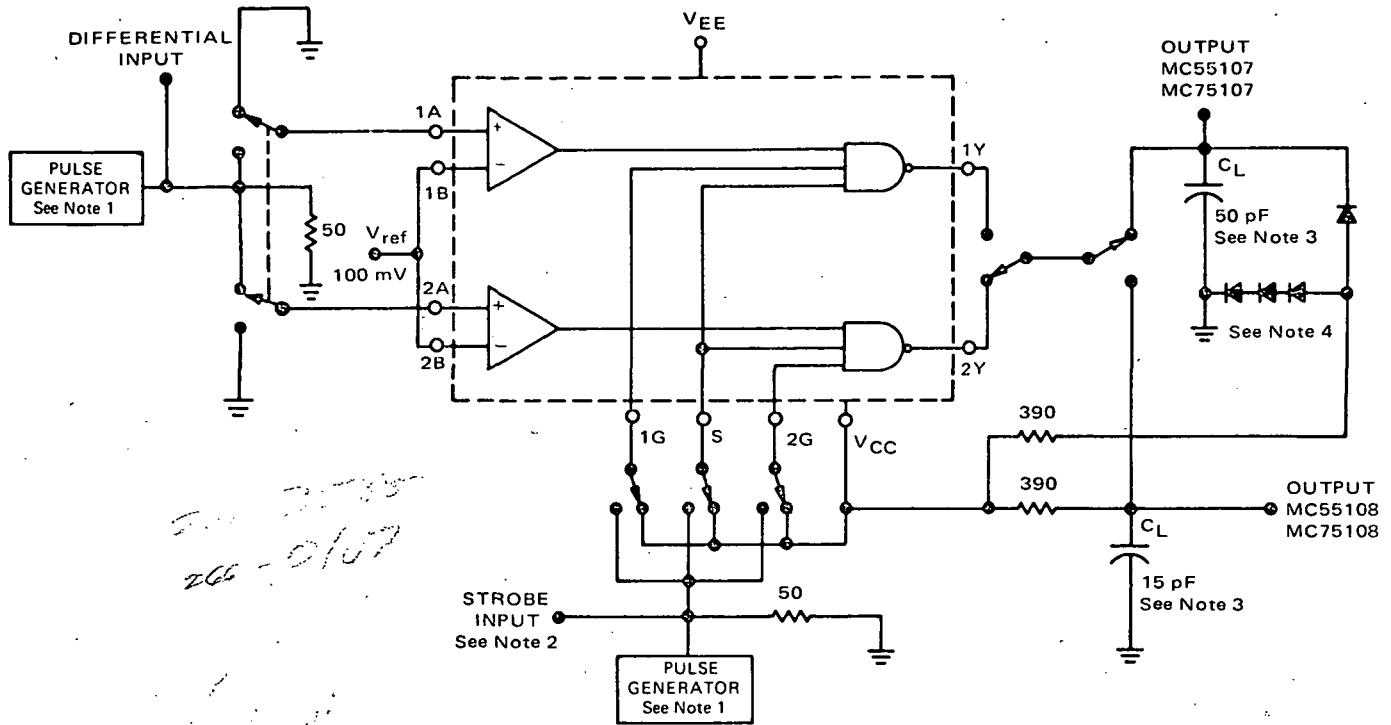
NOTES:
1. The pulse generators have the following characteristics: $z_0 = 50\,\Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1$ ms, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

TYPICAL APPLICATION

FIGURE 8 — MOS-TO-TTL TRANSLATOR

ORIGINAL PAGE IS OF POOR QUALITY

+5 V

18 k

MOS MEMORY (MC1103 TYPE)

DATA OUT

200   200

1/2 MC75107 OR MC75108

TRANSLATED DATA OUT

STROBES

OUTLINE DIMENSIONS
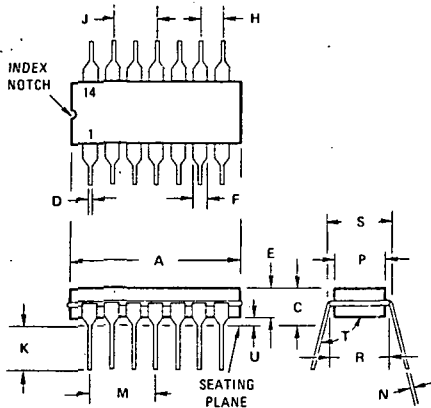
Weight ≈ 1.954 grams

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.660	0.780	17.400	19.900
C	–	0.200	–	5.080
D	0.015	0.023	0.381	0.584
F	0.030	0.070	0.770	1.770
H	0.090	0.110	2.290	2.790
J	0.190	0.210	4.830	5.330
K	0.100	–	2.540	–
M	0.290	0.310	7.370	7.870
N	0.008	0.015	0.203	0.381
P	0.220	0.280	5.590	7.110
R	0.290	0.310	7.370	7.870
S	–	0.325	–	8.260
T	90°	105°		
U	0.020	0.030	0.508	0.762

NOTE:
1. "R" – Installed Position of Lead Centers.
2. "S" – Overall Installed Width.

All JEDEC TO-116 dimensions and notes apply.

L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)
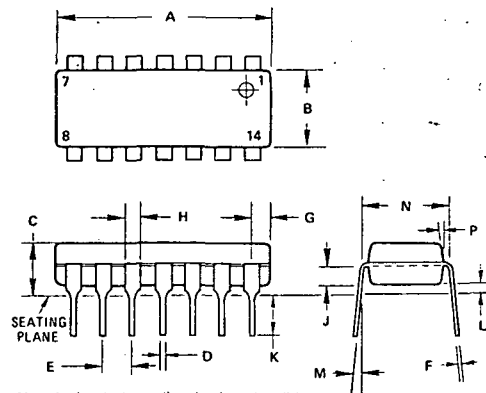
*Dimension is to lead centerline when formed parallel.
All JEDEC dimensions and notes apply.

Weight ≈ 0.911 gram

1. DIM "N" TO LEAD CENTERLINE WHEN FORMED PARALLEL.

| DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.710	0.740	18.030	18.790
B	0.240	0.260	6.090	6.600
C	0.160	0.180	4.060	4.570
D	0.015	0.020	0.381	0.508
E	0.100 T P		2.54 T P	
F	0.009	0.014	0.228	0.355
G	0.060	0.080	1.520	2.030
H	0.040	0.065	1.020	1.650
J	0.062	0.072	1.570	1.830
K	0.115	0.135	2.920	3.430
L	0.025	0.035	0.635	0.889
M	0°	10°	0°	10°
N	0.290	0.310	7.360	7.870
P	7° TYP		7° TYP	

P SUFFIX
PLASTIC PACKAGE
CASE 646
(TO-116)

© MOTOROLA INC., 1972

DATEL SYSTEMS, INC.
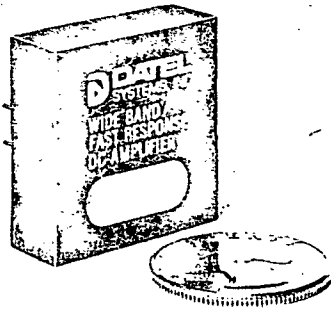
WIDE BAND FAST RESPONSE DIFFERENTIAL FET OPERATIONAL AMPLIFIERS

AM-100 SERIES

DESIGNED SPECIFICALLY FOR HIGH SPEED APPLICATIONS

MODEL AM-100 A/B/C

DESCRIPTION:
Designed specifically to drive C.R.T. displays the DATEL Models AM-100-A/B/C permit settling (to 0.01%) of a 0.5 V step within 0.15 usec. Clean, crisp alpha/numeric characters, together with sharp, linear vectors are the result on the screen face when these amplifiers with their fast settling, true 6B/octave response and minimum overshoot and undershoot characteristics are used. These devices are also excellent choices for use in high speed applications such as D/A output drivers, integrators, comparators, buffers and many other analog sampling circuits.

FEATURES:
- ☐ 60 Volts/μsec. Slew Rate
- ☐ Settles to 0.01% Within 0.15 μsec. (Small Step)
- ☐ Recovery From Overload in 0.5 μsec.
- ☐ Gain of 500,000
- ☐ 10^{12} Ω Differential Input Resistance
- ☐ True 6 dB/Octave Response

MODEL AM-101 A/B

DESCRIPTION:
Models AM-101A/B is a FET-input differential operational amplifier designed specifically for applications requiring a combination of high accuracy, high gain and fast settling with the ability to drive substantial capacitive loads. They have a gain bandwidth product of 5 MHz and will settle to 0.01% within 1.5 u sec., min. in a unity gain inverting mode while driving a capacitive load of 300 picofarads. These amplifiers will settle to 0.01% within 2 u sec., min., in the same mode driving a 1000 picofarad load and are stable driving a load of 2000 picofards, minimum. Typically they are stable up to 5,000 picofarads. In addition, low drift, low noise and excellent overload recovery characteristics together with a reasonable price make these amplifiers a must to consider wherever analog voltage sampling is required.

Model AM-101 A/B has a CMRR of 40,000 typical and 20,000 minimum and should be considered wherever a non-inverting amplifier is necessary such as in buffer or multiplexer applications. Since settling time to 0.01% is approximately the same in the non-inverting mode excellent gain and linearity characteristics are achieved with the high CMRR of the AM-101 Series.

FEATURES:
- ☐ Will drive high capacitive load .... 2000 pF, min.
- ☐ Gain Bandwidth Product .... 5 MHz, min.
- ☐ D.C. Gain at Rated Load .... 300,000, min.
- ☐ Differential Input Resistance .... 10^{12} Ω min.
- ☐ Output .... ±10 V @ ±20 mA, min.
- ☐ CMRR .... 20,000, min.
- ☐ Fast Overload Recovery Time .... 1 usec
- ☐ Low Profile Case .... 0.4"
- ☐ Low Cost .... From $46 ea.

MODEL AM-102 A/B

DESCRIPTION:
The Model AM-102 A/B is a differential FET input fast settling operational amplifier designed primarily for use in circuits where polarity reversal is not desired. All the ingredients of a good, fast and accurate FET Follower can be found in the AM-102 A/B. High CMRR, very high common mode resistance, high gain, wide bandwidth and fast settling along with high input impedance, excellent drift and noise characteristics all combine to make the AM-102 A/B one of the best all around Follower Amplifiers available today.

FEATURES:
- ☐ 100 Volts/μsec. Slew Rate
- ☐ 0.6 μsec, Settling Time to 0.01% as Follower
- ☐ 1 μsec. Overload Recovery Time
- ☐ 100,000 Gain at Rated Load
- ☐ 30 MHz Gain Bandwidth Product

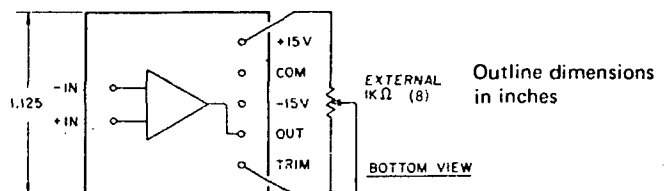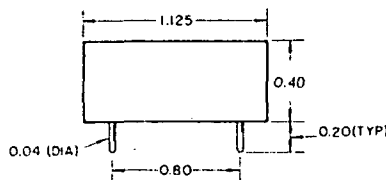## MODEL AM-103 A/B

DESCRIPTION:
The fastest yet of the DATEL Systems operational amplifiers, the AM-103 A/B features a 250 Volt per microsecond slew rate, a guaranteed 0.4 microsecond settling time (to 0.01%), an overload recovery time of 1 microsecond, max. together with a minimum gain of 100,000. Designed especially for use in high speed comparators, integrator A/D and D/A converter circuits the AM-103 A/B is an excellent choice for consideration whenever analog sampling is necessary.

FEATURES:
- ☐ 250 Volts/μsec. Slew Rate, Min.
- ☐ Settles to 0.01% Within 0.4 μsec., Max.
- ☐ Recovery From Overload in 1 μsec., Max.
- ☐ Gain of 100,000, Min.
- ☐ 10^{12} Differential Input Resistance
- ☐ Stable Unity Gain Frequency 30 MHz, Min.

MECHANICAL DIMENSIONS

Outline Dimensions in inches

1.125
0.40
0.04 (DIA)
0.20 (TYP)
0.80

+15V
COM
-15V
OUT
TRIM
-IN
+IN
1.125
EXTERNAL 1KΩ (8)
Outline dimensions in inches
BOTTOM VIEW

SPECIFICATIONS	MODEL AM-100			MODEL AM-101			MODEL AM-102			MODEL AM-103		
	A	B	C	A	B		A	B		A	B	
	DIFFERENTIAL I/P IN VAN USEC			FAST SETTLING FET I/P AMPS			FAST POWER AMP			FAST VIDEO AMP		
Differential Voltage	±15V (5)			±15V (5)			±15V (5)			±15V (5)		
Common Mode Voltage	±18V (7)			±18V (7)			±18 (7)			±18V (7)		
Common Mode Rejection Ratio	10,000 (5)			40,000 (5)			40,000 (5)			10,000 (5)		
Common Mode Resistance	$10^{12} \Omega$ (6)			$10^{12} \Omega$ (6)			$10^{12} \Omega$ (6)			$10^{12} \Omega$ (6)		
Differential Input Resistance	$10^{12} \Omega$ (6)			$10^{12} \Omega$ (6)			$10^{12} \Omega$ (6)			$10^{12} \Omega$ (6)		
Voltage	±10V (6)			±10V (6)			±10V (6)			±10V (6)		
Current, Continuous	±20mA (6)			±20mA (6)			±20mA (6)			±20mA (6)		
Current, Transient	±30mA (5)			±30mA (5)			±30mA (5)			±30mA (5)		
Capacitive Load	300 pF			5000 pF			300 pF			300 pF		
D.C. Gain at Rated Load	500,000 (5)			500,000 (5)			400,000 (5)			400,000 (5)		
Gain Bandwidth Product	18 MHz (5)			7 MHz (5)			45 MHz (5)			45 MHz (5)		
Stable Unity Gain Frequency	18 MHz (5)			7 MHz (5)			37 MHz (5)			37 MHz (5)		
Full Power Response	900 KHz (1)(5)			900 KHz (1)(5)			2 MHz (2)(5)			6 MHz (1)(5)		
Slew Rate	60V/us. (1)(5)			60V/us. (1)(5)			140V/us. (2)(5)			400V/us. (1)(5)		
Settling Time to 0.01%	0.4 us. (1)(5)			1 us. (1)(5)			0.4 us. (2)(5)			0.3 us. (1)(5)		
Settling Time to 0.01%	0.15 us. (3)(5)			1.5 us. (4)(5)								
Overload Recovery Time	0.5 us. (5)			1 us. (5)			0.5 us. (5)			0.5 us. (5)		
Rise Time to 90% (Small Signal)	50 ns. (1)(5)			100 ns. (1)(5)			20 ns. (2)(5)			20 ns. (1)(5)		
Offset Voltage (Initial) @ 25°C	Adj. to 0			Adj. to 0			Adj. to 0			Adj. to 0		
Vs. Temp. Range -25°C to +85°C, µV/°C	50 (7)	25 (7)	10 (7)	40 (7)	20 (7)		40 (7)	20 (7)		40 (7)	20 (7)	
Vs. Power Supply	±10uV/% (5)			±10uV/% (5)			±10uV/% (5)			±10uV/% (5)		
Vs. Time	±50uV/day (5)			±50uV/day (5)			±50uV/day (5)			±50uV/day (5)		
Input Offset Current	±10pA (7)			±10pA (7)			±10pA (7)			±10pA (7)		
Bias Current @ 25°C, pA	100 (7)	50 (7)	20 (7)	50 (7)	20 (7)		50 (7)			50 (7)		
Vs. Temperature Range -25°C to +85°C	Doubles every 10°C			Doubles every 10°C			Doubles every 10°C			Doubles every 10°C		
Input Noise (Voltage)	25nV $\sqrt{Hz}$ (5)			25nV $\sqrt{Hz}$ (5)			25nV $\sqrt{Hz}$ (5)			25nV $\sqrt{Hz}$ (5)		
Operating Voltage Range	±15V (5)			±15V (5)			±15V (5)			±15V (5)		
Quiescent Current	±13mA (7)			±13mA (7)			±18mA (7)			±18mA (7)		
Operating	-25 to +85°C			-25 to +85°C			-25 to +85°C			-25 to +85°C		
Storage	-55 to +125°C			-55 to +125°C			-55 to +125°C			-55 to +125°C		
	1.12"L x 1.12"W x 0.4"H			1.12"L x 1.12"W x 0.4"H			1.12"L x 1.12"W x 0.4"H			1.12"L x 1.12"W x 0.4"H		
	MS-9 $2.00 ea.			MS-9 $2.00 ea.			MS-9 $2.00 ea.			MS-9 $2.00 ea.		
	$40	$45	$52	$46	$52		$49	$55		$49	$55	

NOTES: (1) Unity gain inverting. (2) As Follower. (3) Unity gain inverting 0.5 volt step. (4) Unity gain inverting with 1000pF capacitive load
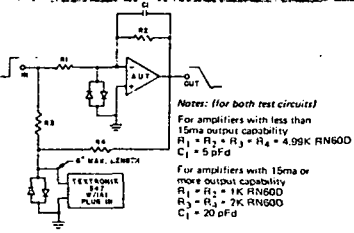(5) Typical (6) Minimum (7) Maximum. (8) Ext. balance pot, Model TP-1K — $3.00 ea.

SETTLING TIME

Settling time is one of the most important requirements an amplifier should meet for high speed applications. It is defined as the time that is required, after a full scale input step is applied, for the output voltage to reach a predetermined percentage of its final value. Settling time contributes a dynamic error. It characterizes the transient behavior of the amplifier, encompassing slew rate and other important effects. For high speed data system applications, the output signal should be within a specified error band before it is ready to be further processed. In all applications involving abrupt changes in gradient, the settling characteristics of an amplifier determine how long the output signal deviates from the true value and should be a prime consideration for its selection.
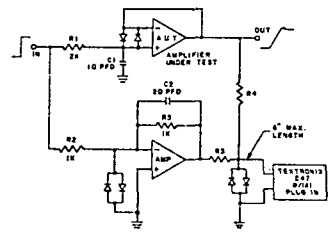
Settling time is a complex function of the open loop response and slewing rate under operating conditions. For optimum settling characteristics, the DATEL amplifiers have true 6 dB/octave stabilization determined by a single component instead of the usual multielement response shaping which introduces irregularities in the response curve.
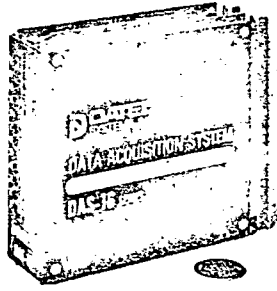
Test circuits for measuring a settling time in both the inverting and non-inverting modes are shown. The test circuits are self explanatory but it is wise to keep the leads short, stray capacitance to a minimum and use a signal source that is a good clean square wave with minimum averations. The oscilloscope and plug-in recommended in the test circuit will, in general, give good results on amplifiers with settling times of 1 microsecond or less. Many oscilloscopes of other types will introduce errors far in excess of the amplifier errors due to the overload condition to which they are subjected by this method of measurement.

SETTLING TIME TEST CIRCUIT FOR INVERTING AMPLIFIERS

Notes: (for both test circuits)
For amplifiers with less than 15ma output capability
R_1 = R_2 = R_3 = 4.99K RN60D
C_1 = 5 pFd
For amplifiers with 15ma or more output capability
R_1 = R_2 = 1K RN60D
R_3 = 2K RN60D
C_1 = 20 pFd

SETTING TIME TEST CIRCUIT FOR NON-INVERTING AMPLIFIERS

DATEL
SYSTEMS, INC.

MODULAR
16 CHANNEL
DATA ACQUISITION
SYSTEM
DAS-16 SERIES

FEATURES

☐ Small Size . . . . 1.5" x 4.5" x 5.0"
☐ Complete . Simply Apply D.C. Power
☐ Two Modes
   of Operation . . Random or Sequential
☐ High Input Impedance . . . 100M ohm
☐ Low Power
   Consumption . . . . . Less than 7 Watts
☐ Fast Throughput Rate Up to 100 KHz.
☐ High Resolution   Up to 12 Binary Bits
☐ Variety of
   Output Formats . . . . . Binary or BCD

TYPICAL APPLICATIONS

☐ Air Pollution Data Gathering and
   Analysis

☐ Automatic Testing of Components

☐ Meteorological Data Gathering

☐ Biomedical Data Gathering and
   Monitoring

☐ Geophysical Testing

☐ Chemical Process Analysis and Con-
   trol

☐ Telemetry Data Reduction

☐ Oceanographic Data Logging

NEW CATALOG
A/D — D/A CONVERTERS

A comprehensive 12 page catalog de-
scribes in detail a new line of ultra-
miniature A/D and D/A converters
and accessories.

Write or call for immediate receipt of
this catalog.

DATEL
SYSTEMS, INC.

A/D

D/A

CONVERTERS

DAS-16 Applications handbook
available upon request

FIRST SYSTEM IN A MODULE PRICED FROM $395. EA.

GENERAL DESCRIPTION

Datel Systems proudly announces a new approach to the Data Acquisition
System, a "Complete Data Acquisition module", occupying only 34 cubic inches
and weighing less than 18 oz. Through the use of MOS and Monolithic circuits
and unique packaging techniques, Datel has significantly reduced the size
over competitive systems, at the same time reducing cost.

System DAS - 16 was designed primarily to interface directly with most
mini-computers available on the market today. For real time data logging,
System DAS - 16 can be interfaced to printers, paper tape punches, solid state or
core memory and magnetic tape recorders.

DAS - 16 contains an eight or sixteen channel Multiplexer, Sample & Hold
amplifier Analog to Digital converter, System Sequencer which includes all
necessary control and interface logic and a solid state readout, displaying
multiplexer address and the analog to digital output value.

Random and Sequential addressing is employed to enhance system flexibility.
Mode selection is determined by external control signals. Individual channels
may be sampled at rates consistent with their particular bandwidth.

DAS-16 is available with input ranges of 0to+5V, 0 to +10V, ± 5V, or ± 10V at
an input impedance of 100 megohms. Overall accuracy is ± 0.05% with a
temperature coefficient of ± 40 ppm/°C. DAS - 16 will operate over an operating
temperature range of 0° to +70°C. Gain and offset adjustments are provided,
however long term stability is excellent, so it will seldom be necessary to
readjust the external gain and offset trims once the initial adjustments are made.

Output coding can be Binary or BCD with word lengths of 8, 10, 12 Binary bits
or 3 digit BCD. System throughput rates are available up to 100 KHz (8 Binary
bits), 60 KHz (10 Binary bits), and 50 KHz (12 Binary bits).

Input control lines consist of "Device Select" (1 line), "Random or Sequential"
(1 line), "Channel Address" (4 lines), "Convert Command" (1 line), "Reset" (1
line), and "Strobe" (1 line). The "Device Select" signal inhibits all input
commands, therefore, allowing the system to be multiplexed with other
peripherals tied into the computer.The"Strobe"input is used to "lock" in all of
the commands that are "True" on the inputs during strobe time, therefore, it is
not necessary to hold the commands except during strobe time. All control
inputs are buffered and present one TTL input load. All inputs are "negative
true", consistent with transfer gated computer output. All data outputs are
"True" when the "Busy output" is False, i.e., not digitizing.

WHO WILL USE DAS - 16

The tremendous expansion in the data acquisition market has been mainly
brought about by the advent of the "mini-computer".

Anyone in the data processing, data analysis, data utilization, research,
measurement, and control business, needs or will soon need DAS - 16.
Applications include measuring, studying, and generating data in analog form.
This includes variables like pressure, temperature, force, position, velocity, and
voltage that are continuous.

An engineer wants to utilize DAS-16 for converting analog data to digital codes
for three reasons:

   1.)   He wants to do some computer analysis, and computers require
        numerical form such as binary digital codes for input.

   2.)   He wants to do some telemetering or transmission of the data.

   3.)   He wants to store multi-channel data for a long period without
        degrading it, and the output of DAS - 16 can be stored in cores, tape
        memories or most other storage media.

Sooner or later most every data processor is going to want to convert
multi-channel analog data to digital. DAS - 16 has tremendous appeal, since it is
low cost, small size and easily adaptable to peripheral devices.

MODES OF OPERATION

The input analog signals may be multiplexed for digitizing in a sequential or random manner. Mode selection is determined by control signals and by hard-wire jumpers (sequential mode for channel short cycle).
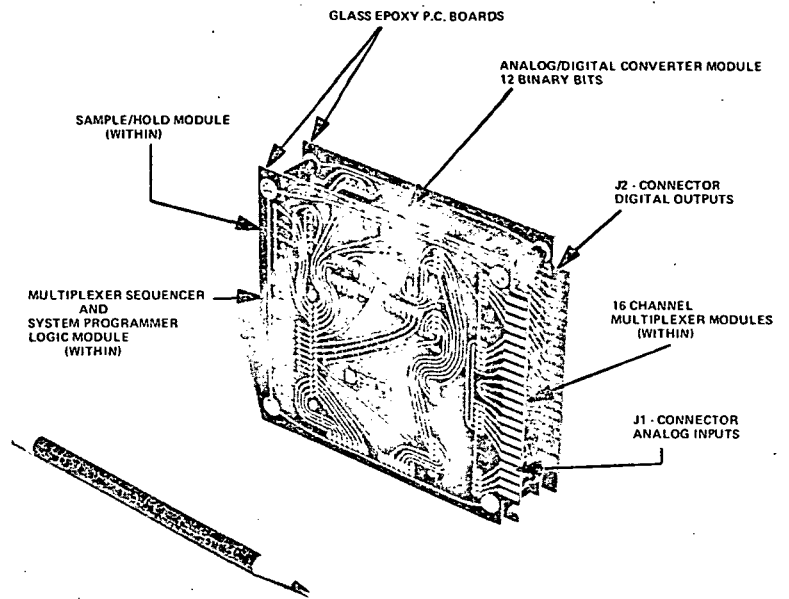
Sequential Mode

In the "Sequential Mode", analog multiplexing is controlled by an internal binary counter. When the "Busy" signal of the analog to digital converter goes false the sequential counter is advanced to the next channel. A 5 μsec delay is necessary before converting, this allows for Multiplexer and Sample/Hold settling time. The last channel to be sequenced is determined by hard wiring, the short cycle inputs to the sequencer counter outputs. If the full 16 channels are to be utilized the short cycle feature need not be used.

Random Mode

In the "Random Mode" any of the 16 channels may be addressed in any order.

When the "Device Select" signal is true and a "Strobe" is generated with the appropriate binary code on the channel address inputs, a channel will be selected. As in the case in Sequential mode, a delay of 5 μsec is necessary before giving a "Convert" command. This is to allow for settling time of the Multiplexer and Sample/Hold. When the Busy signal goes to False a new channel may be selected.

GLASS EPOXY P.C. BOARDS

ANALOG/DIGITAL CONVERTER MODULE 12 BINARY BITS

SAMPLE/HOLD MODULE (WITHIN)

J2 - CONNECTOR DIGITAL OUTPUTS

MULTIPLEXER SEQUENCER AND SYSTEM PROGRAMMER LOGIC MODULE (WITHIN)

16 CHANNEL MULTIPLEXER MODULES (WITHIN)

J1 - CONNECTOR ANALOG INPUTS

DATA ACQUISITION SYSTEM
MODEL DAS-N-L12B2D4B

TYPICAL SYSTEM CONFIGURATION
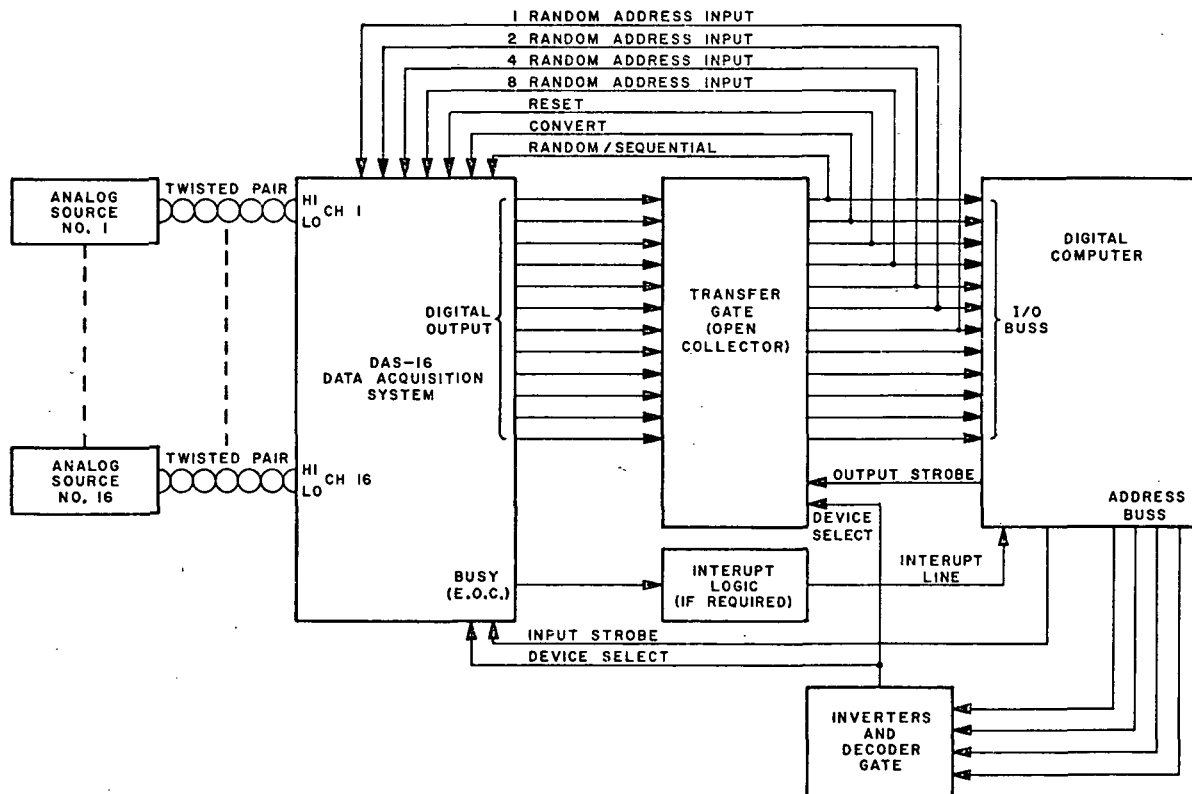
BLOCK DIAGRAM
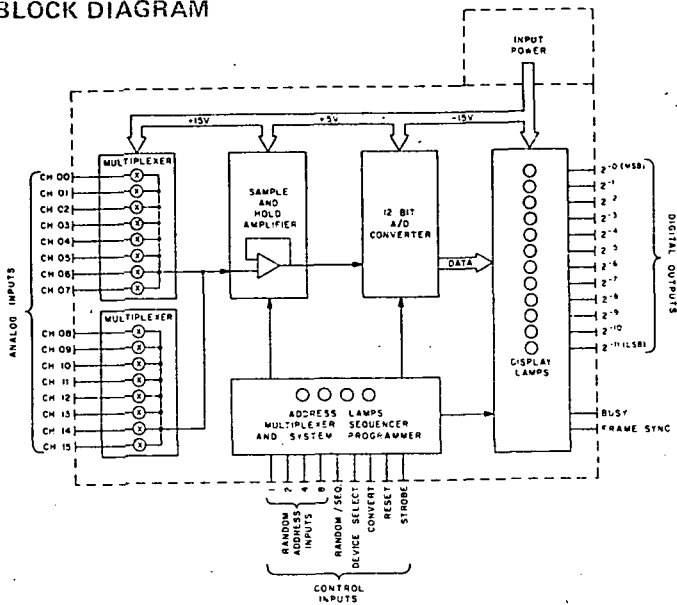
MULTIPLEXER

It contains 16 MOS-FET switches with associated driver circuits, each having a current limiter pull-up FET to provide minimum propagation delay, also, included is all the necessary decoding logic for channel selection.

SAMPLE AND HOLD

Basic elements are a high input impedance non-inverting amplifier, a sample and hold FET switch/holding capacitor and a high gain output amplifier.

ANALOG TO DIGITAL CONVERTER

The A/D contains a programmer/output register, a precision D/A Converter, high-speed voltage comparator and an operational temperature compensated voltage reference source. A modified successive approximation technique is employed which allows for encoding speeds of 750 nsec/bit.

SYSTEM PROGRAMMER

It contains a sequential and random addressable register or counter, interface logic for strobing random or sequential operation, and all necessary logic to be addressed by the output of a mini-computer.

DISPLAY

Both input channels and A/D output value are displayed by sixteen gallium phosphide red light-emitting diodes.

MODEL	DAS–16–L8B	DAS–16–L10B	DAS–16–L12B	DAS–16–L8D	DAS–16–L12D	DAS–16–M8B	DAS–16–M10B	DAS–16–M12B	DAS–16–M8D	DAS–16–M12D
SYSTEM OUTPUT RESOLUTION (DTL/TTL COMPATIBLE)	8 Binary Bits	10 Binary Bits	12 Binary Bits	2 Digits BCD	3 Digits BCD	8 Binary Bits	10 Binary Bits	12 Binary Bits	2 Digits BCD	3 Digits BCD
NUMBER OF ANALOG INPUTS	8(16 opt.)	8(16 opt.)	8(16 opt.)	8(16 opt.)	8(16 opt.)	8(16 opt.)	8(16 opt.)	8(16 opt.)	8(16 opt.)	8(16 opt.)
AVAILABLE INPUT VOLTAGE RANGES		+5V, +10V ±5V, ±10V Same on All Models					+5V, +10V ±5V, ±10V Same on All Models			
CHANNEL INPUT IMPEDANCE "ON" CONDITION	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms
CHANNEL INPUT IMPEDANCE "FF" CONDITION	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms	100 Megohms
CHANNEL INPUT ACQUISITION TIME	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%	5 μsec to ±0.025%
SYSTEM APERTURE TIME	50 nsec	50 nsec	50 nsec	50 nsec	50 nsec	50 nsec	50 nsec	50 nsec	50 nsec	50 nsec
SYSTEM ACCURACY	±0.05% of FS	±0.05% of FS	±0.05% of FS	±0.05% of FS	±0.05% of FS	±0.025% of FS	±0.025% of FS	±0.025% of FS	±0.025% of FS	±0.025% of FS
LINEARITY	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB	± 1/2 LSB
SYSTEM THROUGHPUT RATE	50KHz (20 μsec)	30KHz (33 μsec)	25KHz (40 μsec)	50KHz (20 μsec)	25KHz (40 μsec)	100KHz (10 μsec)	60KHz (16.6 μsec)	50KHz (20 μsec)	100KHz (10 μsec)	50KHz (20 μsec)
TEMPERATURE COEFFICIENT	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C	±40 ppm/°C
SYSTEM CONTROL INPUTS (DTL/TTL COMPATIBLE)	Random Address Input. Sequential Input. Device Select. Convert, Reset, Strobe.		SAME ON ALL MODELS			Random Address Input. Sequential Input. Device Select. Convert, Reset, Strobe.		SAME ON ALL MODELS		
SYSTEM DIGITAL OUTPUTS	Up to 12 Parallel Lines. Serial Output. End of Conversion. Multiplexer Short Cycle. Frame Sync.		SAME ON ALL MODELS			Up to 12 Parallel Lines. Serial Output End of Conversion. Multiplexer Short Cycle. Frame Sync.		SAME ON ALL MODELS		
SYSTEM OUTPUT DISPLAY (OPTIONAL)	Up to 12 LIGHT EMITTING Diodes for "A/D" Output. Up to 4 LIGHT EMITTING Diodes for Channel Address.		SAME ON ALL MODELS			Up to 12 LIGHT EMITTING Diodes for "A/D" Output. Up to 4 LIGHT EMITTING Diodes for Channel Address.		SAME ON ALL MODELS		
OPERATING TEMPERATURE RANGE	0° to +70°C	0° to +70°C	0° to +70°C	0° to +70°C	0° to +70°C	0° to +70°C	0° to +70°C	0° to +70°C	0° to +70°C	0° to +70°C
STORAGE TEMPERATURE RANGE	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C	−55°C to +85°C
POWER REQUIREMENTS	+ 5VDC @ 800 ma +15VDC @ 130 ma −15VDC @ 70 ma (1)		SAME ON ALL MODELS			+ 5VDC @ 800 ma +15VDC @ 130 ma −15VDC @ 70 ma (1)		SAME ON ALL MODELS		
CASE SIZE	1.5"W x 4.5"L x 5.0"D		SAME ON ALL MODELS			1.5"W x 4.5"L x 5.0"D		SAME ON ALL MODELS		

NOTE: (1) −20VDC @ 16 ma FOR ±10V INPUT VOLTAGE RANGE

OUTPUT CODING FOR DAS-16 SERIES

Analog Input Range (± 10V, FS)	Offset Binary	2's Complement	Analog Input Range (0 to +10V, FS)	Straight Binary	Analog Input Range (0 to +10V, FS)	BCD (8-4-2-1)
+ 9.995	111111111111	011111111111	+ 9.9975	111111111111	+ 9.990	100110011001
+ 8.750	111100000000	011100000000	+ 8.7500	111000000000	+ 8.750	100001110101
+ 7.500	111000000000	011000000000	+ 7.5000	110000000000	+ 7.500	011101010000
+ 5.000	110000000000	010000000000	+ 5.0000	100000000000	+ 5.000	010100000000
0.000	100000000000	000000000000	+ 2.5000	010000000000	+ 2.500	001001010000
− 5.000	010000000000	110000000000	+ 1.2500	001000000000	+ 1.250	000100100101
− 7.500	001000000000	101000000000	0.0000	000000000000	0.000	000000000000
− 8.750	000100000000	100100000000				
− 9.995	000000000001	100000000001				
−10.000	000000000000	100000000000				

MECHANICAL LAYOUT FOR DAS-16 SERIES

BLACK ANODIZED ENCLOSURE (OPTIONAL)
GAIN
OFFSET

SOLID STATE DISPLAY LAMPS (OPTIONAL)
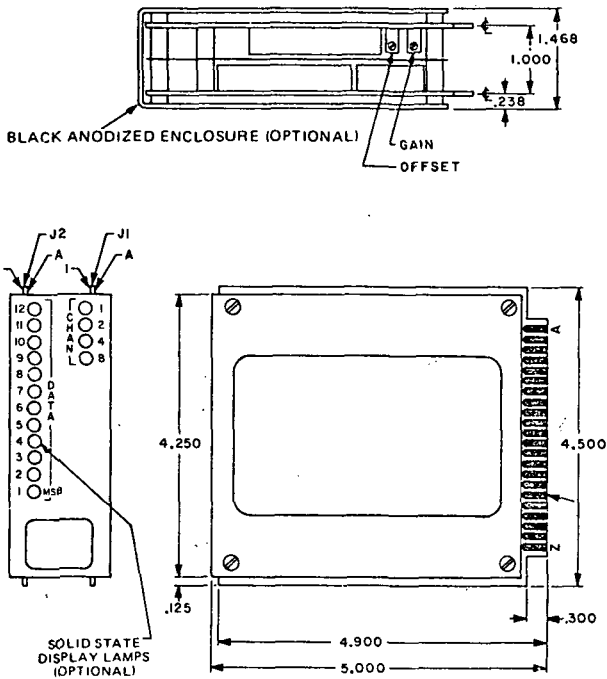
INSTALLATION DIMENSIONS

MATING CONNECTORS
VIKING # 2VK22D/1-3 OR
CINCH # 50 44 A 30
(2 REQ)

INPUT/OUTPUT CONNECTIONS

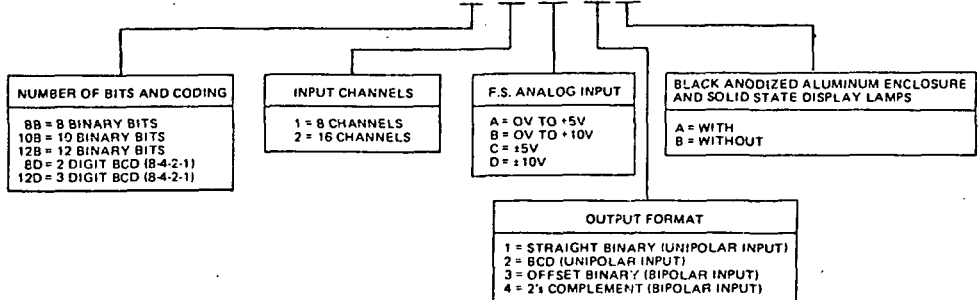| PIN	FUNCTION J1	FUNCTION J2
1	CH 16 LO ANALOG INPUT	8 SEQUENCER OUTPUT
2	CH 15 LO ANALOG INPUT	4 SEQUENCER OUTPUT
3	CH 14 LO ANALOG INPUT	2 SEQUENCER OUTPUT
4	CH 13 LO ANALOG INPUT	1 SEQUENCER OUTPUT
5	CH 12 LO ANALOG INPUT	NO CONNECTION
6	CH 11 LO ANALOG INPUT	NO CONNECTION
7	CH 10 LO ANALOG INPUT	NO CONNECTION
8	CH 9 LO ANALOG INPUT	NO CONNECTION
9	AUX. LO ANALOG INPUT	CONVERT
10	RANDOM / SEQUENTIAL	NO CONNECTION
11	RESET	NO CONNECTION
12	4 RANDOM ADDRESS INPUT	NO CONNECTION
13	8 RANDOM ADDRESS INPUT	−15VDC (S & H)
14	AUX. LO ANALOG INPUT	FRAME SYNC
15	CH 8 LO ANALOG INPUT	1 SEQUENCER OUTPUT
16	CH 7 LO ANALOG INPUT	2 SEQUENCER OUTPUT
17	CH 6 LO ANALOG INPUT	4 SEQUENCER OUTPUT
18	CH 5 LO ANALOG INPUT	8 SEQUENCER OUTPUT
19	CH 4 LO ANALOG INPUT	1 SHORT CYCLE INPUT
20	CH 3 LO ANALOG INPUT	2 SHORT CYCLE INPUT
21	CH 2 LO ANALOG INPUT	4 SHORT CYCLE INPUT
22	CH 1 LO ANALOG INPUT	8 SHORT CYCLE INPUT
A	CH 16 HI ANALOG INPUT	12 DIGITAL OUTPUT (LSB)
B	CH 15 HI ANALOG INPUT	11 DIGITAL OUTPUT
C	CH 14 HI ANALOG INPUT	10 DIGITAL OUTPUT
D	CH 13 HI ANALOG INPUT	9 DIGITAL OUTPUT
E	CH 12 HI ANALOG INPUT	8 DIGITAL OUTPUT
F	CH 11 HI ANALOG INPUT	7 DIGITAL OUTPUT
H	CH 10 HI ANALOG INPUT	6 DIGITAL OUTPUT
J	CH 9 HI ANALOG INPUT	5 DIGITAL OUTPUT
K	AUX. LO ANALOG INPUT	4 DIGITAL OUTPUT
L	DEVICE SELECT	3 DIGITAL OUTPUT
M	STROBE	2 DIGITAL OUTPUT
N	2 RANDOM ADDRESS INPUT	1 DIGITAL OUTPUT (MSB)
P	1 RANDOM ADDRESS INPUT	SERIAL OUTPUT
R	AUX. LO ANALOG INPUT	BUSY
S	CH 8 HI ANALOG INPUT	−15VDC OR −22VDC
T	CH 7 HI ANALOG INPUT	ADC INPUT (TEST POINT)
U	CH 6 HI ANALOG INPUT	+15VDC
V	CH 5 HI ANALOG INPUT	−15VDC
W	CH 4 HI ANALOG INPUT	GROUND
X	CH 3 HI ANALOG INPUT	GROUND
Y	CH 2 HI ANALOG INPUT	+5VDC
Z	CH 1 HI ANALOG INPUT	+5VDC

PRICE LIST

Model	Price
DAS-16-L8B	− $395.
DAS-16-L10B	− $449.
DAS-16-L12B	− $595.
DAS-16-L8D	− $395.
DAS-16-L12D	− $595.
DAS-16-M8B	− $495.
DAS-16-M10B	− $549.
DAS-16-M12B	− $695.
DAS-16-M8D	− $495.
DAS-16-M12D	− $695.

(1) Eight input channels standard, for an additional eight add $100 to List Price.

(2) Add $195. for optional Black Anodized Aluminum Enclosure and Solid State Display Lamps.

ORDERING INFORMATION

DAS-16-M
or
DAS-16-L

NUMBER OF BITS AND CODING
8B = 8 BINARY BITS
10B = 10 BINARY BITS
12B = 12 BINARY BITS
8D = 2 DIGIT BCD (8-4-2-1)
12D = 3 DIGIT BCD (8-4-2-1)

INPUT CHANNELS
1 = 8 CHANNELS
2 = 16 CHANNELS

F.S. ANALOG INPUT
A = OV TO +5V
B = OV TO +10V
C = ±5V
D = ±10V

BLACK ANODIZED ALUMINUM ENCLOSURE AND SOLID STATE DISPLAY LAMPS
A = WITH
B = WITHOUT

OUTPUT FORMAT
1 = STRAIGHT BINARY (UNIPOLAR INPUT)
2 = BCD (UNIPOLAR INPUT)
3 = OFFSET BINARY (BIPOLAR INPUT)
4 = 2's COMPLEMENT (BIPOLAR INPUT)

DATEL SYSTEMS, INC.

1020 TURNPIKE STREET, CANTON, MASS. 02021   TEL. (617) 828-6395   TWX: 710-348-0135

BULLETIN 151157110K

HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-245/545 *Triple Line Transmitter*

HD-246/546/249/549 *Triple Line Receivers*

HD-248/548 *Triple Party Line Receiver*

FEATURES:

- CURRENT MODE OPERATION
- HIGH SPEED: 15MHz WITH 50FT. CABLE; 2MHz WITH 1,000FT. CABLE
- HIGH NOISE IMMUNITY
- LOW EMI GENERATION
- LOW POWER DISSIPATION

- HIGH COMMON MODE REJECTION
- TRANSMITTER AND RECEIVER PARTY LINE CAPABILITY
- TOLERATES –2.0V TO +20.0V GROUND DIFFERENTIAL (Transmitter with respect to receiver)
- TRANSMITTER INPUT/RECEIVER OUTPUT TTL/DTL COMPATIBLE

GENERAL DESCRIPTION

Each transmitter-receiver combination provides a digital interface between systems linked by 100Ω twisted pair, shielded cable. Each device contains three circuits fabricated within a single monolithic chip. Data rates greater than 15MHz are possible depending on transmission line loss characteristics and length.

The transmitter employs constant current switching which provides high noise immunity along with high speeds, low power dissipation, low EMI generation and the ability to drive high capacitance loads. In addition, the transmitters can be turned "off", allowing several transmitters to time-share a single line.

Receiver input/output differences are shown in the following table:

	INPUT	OUTPUT
HD-246 / 546	100Ω	OPEN COLLECTOR
HD-248 / 548	HI-Z	6K PULL-UP RES.
HD-249 / 549	100Ω	6K PULL-UP RES.

The internal 100Ω cable termination consists of 50Ω from each input to ground.

HD-248/548 "party line" receivers have a high-Z input such that as many as ten of these receivers can be used on a single transmission line.

Each transmitter input and receiver output can be connected to TTL and DTL systems. When used with shielded transmission line, the transmitter-receiver system has very high immunity to capacitive and magnetic noise coupling from adjacent conductors. The system can tolerate ground differentials of –2.0 V to +20.0V (transmitter with respect to receiver).

PACKAGES

DUAL INLINE

ALL DIMENSIONS IN INCHES.

NOTE: Pin 1 identified by notch and/or dote in shaded area.
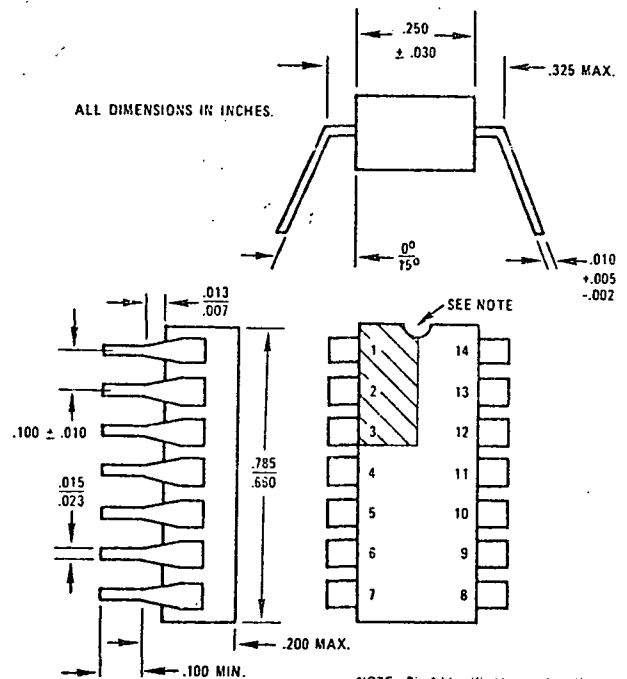
TO – 86 FLAT – PAK
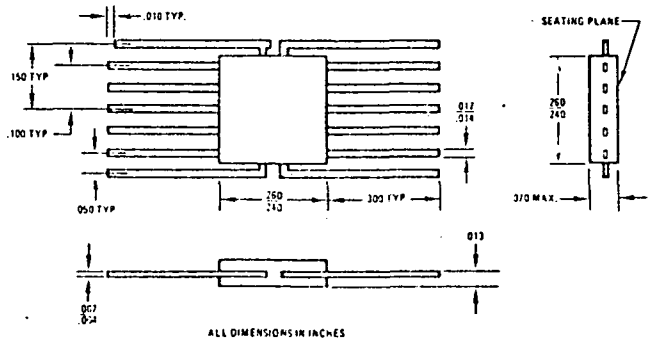
ALL DIMENSIONS IN INCHES

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range	-1.0V to +1.0V	Input Current	±25mA
Output Voltage Range	-0.5V to +6.0V	Output Current	+50mA
V_{CC} Range	-0.5V to +8.0V	Storage Temperature	-65°C to +150°C
V_{EE} Range	-8.0V to +0.5V		

ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	TEMP.	HD-246/248/249 -55°C to +125°C MIN.	TYP.	MAX.	HD-546/548/549 0°C to +75°C MIN.	TYP.	MAX.	UNITS	TEST COND. $V_{EE}=-5V$ V_{CC}	NOTES
INPUT RESISTANCE (HD-246/546 & HD-249/549)	R_{IN}	+25°C / Full	40 / 39	47	61 / 68	35 / 33	47	65 / 70	Ohms		
PULL-UP RESISTOR (HD-248/548 & HD-249/549)		+25°C / Full	4.2 / 4.1	6	7.8 / 8.6	4.0 / 3.9	6	8.1 / 8.6	K Ohms		
OUTPUT VOLTAGE (HIGH)	V_{OH}	+25°C / Full	2.6 / 2.5			2.6 / 2.5			V	4.5	Note 1 $I_{OH}=-120\mu A$ Ext. 6K Res. For HD-246/546
OUTPUT VOLTAGE (LOW)	V_{OL}	+25°C / Full			0.45 / 0.45			0.45 / 0.45	V	4.5	Note 2 $I_{OL}=9.6mA$ 10mA For HD-246/546
OUTPUT VOLTAGE (LOW) (INPUT SHORT CIRCUIT)	V_{OLSC}	+25°C		0.4			0.4		V	5.0	Note 3 $I_{OL}=3.2mA$
HD-246/546 POWER SUPPLY CURRENT (TOTAL) — I_{CC} / I_{EE}		+25°C		3.3 / 5.1	4.8 / 6.0		3.3 / 5.1	5.7 / 6.3	mA	5.0	Note 4
I_{CC} / I_{EE}		+25°C		3.9 / 5.1	6.6 / 6.0		3.9 / 5.1	7.5 / 6.3	mA	5.0	Note 5
HD-248/548 & HD-249/549 — I_{CC} / I_{EE}		+25°C		6.3 / 5.1	7.8 / 6.0		6.3 / 5.1	8.7 / 6.3	mA	5.0	Note 4
I_{CC} / I_{EE}		+25°C		3.9 / 5.1	6.6 / 6.0		3.9 / 5.1	7.5 / 6.3	mA	5.0	Note 5
PROPAGATION DELAY TEST CIRCUIT 2 PAGE 4 — t_{PLH}		+25°C / Full		18	30 / 30		18	30 / 30	ns	5.0	
t_{PHL}		+25°C / Full		25	30 / 30		25	30 / 30	ns	5.0	

DC — (rows: V_{OH}, V_{OL}, V_{OLSC}, power supply current)

AC — (rows: t_{PLH}, t_{PHL})

NOTES:
1. (+) $I_{IN}=1.5mA$; (−) Input = open (For HD-248/548; Ext. 50Ω Res. or 0.75mV).
2. (+) Input = open; (−) $I_{IN}=1.5mA$. (For HD-248/548; Ext. 50Ω Res. or 0.75mV).
3. Both inputs shorted to Gnd; or both inputs open such that 50Ω termination resistors are in the circuit.
4. (+) Input = open; (−) $I_{IN}=3mA$.
5. (+) $I_{IN}=3mA$; (−) Input = open.

BLOCK DIAGRAM

(−) INPUT	1	14	V_{CC} R1 & R2
(+) INPUT	2	13	V_{CC} R3
(R1) OUTPUT	3	12	V_{EE} R1 & R2
(−) INPUT	4	11	V_{EE} R3
(+) INPUT	5	10	OUTPUT R3
(R2) OUTPUT	6	9	INPUT (+)
GND	7	8	INPUT (−)
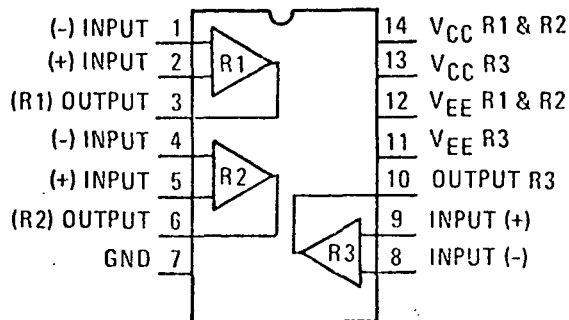
SCHEMATIC
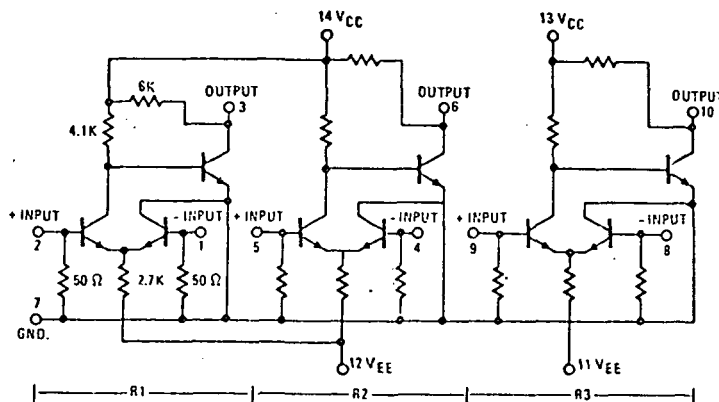
NOTES:
1. HD-249/549 is as shown
2. HD-246/546 does not have 6K output pull-up resistors.
3. HD-248/548 does not have 50Ω input termination resistors.
4. Resistor values are nominal

TEST CIRCUIT 1 - TRANSMITTER PROPAGATION DELAY

INPUT:

$\left.\begin{array}{c} t_{TLH} \\ t_{THL} \end{array}\right\} \leq 10 \text{ ns}$

pw = 500 ns
f = 1 MHz

$\phi 1$ IN ─── OPEN ($\approx$3.2V)
── 0V

$\phi 2$ IN ─── OPEN ($\approx$3.2V)
── 0V

t_{PHL} ── ── t_{PLH}

$\phi 1$ OUT ─── $\approx$0.15V ($\approx$3MA)
── 0V

$\phi 2$ OUT ─── $\approx$0.15V ($\approx$3MA)
── 0V

All measurements referenced to 50 % V points

V_{CC}=+5V

$\phi 1$ ○── D.U.T. ──○ $\phi 1$ V out
50 Ω 1%

TRANSMITTER OUT

$\phi 2$ ○── ──○ $\phi 2$ V out
50 Ω 1%

$$I_{out} = \frac{V_{out}}{50\ \Omega}$$
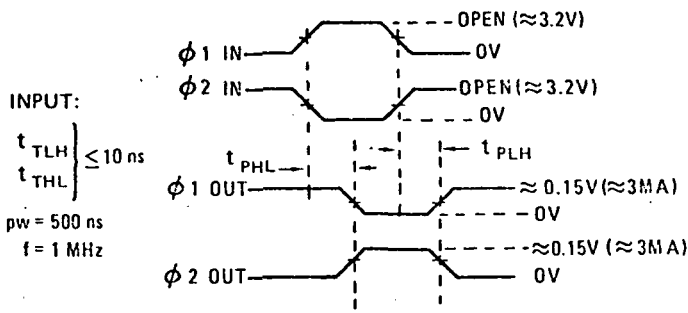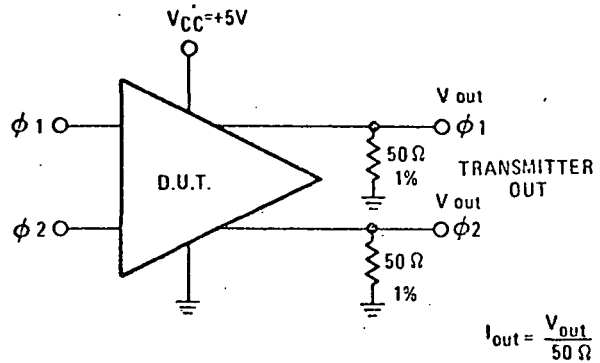
TEST CIRCUIT 2 - RECEIVER PROPAGATION DELAY

INPUT:

$\left.\begin{array}{c} t_{TLH} \\ t_{THL} \end{array}\right\} \leq 10 \text{ns}$

pw = 500ns
f = 1 MHz

(+) IN ─── 150 MV
── 0V

(−) IN ─── 150 MV
── 0V

t_{PLH} ──

RECEIVER OUT ─── ─5V
── 0V

t_{PHL}

All measurements referenced to 50%V points.

V_{CC}=+5V

(+) ○── 50 Ω 520 Ω
50 Ω D.U.T.
(−) ○── 800 Ω RCVR. OUT.
30 pF

V_{EE}=−5V
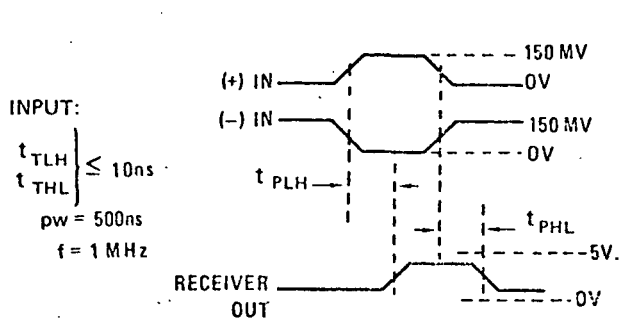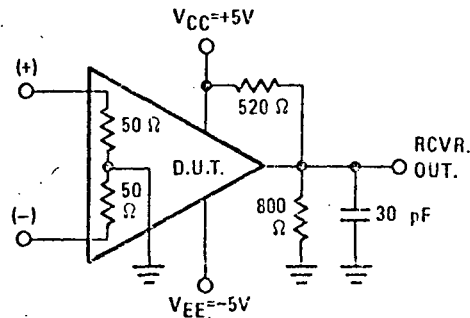
NOTE: External 50Ω resistors needed for HD−248/548.

TYPICAL APPLICATION

IN

+5V

1/3 HD-245/545

ENABLE

+5V

(+) 50Ω 1/3 HD-246/546 OR HD-249/549
50Ω RCVR. OUT.
(−)

−5V

+5V

(+) 1/3 HD-248/548 "PARTY LINE" RECEIVER
(−) ○ OUTPUT

−5V
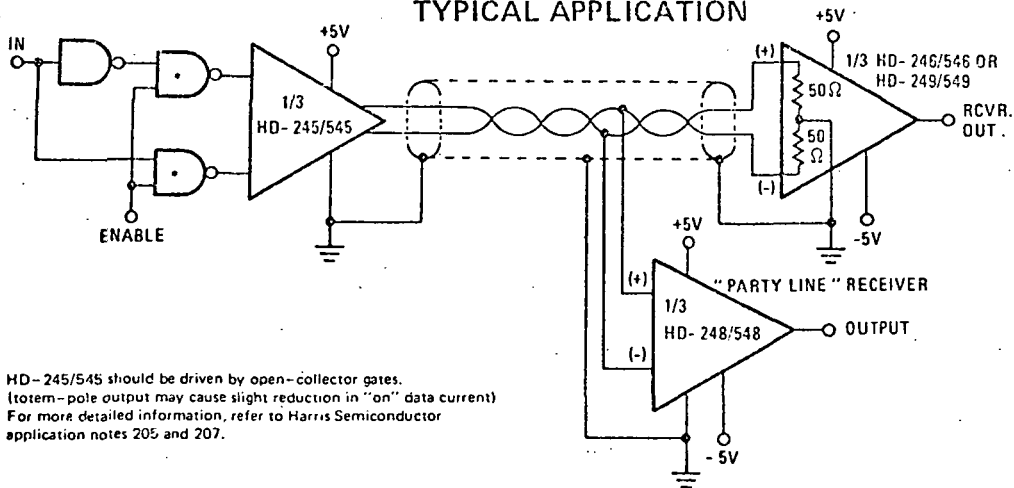
- HD-245/545 should be driven by open-collector gates.
  (totem-pole output may cause slight reduction in "on" data current)
  For more detailed information, refer to Harris Semiconductor
  application notes 205 and 207.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

1024 BIT CAPACITY MULTIPLEXED DYNAMIC SHIFT REGISTERS

SILICON GATE MOS 2500 SERIES

2502
2503
2504

DESCRIPTION

These Signetics 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

FEATURES

- 10 MHz TYPICAL DATA RATE
- THREE CONFIGURATIONS—QUAD 256, DUAL 512, SINGLE 1024
- LOW POWER DISSIPATION—40 μW/bit at 1 MHz DATA RATE
- LOW CLOCK CAPACITANCE—140 pF
- TTL, DTL COMPATIBLE
- STANDARD PACKAGES - 8 LEAD TO-99, 8-PIN AND 16-PIN SILICONE DUAL IN-LINE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (10 MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.
The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

The data inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

PIN CONFIGURATIONS (Top View)

2502B

1. OUT 1	16. IN 4
2. NC	15. NC
3. IN 1	14. OUT 4
4. ϕ1	13. NC
5. V$_{CC}$	12. V$_{DD}$
6. OUT 2	11. ϕ2
7. NC	10. IN 3
8. IN 2	9. OUT 3

2503V

1. OUT$_2$	8. V$_{CC}$
2. IN$_2$	7. ϕ_1
3. ϕ_2	6. IN$_1$
4. V$_{DD}$	5. OUT$_1$

2503TA

1. OUT 1	5. OUT 2
2. IN 1	6. IN 2
3. ϕ1	7. ϕ2
4. V$_{CC}$	8. V$_{DD}$

2504V

1. OUT	8. V$_{CC}$
2. ϕ_2	7. NC
3. NC	6. ϕ_1
4. V$_{DD}$	5. IN

2504TA

1. NC	5. OUT
2. IN	6. NC
3. ϕ1	7. ϕ2
4. V$_{CC}$	8. V$_{DD}$

PART IDENTIFICATION TABLE

TYPE	FUNCTION	PACKAGE
2502B	Quad 256-bit	16-Pin DIP
2503TA	Dual 512-bit	TO-99
2503V	Dual 512-bit	8-Pin DIP
2504TA	Single 1024-bit	TO-99
2504V	Single 1024-bit	8-Pin DIP

SILICON GATE MOS 2502, 2503, 2504

MAXIMUM SIGNETICS GUARANTEED RATINGS[1]

Operating Ambient Temperature[2]	$0°C$ to $+70°C$
Storage Temperature	$-65°C$ to $+150°C$
Power Dissipation[2] at $T_A = 70°C$	
TA and V Package	535mW
B Package	640mW
Data and Clock Input Voltages	
and Supply Voltages with	
respect to V_{CC} [3]	$+0.3V$ to $-20V$

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a $+150°C$ maximum junction temperature and a thermal resistance of $150°C/W$ (TA and V package) or $125°C/W$ (B package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values at $+25°C$ and nominal supply voltages.
8. V_{CC} tolerance is $\pm5\%$. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

POWER DISSIPATION VERSUS DATA RATE
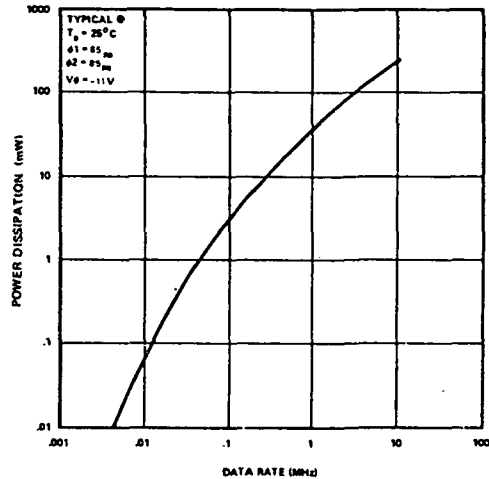
DC CHARACTERISTICS

$T_A = 0°C$ to $+70°C$; $V_{DD} = -5V \pm5\%$; $V_{CC} = +5V$ (8) unless otherwise noted. (See Notes 4,5,6,7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	$V_{IN} = V_{CC}$ to V_{DD}, $T_A = 25°C$
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi 1} = V_{\phi 2} = -10V$ $V_{OUT} = 0.0V$, $T_A = 25°C$
I_{LC}	Clock Leakage Current		10	1000	nA	$V_{ILC} = -10V$, $T_A = 25°C$
I_{DD}	Power Supply Current		15	25	mA	Outputs at logic "0", 4 MHz data rate, $\phi 1 = \phi 2 = 85ns$ continuous operation, $V_{ILC} = -12V$ $T_A = 25°C$
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-10		-12	V	

AC CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$, (See notes 4, 5, 6, 7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0.0005		4	MHz	
Frequency	Data Rep Rate	0.001		8	MHz	
ϕ pw	Clock Pulse Width	85			ns	
ϕ d	Clock Pulse Delay	10			ns	
t_r, t_f	Clock Pulse Transition	10		1000	ns	
t_w	Data Write Time (Setup)	50			ns	
t_{DO}	Data in Overlap	10			ns	
t_a+	Data Out			90	ns	
C_{IN}	Input Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
C_{OUT}	Output Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
$C\phi$	Clock Capacitance	130		150	pF	@ 1 MHz 25 mV p-p
V_{OL}	Output "Low" Voltage		-0.3		V	R_L=3k, depends on R_L and TTL Gate
V_{OH1}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6k
V_{OH2}	Output "High" Voltage Driving TTL	3.0	3.5		V	R_L = 3k

MULTIPLEXED 4-BIT MOS SHIFT REGISTER

Figure 1

Figure 1 is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at $\phi 1$ time, it exits at $\phi 1$ time, (beginning on $\phi 1$'s negative going edge and ending on the succeeding $\phi 2$'s negative going edge).
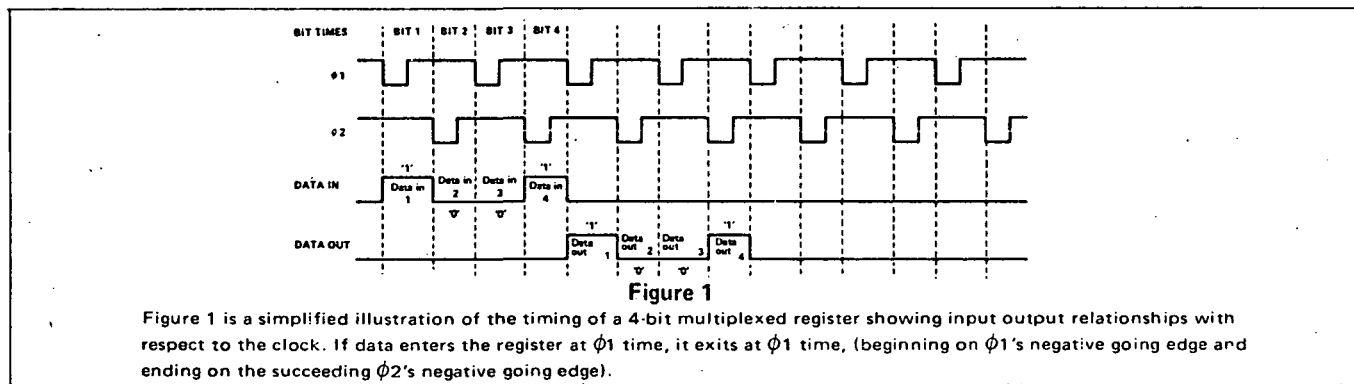
CONDITIONS OF TEST

Input rise and fall times: 10nsec. Output load is 1 TTL gate.

TIMING DIAGRAM

* t_w and t_{DO} same for $\phi 2$
** N=256 for 2502, N = 512 for 2503, N = 1024 for 2504

APPLICATIONS INFORMATION

DTL/TTL/MOS INTERFACES

NOTE: When interfacing MOS to MOS output resistors should be 4.7K min

41
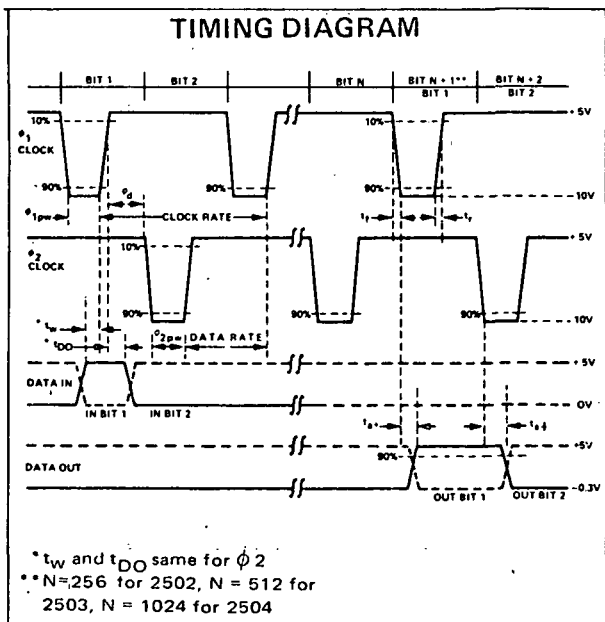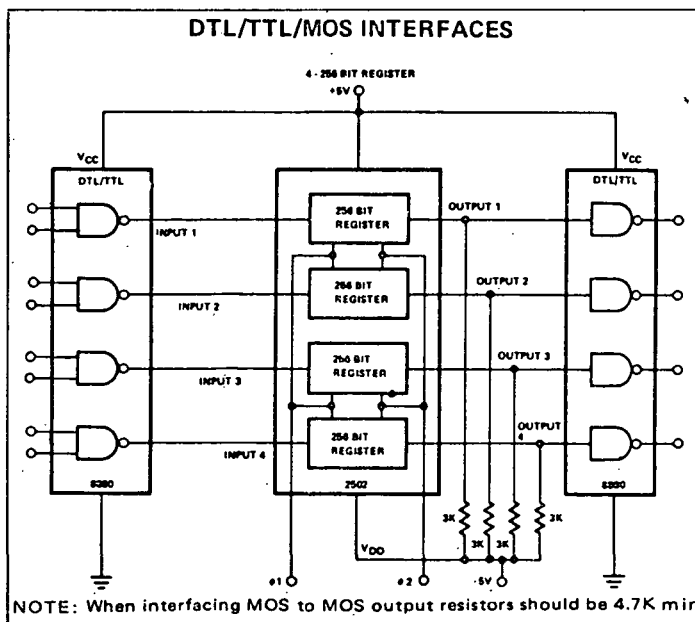
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE

POWER DISSIPATION (mW/BIT)

$|V_{CC} - V_{DD}|$ (VOLTS)
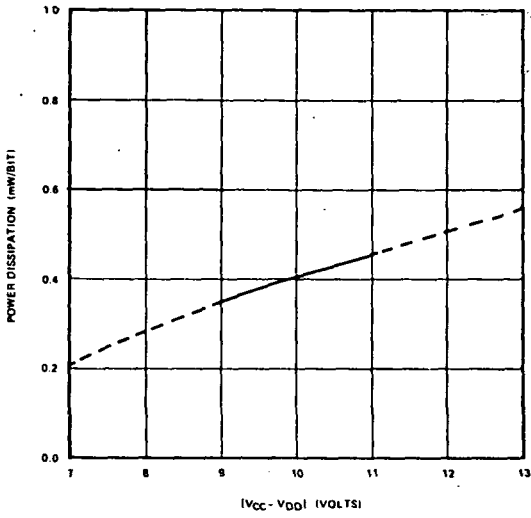
POWER DISSIPATION/BIT VERSUS CLOCK AMPLITUDE

POWER DISSIPATION (mW/BIT)

CLOCK AMPLITUDE (VOLTS p-p)
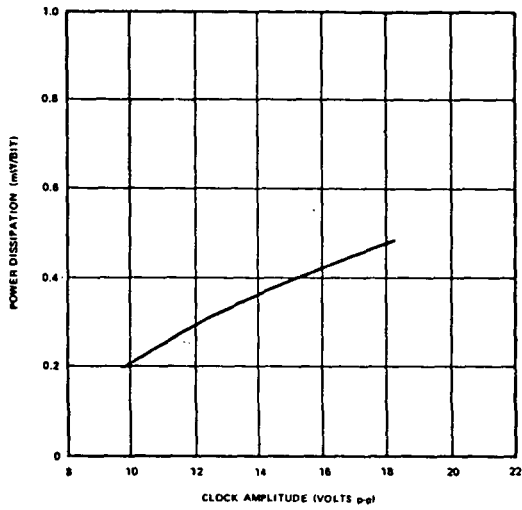
POWER DISSIPATION/BIT VERSUS TEMPERATURE

POWER DISSIPATION (mW/BIT)
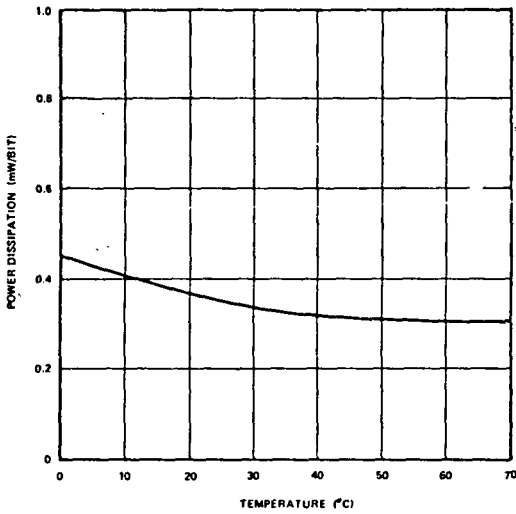
TEMPERATURE (°C)

MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

PACKAGE MAXIMUM ALLOWABLE POWER DISSIPATION (mW)

"B" PKG.

"V" AND "TA" PKG.
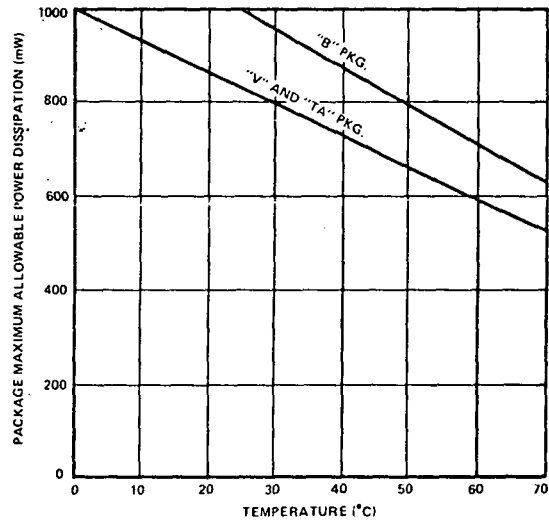
TEMPERATURE (°C)

CLOCK AMPLITUDE V_ϕ VERSUS MAXIMUM DATA RATE

MAXIMUM DATA RATE (MHz)

CLOCK AMPLITUDE (VOLTS p-p)
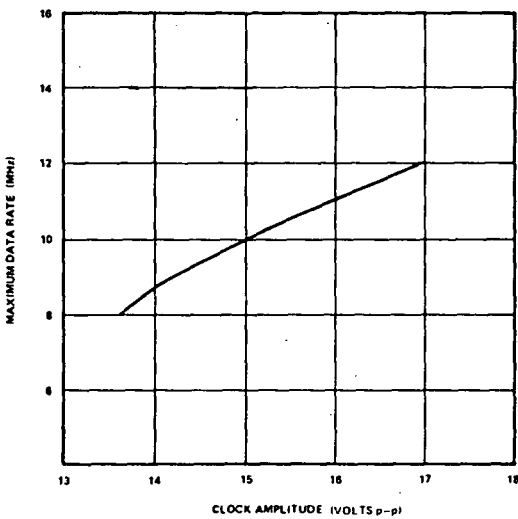
MINIMUM OPERATING DATA RATE VERSUS TEMPERATURE

DATA RATE (Hz)

GUARANTEED

TYPICAL

TEMPERATURE (°C)
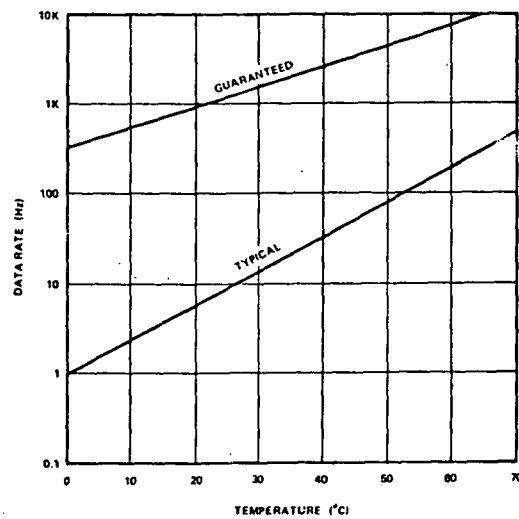
NOTE:
Conditions for Typical Curves; V_{CC} = +5V, V_{DD} = -5V, ϕ_{1PW} and ϕ_{2PW} = 85ns, V_ϕ = -11V, T_A = 25°C, f_{DATA} = 10MHz unless otherwise noted.

APPLICATIONS (Cont'd)

WRITE/RECIRCULATE LOGIC
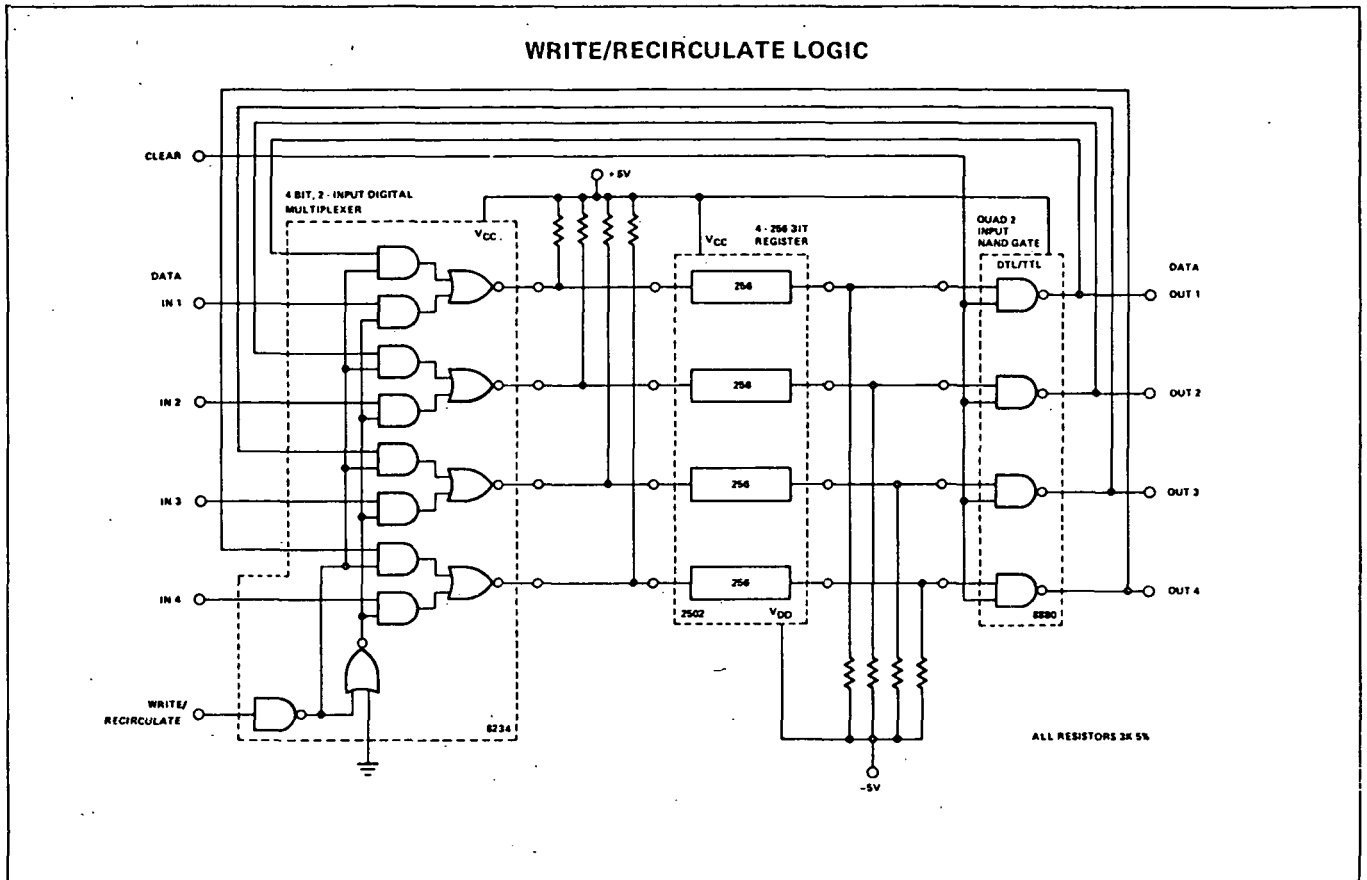
CIRCUIT SCHEMATIC
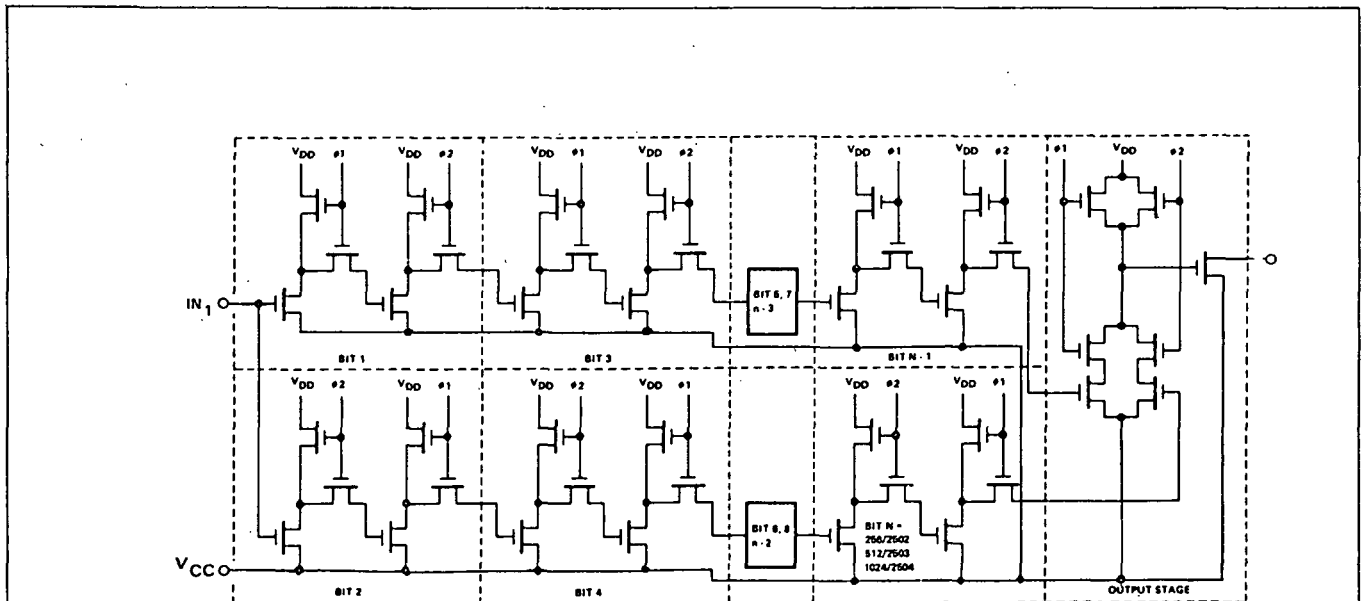
NOTES:
1. N = 1024 on 2504
2. N = 512 on 2503 schematic for second register same as above.
3. N = 256 on 2502 schematic for second, third and fourth registers same as above.

PACKAGE INFORMATION

B PACKAGE

NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: (-) Ja = .16 C/mW, (-) Jc = .08° C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

T PACKAGE

NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT, GOLD PLATED, GLASS BODY.
3. LID MATERIAL: NICKEL, WELD SEAL.
4. THERMAL RESISTANCE FROM JUNCTION TO CASE, (-) Ja = .150 C/mW, (-) Jc = .025 C/mW.
5. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

V PACKAGE

NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: (-) Ja = .16 C/mW, (-) Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

PRODUCT DIGEST

The UNI Series VARI-rated power supply modules may be operated at any range of DC output voltages and currents, so the nine units replace literally thousands of more expensive, narrow-range power supplies. Collectively, the outputs of the UNI Series cover currents from 0 to 34 amperes and voltages from 0 to 34 volts. All units are UL approved.

These power supplies are compact, rugged, mount on any of three sides, and meet Mil Spec environment requirements. They are short-circuit proof, designed for efficient operation up to 71°C without external cooling, carry a 5-year Warranty, and are significantly less expensive than narrow-range units.

THE UNIQUE UNI CONCEPT

The key to the versatility of PMC's UNI Series is an exceptional design concept pioneered by POWER/MATE CORP. It allows any UNI power supply to be set for a range of DC outputs. This adjustable feature simplifies the customer's inventory situation, and it makes possible POWER/MATE's Same-Day-Shipment policy for UNI power supplies.

SPECIFICATIONS

INPUT: 105-125V, 47-420 CPS.

OUTPUT VOLTAGE: 0-30 volts for all units except Uni-76 (0-34V); Uni-88 (0-34V); and UniTwin 164 (0-25V dual output).

OUTPUT VOLTAGE RANGE: Set in overlapping ranges by means of internal quick disconnect taps.

OUTPUT CURRENT: See chart on following page.

REGULATION: Uni-76 and Uni-88 better than ±0.005% +1MV for line and load. All other units better than ±0.01% +1MV for line and load.

RIPPLE: Less than 250 microvolts.

RESPONSE TIME: Less than 20 microseconds.

TEMPERATURE COEFFICIENT: Better than 0.01%/°C.

LONG TERM STABILITY: Better than 0.025% for 8 hours.

OVERLOAD & SHORT CIRCUIT PROTECTION: Solid state short circuit and overload protected. Instantaneous recovery, and automatic reset. Unit cannot be damaged by prolonged short circuits or overloads.

POLARITY: May be either positive, negative or floating up to 300 volts.

AMBIENT OPERATING TEMPERATURE: Continuous duty from −20°C to +71°C ambient.

STORAGE TEMPERATURE: −55°C to +85°C.

OUTPUT CURRENT vs. TEMPERATURE: Unit is rated for full current output at temperatures between −20°C and +45°C and is linearly derated from +45°C to 70% of the full output at +71°C.
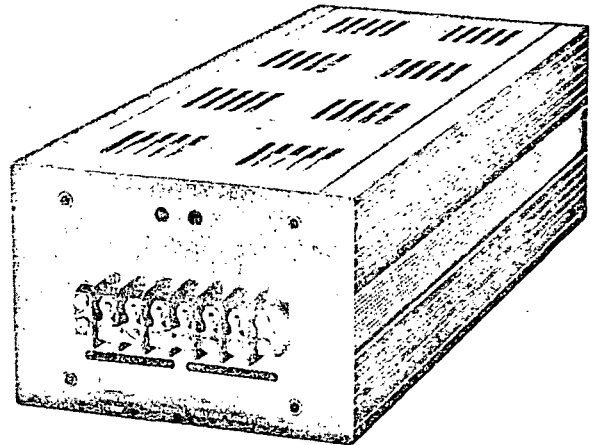
REMOTE-LOCAL SENSING: Provision is included to permit remote sensing of the output voltage directly at the load for improved over-all regulation. Unit may be connected for local sensing if desired.

REMOTE-LOCAL VOLTAGE ADJUST: Output voltage may be remotely adjusted, or internally adjusted with coarse and fine controls. Both are accessible through holes in the terminal end of the supply.

MECHANICAL DATA

UNI power supplies may be mounted on any of three surfaces. They will function when mounted in any position.
10-32 screws and studs are supplied for mounting each power supply. For detail dimensions see page 10.
3½-inch and 5¼-inch rack mounting assemblies are available, along with other accessories. See pages 19-22.

SAME-DAY-SHIPMENT
You can be sure that POWER/MATE CORP. will ship any of its UNI series power supplies to you the same day that your order arrives in our offices.

UL APPROVED
POWER/MATE's power supplies are listed as a recognized component in Underwriter Laboratory's recognized component index. (UL 478-1967).

5-YEAR WARRANTY
5 Year Warranty
To express our confidence in the skill and care with which our power supplies are designed and built — confidence based on an impressive 100,000 hour MTBF — we offer the POWER/MATE 5-Year Warranty.

Pioneers of the UNI concept in power supplies

OUTPUT VOLTAGE vs. OUTPUT CURRENT FOR VARI-RATED UNI SERIES

Model	3	5	6	8	10	12	14	15	16	18	20	22	24	26	28	30
UNI-76							0.5 amps throughout range									
UNI-88							1.5 amps throughout range									
UNI-30C	4	4	4	4	4	3.75	3.6	3.5	3.4	3.25	3.0	2.9	2.75	2.5	2.5	2.1
UNI-30D	6	6	6	5.6	5.2	5.0	4.7	4.5	4.3	4.2	4.1	3.7	3.5	3.4	3.3	3.1
UNI-30E	12	12	11	10.5	9.5	9.3	8.5	8.0	7.7	7.5	7.0	6.5	6.0	5.7	5.5	5.2
UNI-30F	15	15	15	14.2	12.8	12.0	11.5	10.0	10.0	9.9	9.4	8.9	8.7	8.5	8.0	7.6
UNI-30G	24	22	21	20	18	17	16.5	16.0	15.5	15	14	13.5	13	12.5	12	11.5
UNI-30H	34	32	31	29	25	23	22	21	20	19	17	16.5	16	15.5	15	14.3

The columns are labeled **VOLTAGE** across the top and **AMPERES** down the right side.

SAME DAY SHIPMENT
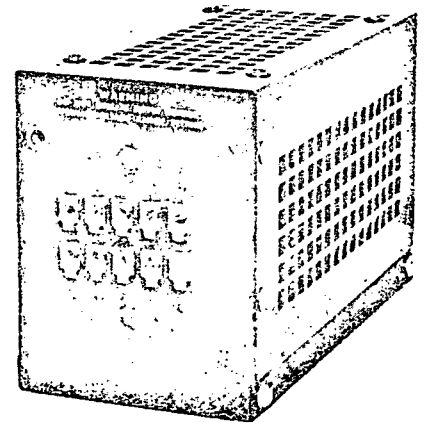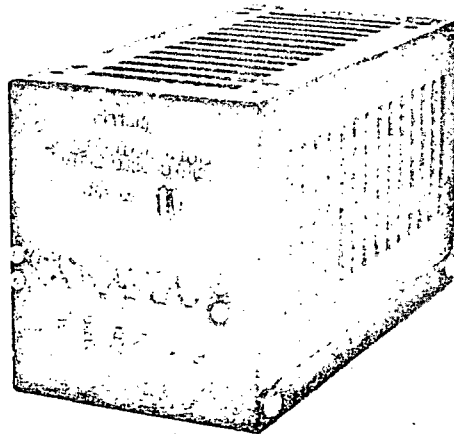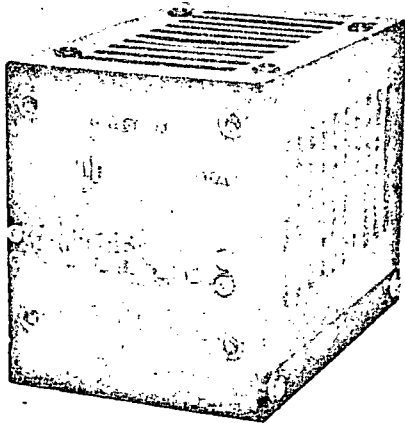
UNI-76 0-34 volts, 0.5 amp over entire voltage range. Regulation: Better than ±0.005% +1 Mv for line and load.
3⅝"W x 3⅞"H x 5⅛"D
Weight: Net 3¾ lbs.,
Shipping 4¾ lbs.
$76⁰⁰

UNI-88 0-34 volts, 1.5 amps over entire range. Regulation: Better than ±0.005% +1 Mv for line and load.
3⅝"W x 3⅞"H x 6⅞"D
WEIGHT: Net 5¼ lbs.,
Shipping 6¼ lbs.
$99⁰⁰

UniTwin-164 DUAL OUTPUT 0-25 volts, 0.75 amps over entire voltage range. Regulation: Better than ±0.005% +1 Mv for line and load.
3⅝"W x 4¼"H x 6⅞"D
WEIGHT: Net 5¾ lbs.,
Shipping 7½ lbs.
$164⁰⁰

Designers and manufacturers of quality power supplies

SAME DAY SHIPMENT
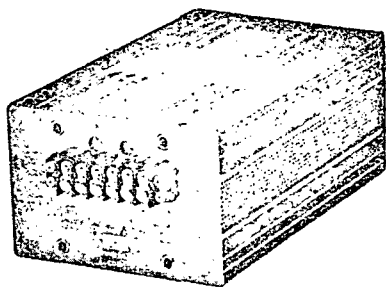
UNI-30C 0-30 volts, up to 4 amps. Regulation: Better than ±0.01% +1 Mv for line and load.

5¾₂"W x 3⅚"H x 7⅝"D
WEIGHT: Net 8¼ lbs.,
Shipping 10¼ lbs.
$134.00
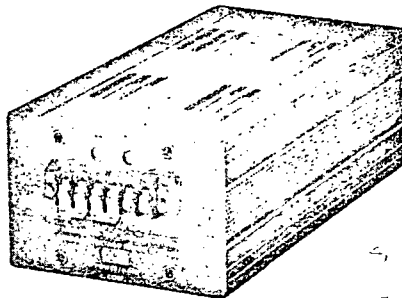
UNI-30D 0-30 volts, up to 6 amps (see chart). Regulation: ±0.01% +1 Mv for line and load.

5¾₂"W x 3⅚"H x 9⅜"D
WEIGHT: Net 11½ lbs.,
Shipping 14 lbs.
$151.00
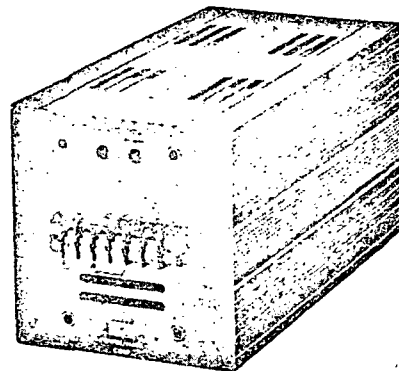
UNI-30E 0-30 volts, up to 12 amps (see chart). Regulation: ±0.01% +1 Mv for line and load.

5¾₂"W x 5¾₂"H x 9⅜"D
WEIGHT: Net 15½ lbs.,
Shipping 19 lbs.
$174.00

SAME DAY SHIPMENT
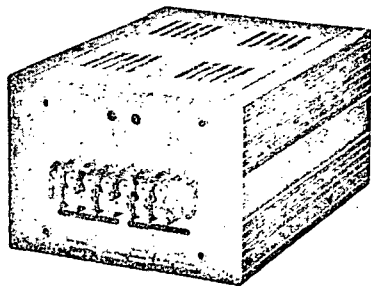
UNI-30F 0-30 volts, up to 15 amps (see chart). Regulation: ±0.01% +1 Mv for line and load.

7½"W x 5¾₂"H x 9⅜"D
WEIGHT: Net 20¼ lbs.,
Shipping 24¼ lbs.
$205.00
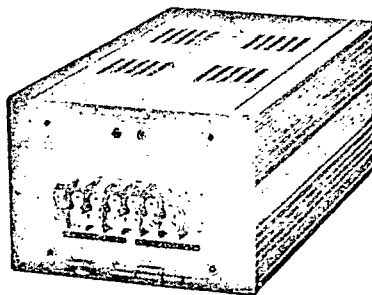
UNI-30G 0-30 volts, up to 24 amps (see chart). Regulation: ±0.01% +1 Mv for line and load.

7½"W x 5¾₂"H x 11⅞"D
WEIGHT: Net 25¾ lbs.,
Shipping 30¼ lbs.
$265.00
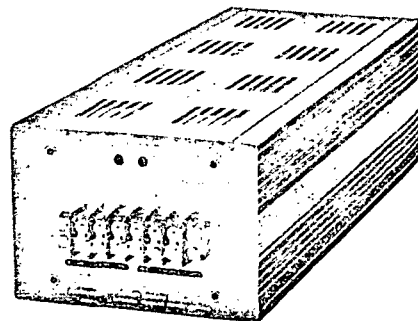
UNI-30H 0-30 volts, up to 34 amps (see chart). Regulation: ±0.01% +1 Mv for line and load.

7½"W x 5¾₂"H x 16½"D
WEIGHT: Net 34½ lbs.,
Shipping 39½ lbs.
$315.00

Pioneers of the UNI concept in power supplies

6

PMC

POWER/MATE CORP.

OPERATING INSTRUCTIONS
for
REGULATED POWER SUPPLY

1.0 GENERAL

All Power/Mate power supplies are carefully inspected and tested to insure conformance to our published specifications as stated in the catalog. However, to insure satisfactory performance and long life, it is important to operate and maintain the power supply properly in accordance with these instructions.

2.0 POWER SUPPLY MOUNTING

All Power/Mate supplies are designed for convention cooling. However, it is important not to impede the air flow across and through the power supply case. Heat is the primary cause of failure in any piece of electronic equipment. Impeding the flow of convection air through your power supply may result in a shortening of the long-life designed into by Power/Mate.

Conversely, forced air, from a small fan, through the heat generating components of the power supply, can overcome any impediment of the natural convention air flow. If there is any doubt as to the amount of convection air flow through your Power/Mate power supply, the use of a small fan to insure a satisfactory air flow is recommended.

When chassis mounting any Power/Mate power supply using the bottom mounting holes, make sure that the ventilation holes in the power supply chassis are not covered by the mounting chassis. The mounting chassis should have cut-outs approximating the ventillating holes in the power supply. This permits the normal air convection throught the power supply.

An alternative method to permit proper air convection current is to provide a 1/2 inch space (minimum) between the power supply and the mounting chassis.

Detailed mounting and outline dimensions for most Power/Mate power supplies are given in the general Power Mate power supply catalog.

3.0 OUTPUT VOLTAGE ADJUSTMENTS

The output of most Power/Mate power supplies can be adjusted simply by monitoring the output voltage on a meter placed across the output terminals or by means of the front panel meter (where applicable.)

Many power supplies have both a coarse and fine voltage control to more accurately set the output voltage.

3.1 UNI SERIES POWER SUPPLY OUTPUT ADJUSTMENT

All UNI Series (universal series) power supplies as shipped from the factory are set for a nominal 5 volts output. These power supplies may be set for any output from zero to 30 volts by the following procedure:
1. Remove the cover on case size A, B, and BB. Remove the rear panel on case size C through H.
2. Select the proper tap for the desired output voltage range. The voltage range for each tap is indicated on the transformer.
3. Set coarse and fine voltage controls (accessible from terminal block side of power supply) to nominal center position.
4. Make sure + (pos.) terminal and + sense terminal are connected together. Similarly, make sure - (neg.) terminal and - sense term are connected together.
5. Connect 115 volt to AC input terminals.
6. Connect an accurate meter to DC output terminals of power supply.
7. Adjust the coarse voltage control to the desired output voltage.
8. Turn off the AC, replace the cover or rear panel. The fine voltage control may be used to more accurately adjust the output voltage to the precise desired value.

CAUTION

THE POWER SUPPLY MAY BE DAMAGED IF THE COARSE CONTROL IS SET TO OPERATE THE POWER SUPPLY OUTSIDE OF THE VOLTAGE RANGE LIMITS NOTED ON THE TRANSFORMER TAP RANGE SETTING INSIDE OF THE POWER SUPPLY.

4.0 LOCAL-REMOTE LOAD SENSING

Many power supplies have the remote local load sensing feature. This feature is available on power supplies with +sense and -sense terminals marked on the terminal block. Power supplies shipped from the factory are normally connected for local sensing. Connections for remote or local load sensing is shown in Fig. 1.

5.0 OUTPUT CURRENT ADJUSTMENT

On power supplies with an output current limit control, this may be adjusted as follows:

Connect an ammeter across the output terminals of the power supply. Use an ammeter with a range greater than the desired current limit setting. Remove all other loads from the power supply. Apply AC to the input of the power supply and adjust the current limit control to the desired current as indicated on the ammeter. This adjustment limits the output current from the power supply under all load conditions.

CAUTION

Make sure that this current setting is within the ratings of the power supply otherwise overheating and possible damage may occur to your power supply. Make certain that the power supply output voltage is set to the normal output voltage under normal or open circuit load conditions, before adjusting the current setting. Make sure the current setting is set beyond the "knee" of the current setting, otherwise the voltage regulation of the power supply may be affected.

On power supplies with front panel meters, it is only necessary to short circuit the output of the power supply. The current adjust may be set to the desired current limit as indicated on the front panel meter.

6.0 OVERVOLTAGE ADJUSTMENT

Many Power/Mate power supplies have overvoltage protection built-in to the power supply. This unit is also available as a separate unit.

The adjustment and checking of the overvoltage feature can be accomplished as follows:

Set the overvoltage adjustment to the highest voltage setting. Set the power supply output voltage to the desired overvoltage set point and monitor the output on a voltmeter. Typically, the overvoltage set point is at least 15% plus one volt above the normal output voltage of the power supply. This prevents spurious triggering of the OVP from external transients. Turn the overvoltage control slowly until the output voltage of the power supply drops from the set point to approximately 0.6 volts. Turn off power for 15 seconds and readjust power supply voltage controls to normal setting. Re-apply power and readjust output voltage to normal output voltage.

In the event that the power supply cannot be adjusted to the desired overvoltage set point, an externally adjustable power supply connected across the output terminals of the power supply may be used.

Under certain conditions, the AC input current can become large when the overvoltage protector operates. It is recommended the following fuse rating be used in the AC input lead to the power supply.

$$\text{Input fuse rating, Slo-blo type} = \frac{\text{Output voltage x output current x 4}}{\text{Nominal line voltage}}$$

7.0 SERVICE

When additional instructions are required or repair service is desired, contact the Power/Mate Corp. where trained personnel and complete facilities are ready to assist you.

Please include the power supply model and serial number together with complete details of the problem. On receipt of this information, Power/Mate will supply service data or advise shipping for factory repair service.

All repairs not covered by the warranty will be billed at cost and an estimate forwarded for approval before work is started.

8.0 PARTS ORDERING

Standard components and special components used in any Power/Mate power supply can be obtained from the factory.

The following information must be included when ordering parts:

1. Model number and serial number of power supply and purchase date.
2. Power/Mate part number.
3. Description of part together with reference designation.
4. If part is not an electronic part, or is not listed, provide a description, function, and location of the part.

PIMIC

UNI-SERIES
OEM-SERIES
FR-SERIES

PM & PX-SERIES
MODELS-B & C
5V THRU 28V

$R_P \cong 100\Omega/V$, $C \cong 2.5\mu F$

$R_P \cong 200\Omega/V$ $C \cong 2.5\mu F$
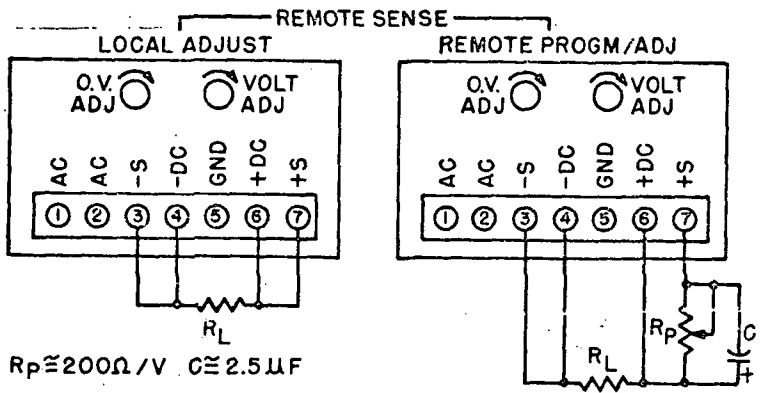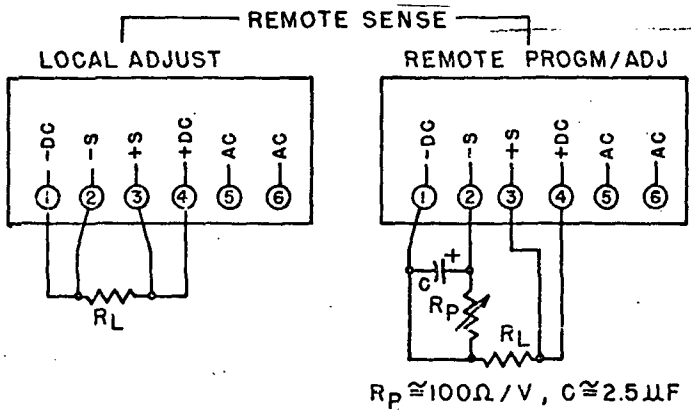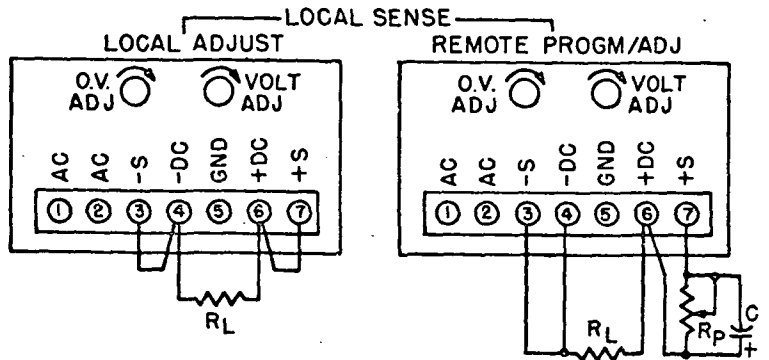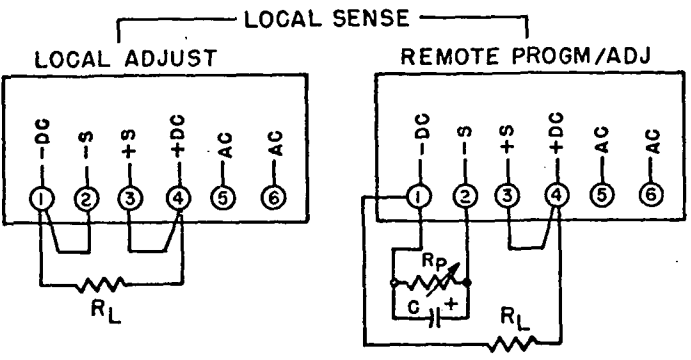
PM-SERIES, MODELS-CC, D, E
PX-SERIES, MODEL-CC
5 VOLTS THRU 28 VOLTS

PX-SERIES
MODELS-D, E, EE

E: $R_P \cong 200\Omega/V$, $C \cong 2.5\mu F$

$R_P = 200\Omega/VOLT$, $C = 2.5\mu F$
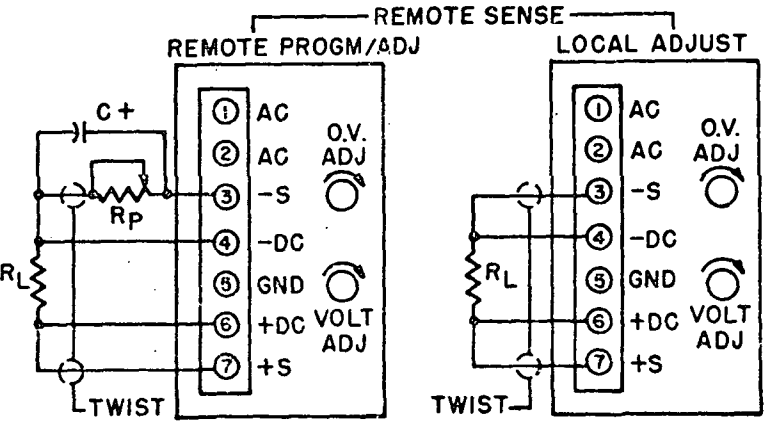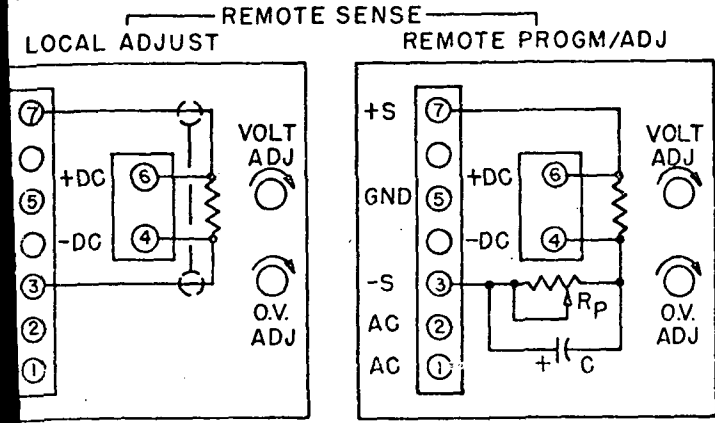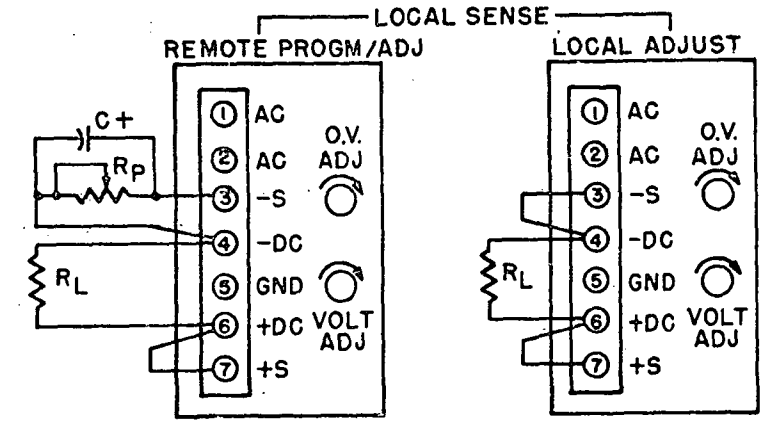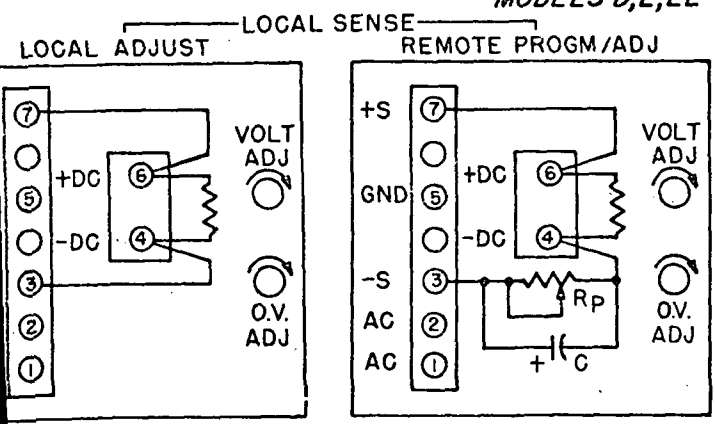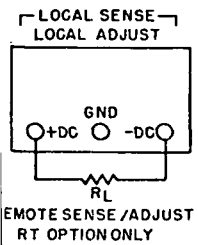
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MODEL-C,D

BP-SERIES
MODEL-E
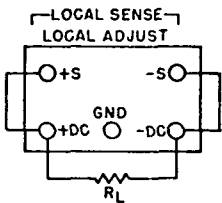
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MODELS-F,G,H
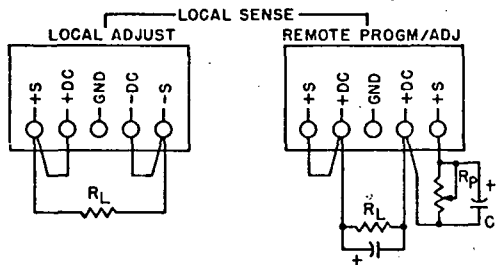
UNI-164
PT-B SERIES
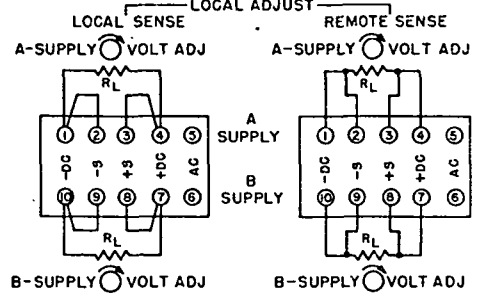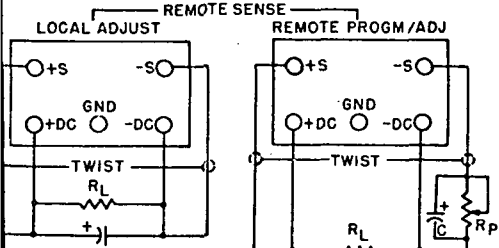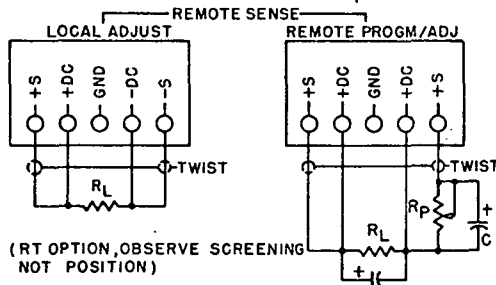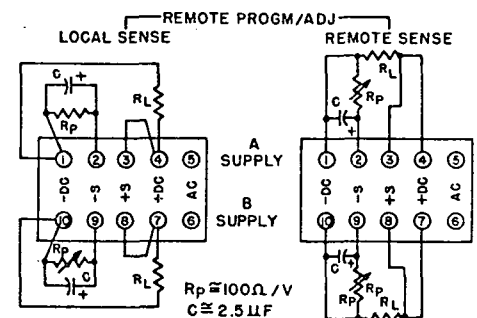
MODEL-E

ORIGINAL PAGE IS
OF POOR QUALITY

PT-SERIES
MODEL-B
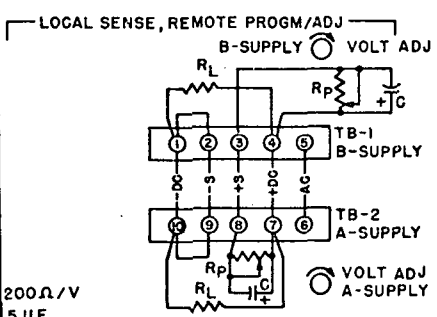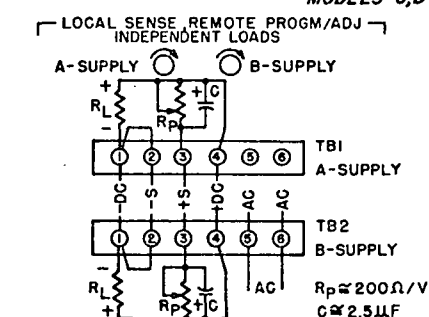
PT-SERIES
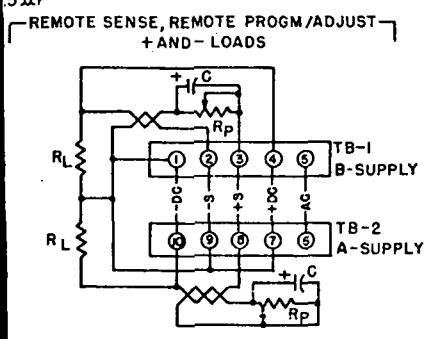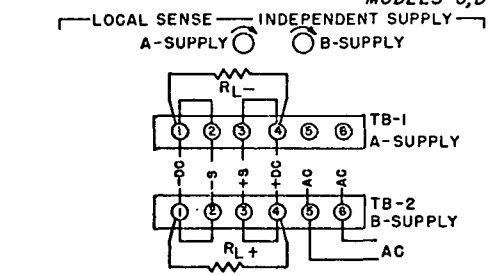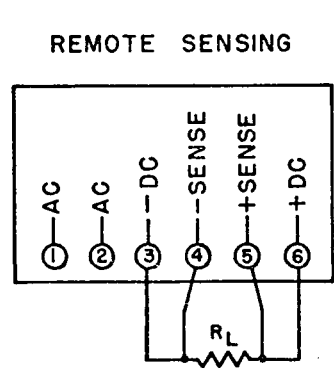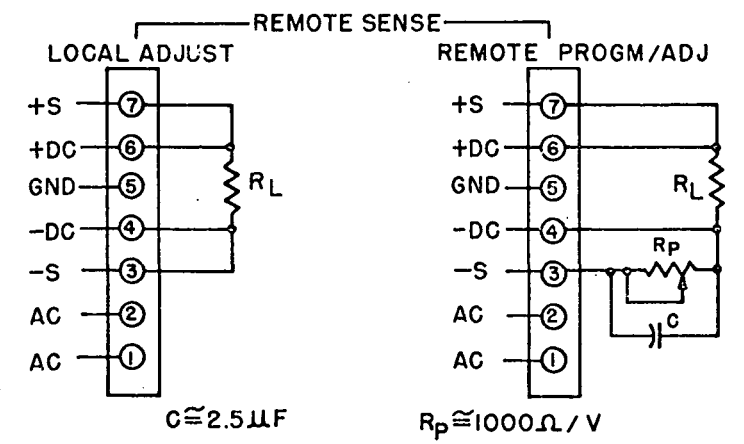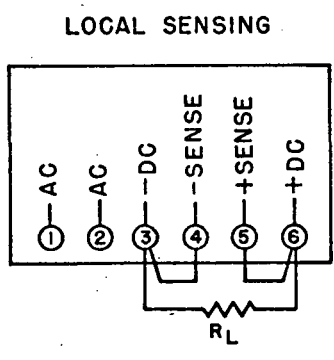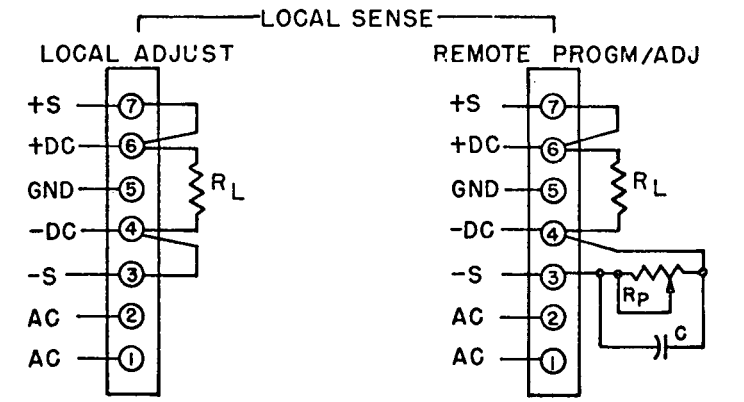MODELS-C,D
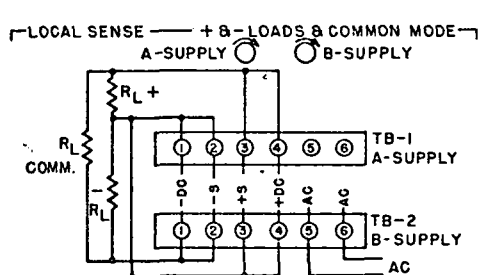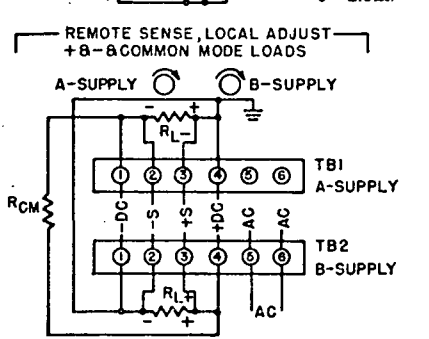
PT-SERIES
MODELS-C,D

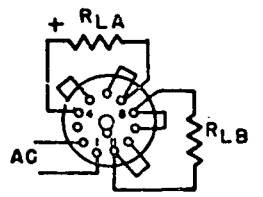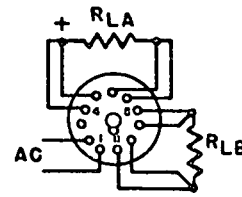OEM-SERIES,
PR-SERIES
MODELS-K,L,J

PR-SERIES
MODEL-H

HE-SERIES

ICX-SERIES

RA SERIES
LOCAL SENSE
LOCAL ADJUST — REMOTE ADJUST

+ LOAD –
AC INPUT

+ LOAD –
AC INPUT
C
RI

REMOTE SENSE
LOCAL ADJUST — REMOTE ADJUST

+ LOAD –
AC INPUT

+ LOAD –
AC INPUT
C
RI

RB SERIES
LOCAL ADJUST — REMOTE ADJUST

+ LOAD –
AC INPUT

+ LOAD –
AC INPUT
C
RI

RC/RD SERIES
LINE AND LOAD CONNECTIONS

+ LOAD –
AC INPUT
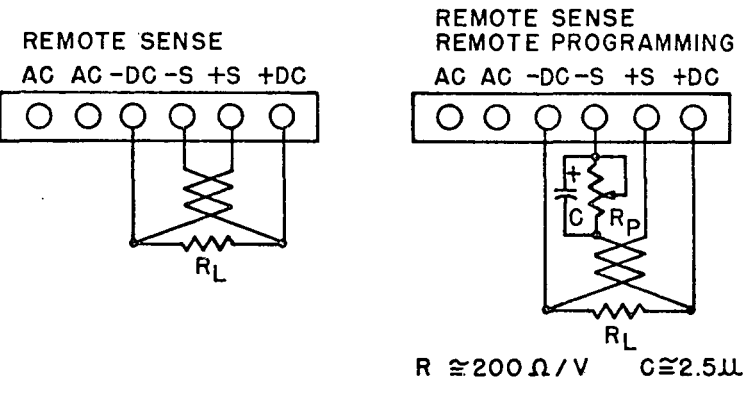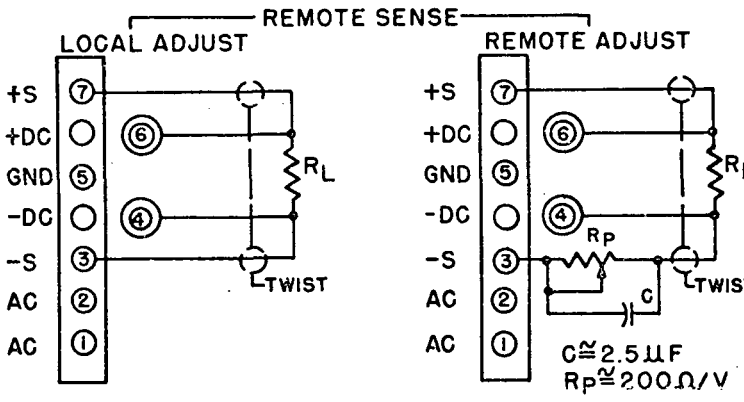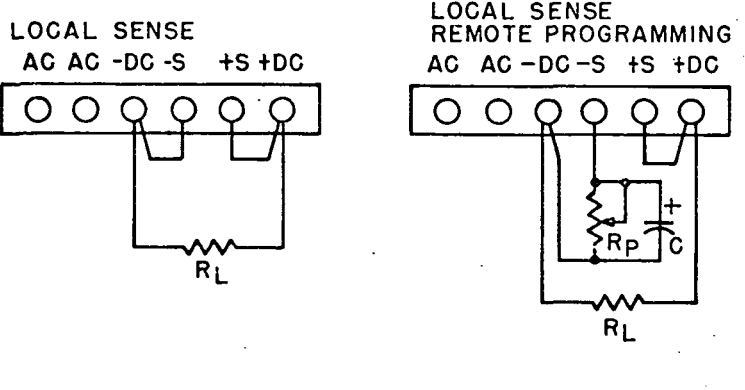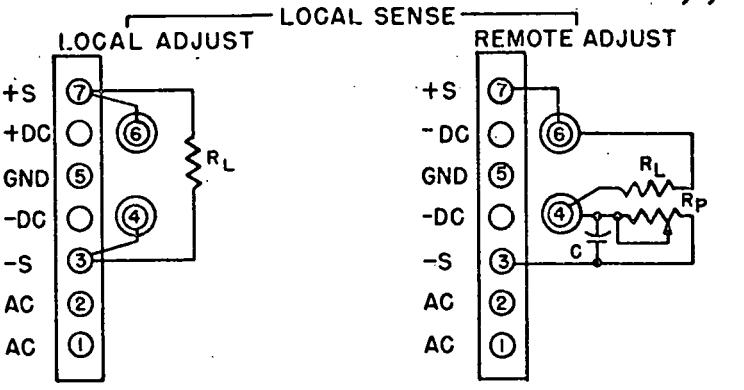
REMOTE SENSE
+ R_{LA}
AC
R_{LB}

LOCAL SENSE
+ R_{LA}
AC
R_{LB}

RA/RB–SERIES 12A & 25A
LOCAL SENSE
LOCAL ADJUST — REMOTE PROGM/ADJ

+ R_L
4 7
1 10
AC

+ R_L
4 7
1 10
AC
+ C
RI

REMOTE SENSE
LOCAL ADJUST — REMOTE PROGM/ADJ

+ R_L
4 7
1 10
AC

+ R_L
4 7
1 10
AC
+ C
RI
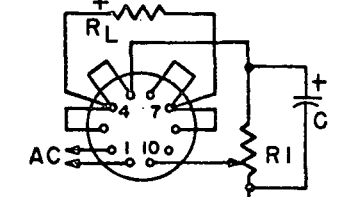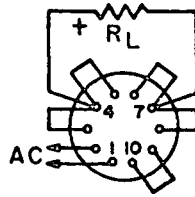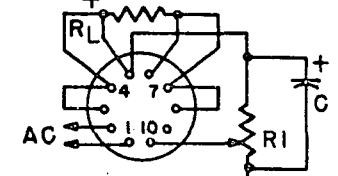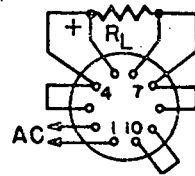
NOTE:
RI–500 Ω POT FOR MODELS PREFIXED RA2 THRU RA8, RA/RB2 THRU RB8
RI–5000 Ω POT FOR MODELS PREFIXED RA10 THRU RA59, RA/RB10 THRU RB385
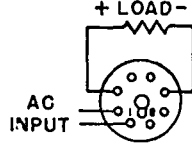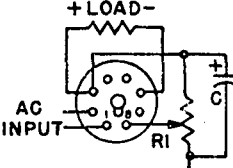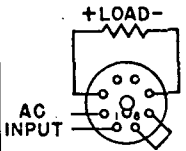
CP-SERIES 4V THRU 8V
LOCAL SENSE
+S +DC AC –DC –S
R_L
AC

REMOTE SENSE
+S +DC AC –DC –S
R_L
AC
TWIST FOR MINIMUM HUM PICKUP

REMOTE PROGM/ADJUST
+S +DC AC –DC –S
R_P C
R_L
AC
TRIM TO INCREASE VOLTAGE
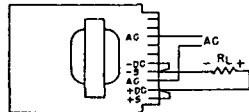
CP-SERIES 9V THRU 15V
LOCAL SENSE
AC
–DC AC +DC +S
AC
R_L +
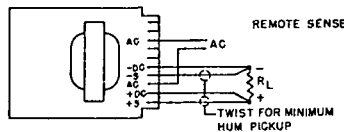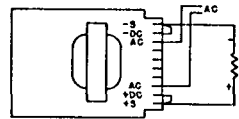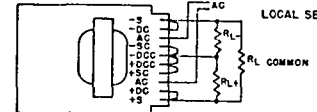
REMOTE SENSE
AC
–DC AC +DC +S
AC
R_L +
TWIST FOR MINIMUM HUM PICKUP

REMOTE PROGM/ADJUST
AC
–DC AC +DC +S
AC
R_L +
R_P
TRIM TO INCREASE VOLTAGE
C ≈ 2.5 μF

CP-SERIES 16V THRU 50V
LOCAL SENSING
–S –DC AC
AC
R_L
+

REMOTE SENSING
–S –DC AC +DC +S
AC
R_L
TWIST FOR MINIMUM HUM PICKUP

REMOTE TRIMMING
–S –DC AC
C R_T
AC +DC +S
R_L
AC
C ≈ 2.5 μF

DCP-SERIES
LOCAL SENSING
–S –DC AC –SC –DCC –DCG +SC +DC AC +DC +S
R_L COMMON
R_L
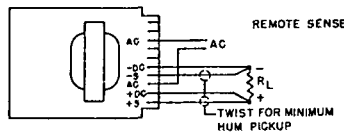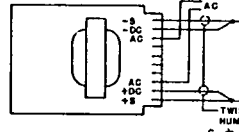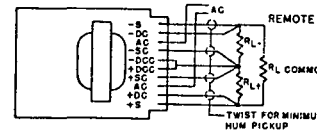
REMOTE SENSING
R_L COMMON
R_L
TWIST FOR MINIMUM HUM PICKUP
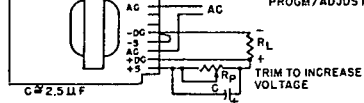
REMOTE TRIMMING
C R_T
R_L
R_L COMMON
R_L
AC
C ≈ 2.5 μF
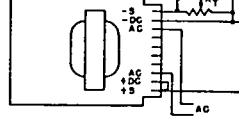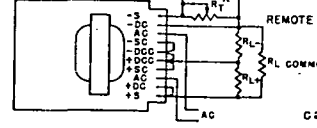
NOTES:
1. ALL CAPACITOR VOLTAGES ≧ VOLTAGE OF SUPPLY
2. TWIST ALL REMOTE SENSING LEADS
3. TERMINATE ALL REMOTE SENSING LEADS AT 2 μF CAPACITOR MINIMUM

4. REMOTE ADJUST: ADJUST INTERNAL POT TO MINIMUM VOLTAGE REQUIRED, ADD REQUIRED R_P TO BRING VOLTAGE UP TO MAXIMUM REQUIRED VOLTAGE. TRIM R_P TO ACTUAL VOLTAGE REQUIRED.

1024 x 1 BIT DYNAMIC
MOS Random Access Memory

MOSTEK

FEATURES

☐ 1024x1 RAM in 16-pin package
☐ Functionally equivalent to Mostek MK4006/4008 RAM's

DESCRIPTION

This 1024x1 Bit Dynamic Ram is selected from Mostek's MK4006 and MK4008 RAMs. See the MK4006/4008 data sheet for additional information, including timing diagrams.

FUNCTIONAL DIAGRAM
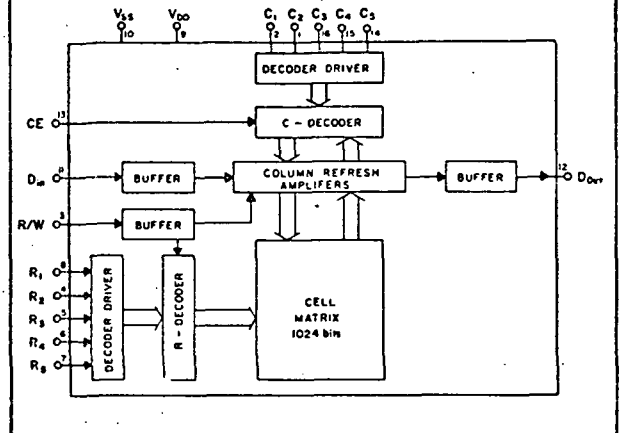
ABSOLUTE MAXIMUM RATINGS

Voltage on any pin (except V_{GG}) relative to V_{SS} ....+0.3 to −10V

Voltage on V_{GG} pin relative to V_{SS} ....+0.3 to −20V

Operating Temperature ....0 °C to +70°C

Storage Temperature Range ....−55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS
(0° C < T_A < 70°C)

	PARAMETER	MIN	MK 4008,-9 P MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.25	V	
V_{DD}	Supply Voltage	−11.4	−12.6	V	
V_{IL}	Input Voltage, Logic 0		+0.8	V	
V_{IH}	Input Voltage, Logic 1	V_{SS}−1	V_{SS}	V	

RECOMMENDED AC OPERATING CONDITIONS[1]
(0° C < T_A < 70°C)

	PARAMETER	MK 4008-9 P MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	800		ns	
t_{WC}	Write Cycle Time (Fig. 2)	1		us	t_{WP}= 450 ns
t_{WP}	Write Pulse Width (Fig. 2)	450		ns	t_{AW}=550 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	550		ns	t_{WP}=450 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	500		ns	t_{WP}=450 ns
t_{RDLY}	Refresh Time (Fig. 3)		1	ms	See Note 2

DC ELECTRICAL CHARACTERISTICS
(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C < T_A < 70° C unless otherwise noted)

	PARAMETER	MK 4008-9 P MIN	MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32	mA	Output
	At T_A=70°C		27	mA	Open
I_{IH}	Input Current, Logic 1, Any Input	−5	+5	μA	$V_I = V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	μA	$V_I = 0.8V$
I_{OH}	Output Current, Logic 1	0.6		mA	Note 3
I_{OL}	Output Current, Logic 0		5	μA	

AC ELECTRICAL CHARACTERISTICS
(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C < T_A < 70° C unless otherwise noted)

	PARAMETER	MK 4008-9 P MIN	MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time		800	ns	Note 1
t_{CE}	Chip Enable Time		450	ns	Note 1
t_{CD}	Chip Disable Time		450	ns	
C_I	Input Capacitance, Any Input		5.0	pF	T_A=25°C; $V_I = V_{SS}$; f=1MHz
C_O	Output Capacitance		10	pF	T_A=25°C; $V_O = V_{SS}-5V$; f=1MHz

NOTES:

(1) Measurement Criteria: Input voltage swing, all inputs: 0.8V to V_{SS} — 1

Input rise and fall times: 20 ns

Measurement point on input signals: +1.5V above ground

Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

(2) t_{RDLY} is the time between refresh cycles for a given row address.

(3) Steady-state values. (Refer to Fig. 1A for clarification)

TIMING
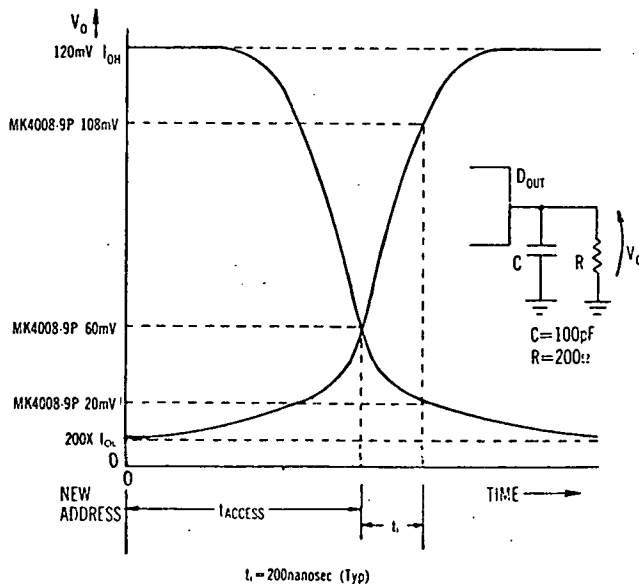
ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4008-9 P.

1024x1 BIT DYNAMIC
MOS Random Access Memory

MOSTEK

FEATURES:

☐ TTL/DTL compatible inputs

☐ No clocks required

☐ Access time:
   MK 4006, −6 P: under 400 ns
   MK 4008, −6 P: under 500 ns

☐ Standby power: under 50 mW

☐ 16-pin standard CDIP

☐ Supply voltage: +5V and −12V
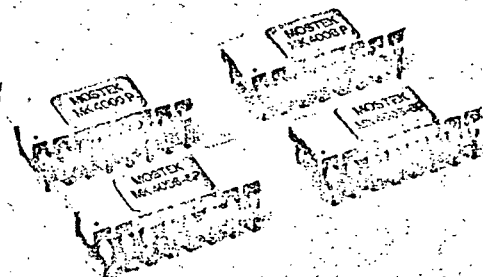
DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed and power-down capabilities. Access time in the MK 4006 P is less than 400 ns; in the MK 4008 P, less than 500 ns. The MK 4006-6 P and the MK 4008-6 P are identical to the MK 4006 P and MK 4008 P, respectively, except that they are specially tested for power down operation.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs, and the memory itself does not exhibit large supply current transients.

Data output is single-ended to minimize propagation delay. Output current is sourced from V_{ss} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

C_2 1	16 C_3
C_1 2	15 C_4
R/W 3	14 C_5
R_2 4	13 $\overline{CE}$
R_3 5	12 D_{OUT}
R_4 6	11 D_{IN}
R_5 7	10 V_{SS} +5
R_1 8	9 V_{DD} −12

0
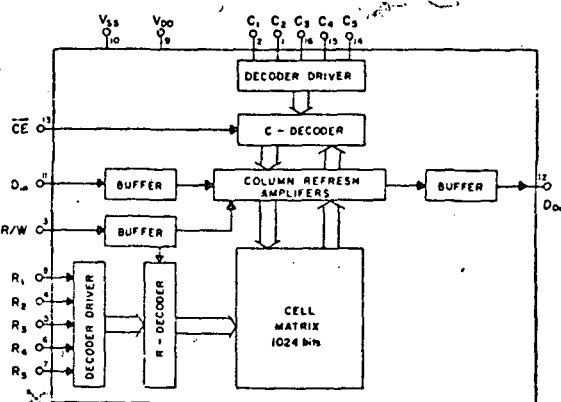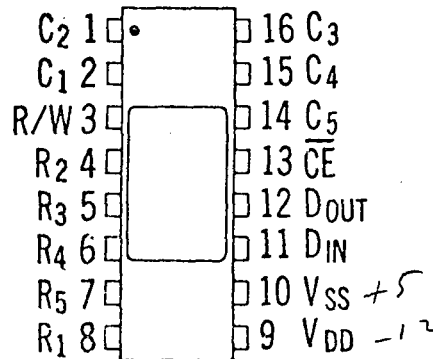
ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} .... +0.3 to −20V

Operating Temperature .... 0°C to +70°C

Storage Temperature Range .... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS
(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MAX	MK 4008 P MK 4008-6 P MIN	MAX	UNITS	NOTES
V_{SS}	Supply Voltage		+4.75		+5.25	V	
V_{DD}	Supply Voltage		−11.4		−12.6	V	
V_{IL}	Input Voltage, Logic 0				+0.8	V	
V_{IH}	Input Voltage, Logic 1		$V_{SS}-1$		V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)		$V_{SS}-4$		$V_{SS}-6$	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]
(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MAX	MK 4008 P MK 4008-6 P MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650		900		ns ns	$t_{WP}=250$ ns $t_{WP}=400$ ns
t_{WP}	Write Pulse Width (Fig. 2)	250		400		ns ns	$t_{AW}=400$ ns $t_{AW}=500$ ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400		500		ns ns	$t_{WP}=250$ ns $t_{WP}=400$ ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300		400		ns ns	$t_{WP}=250$ ns $t_{WP}=400$ ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS
(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C $\leq T_A \leq$ 70°C unless otherwise noted)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MAX	MK 4008 P MK 4008-6 P MIN	MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At $T_A=0$°C		32		32	mA	Output
	At $T_A=70$°C		27		27	mA	Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	$V_I=0.8V$
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

AC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless otherwise noted)

	PARAMETER	MK 4006 P MK 4006-6 P MIN	MK 4006 P MK 4006-6 P MAX	MK 4008 P MK 4008-6 P MIN	MK 4008 P MK 4008-6 P MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time (Fig. 1 & 1-A)		400		500	ns	Note 2
t_{CE}	Chip Enable Time (Fig. 1A & 5)		350		450	ns	Note 2
t_{CD}	Chip Disable Time (Fig. 1A & 5)		350		450	ns	
C_I	Input Capacitance, Any Input		5.0		5.0	pF	$T_A=25°C$; $V_I=V_{SS}$; $f=1MHz$
C_O	Output Capacitance		10		10	pF	$T_A=25°C$; $V_O=V_{SS}-5V$; $f=1MHz$
C_{DD}	V_{DD} Capacitance		75		75	pF	$T_A = 25°C$; Note 6

NOTES:

(1) Applies to MK 4006-6 and MK 4008-6 only.

(2) Measurement Criteria: Input voltage swing, all inputs: 0.8V to $V_{SS} - 1$
Input rise and fall times: 20 ns
Measurement point on input signals: $+1.5V$ above ground
Measurement point on output signal: $+60$ mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

(3) t_{RDLY} is the time between refresh cycles for a given row address.

(4) A V_{DD} rise time of 20 ns is assumed. Longer rise times will lower the minimum value of t_{CDPD} required.

(5) Steady-state values. (Refer to Fig. 1A for clarification)

(6) Average capacitance of the V_{DD} terminal relative to the V_{SS} terminal. Measured by switching the V_{DD} terminal from 0V to $-12V$ with an applied $V_{SS} = 5V$. Peak I_{DD} is observed and the circuit replaced by a capacitance which yields the same peak current as the circuit under test.

TIMING (Note 2)
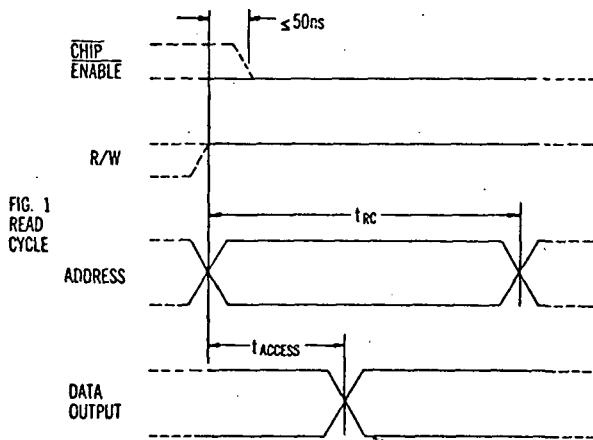
READING (Fig. 1)

Reading is accomplished with the Read/Write input held high. Data output directly follows the application of an address. As long as the address is unchanged and the chip enabled, data output will remain valid until the next refresh cycle. Input addresses can be changed as soon as output data is accessed. Any address can be applied repetitively without degrading stored data, providing that the refresh period of 2 ms is observed.
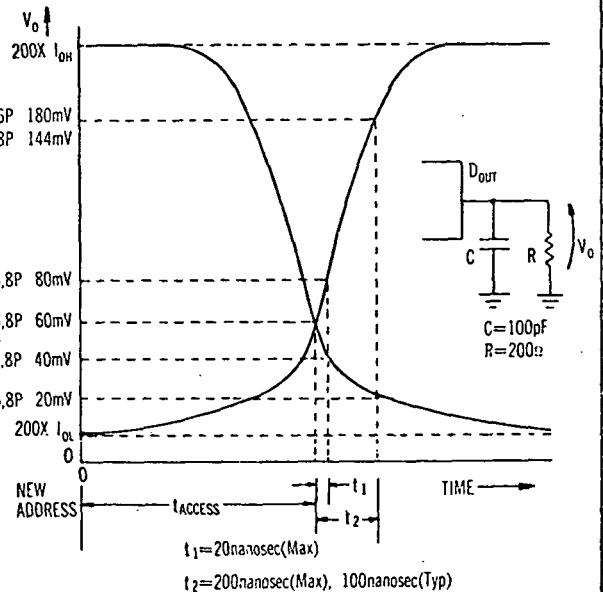
ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

TIMING
(Note 2)

WRITING (Fig. 2)

Writing is accomplished by bringing the Read/Write input low with valid data present at the data input and the Chip-Enable input low (chip enabled). Following the return of the Read/Write line to a high state, new address and input data can be applied. If a read-after-write operation is desired, valid data will appear at the output within one read access time following the rising edge of the Write Pulse. Read-modify-write operation is easily achieved by delaying the Write Pulse until data has been read and modification is complete.

REFRESHING (Figs. 2 & 3))

The dynamic memory cell employed in the MK 4006 P and MK 4008 P will not store data indefinitely. Stored data must be written back into the cell at least once every 2 ms. Rewriting is accomplished internally without the need to reapply external data. This rewriting operation is called *refreshing*.

Refreshing of the MK 4006 P and MK 4008 P is accomplished during both *write cycles* and *refresh cycles*. During a write cycle the state of the Row Address (R_1-R_5) determines which of the 32 memory matrix rows will be internally refreshed. An entire row (32 bits) is refreshed during one write cycle. Since it is difficult in practice to assure that each of the 32 possible R addresses is associated with a write cycle in every 2 ms period, a separate refresh cycle is normally employed.

The refresh cycle is identical to the write cycle except that the chip is disabled while the Read/Write line is pulsed. Disabling the chip removes the data output and prevents data at the data input from being written into the memory. An entire refresh cycle consists of 32 address changes and associated write pulses, involving a total time of approximately 20 microseconds.

STANDBY MODE (Fig. 4)

Power dissipation of the MK 4006-6 P and MK 4008-6 P can be reduced below 50 mW without loss of stored data by lowering the V_{DD} supply voltage to system ground (V_{SS}-5V). Figure 4 illustrates the proper input conditions that should be observed when reducing V_{DD}. If the standby mode is maintained as long as 2 milliseconds, the V_{DD} supply should be returned to −12V and a refresh cycle initiated. Read or write cycles can commence immediately following the return of V_{DD} to −12V.
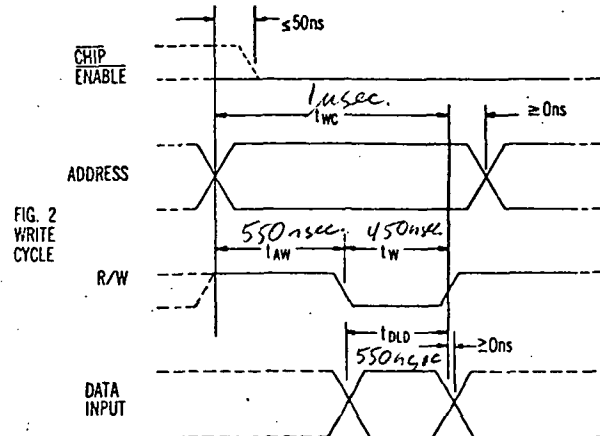
FIG. 2 WRITE CYCLE
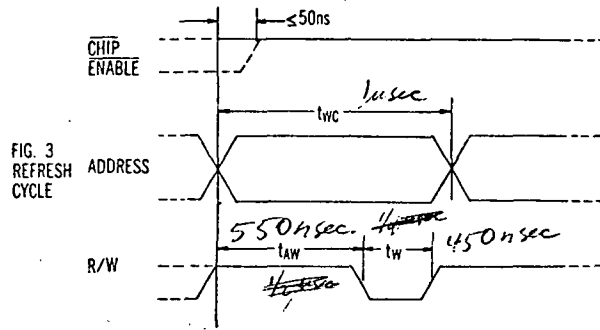
FIG. 3 REFRESH CYCLE
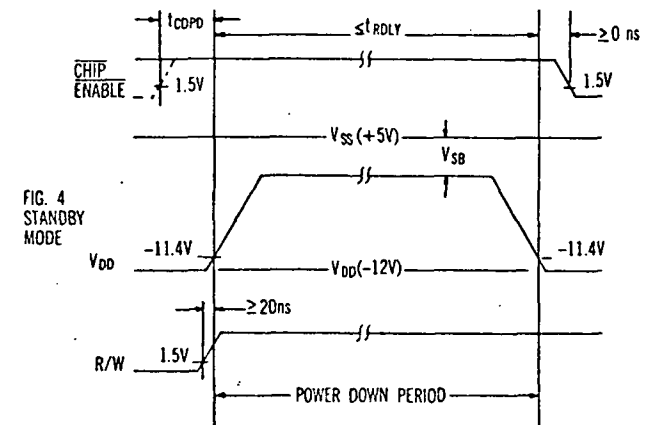
FIG. 4 STANDBY MODE

TIMING
(Note 2)

CHIP ENABLING (Fig. 5)

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.
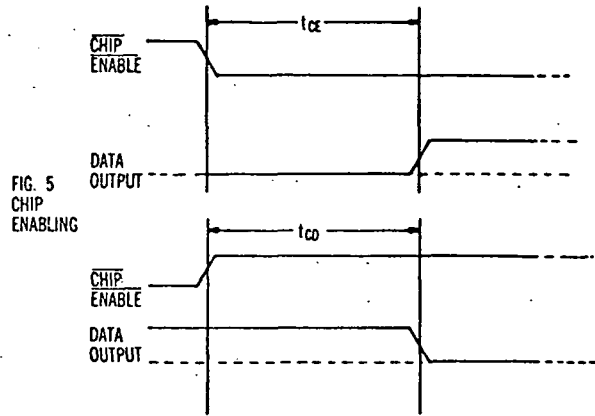
FIG. 5
CHIP
ENABLING

TESTING CONSIDERATIONS

For a complete discussion of testing this memory, see Mostek's Applications Note AN-103.

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from binary equivalent to column address.
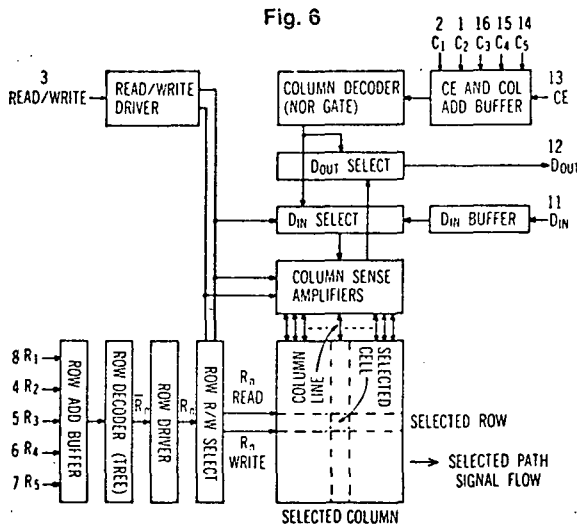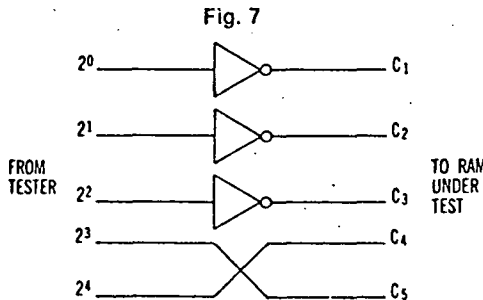
TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test[1]	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby[1]	First	Write, Write	E	V-Bar, $\overline{\text{V-Bar}}$	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

Fig. 6

Fig. 7

FROM TESTER   TO RAM UNDER TEST

PACKAGE (16-lead ceramic dual-in-line hermetic package)
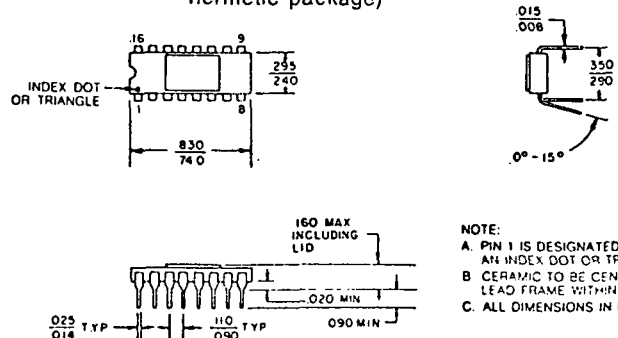
NOTE:
A. PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B. CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C. ALL DIMENSIONS IN INCHES

ORDERING INFORMATION

MK 4006 P: 1024x1 RAM/w/400 ns access time
MK 4008 P: 1024x1 RAM/w/500 ns access time
MK 4006-6 P: Power-down version of MK 4006 P
MK 4008-6 P: Power-down version of MK 4008 P

4

APPLICATION

SENSE AMPLIFIERS FOR MK 4006/4008 P RAM's

Since the interface circuitry used to convert memory signals to system logic levels strongly influences system access times, this circuitry should always be designed to meet the speed and cost requirements of the particular application.

Fig. 1-A (See "Timing") is shown to assist in the design of such amplifiers. This figure shows output voltage (across a specified load) vs. time from application of new address with several points indicated where specified voltage levels are referenced to specific times. Although all the various access times vs. output current levels cannot be shown, a few guidelines are given for interpolation between the specified points.

In Fig. 1-A, the two points at $t_{access} + 20$ nsec give the minimum "1" level and the maximum "0" level for this particular time (80 mV and 40 mV respectively). At $t_{access} + 200$ nsec, voltage levels are specified for the 90% and 10% points of the minimum "1" and maximum "0" levels.

INTERPOLATION

These interpolation guidelines are selected to give the designer a high level of confidence in his sense amplifier design.
From O to 1: This portion of the access curve can be estimated by two linear portions: (1) from the 60 mV to the 80 mV level; and (2) from the 80 mV level to 180/144 mV level.
From 1 to O: This portion of the access curve can be estimated by a semi-logarithmic plot decreasing 20 mV for each decade or 10 nsec of time added to t_{access}, with the end points being 60 mV at 2 nsec and 20 mV at 200 nsec.

EXAMPLE: Let us consider how this data can be used in a sense amplifier design utilizing the 75107/108 Dua-Line-Receiver-and-Driver.

The manufacturer's data sheet for this circuit shows us that at strobe time, three conditions of the line receiver can exist: (1) the input voltage differential can be more positive than 25 mV, resulting in a logic 1 at the output (Input differential voltage is referenced to the inverting terminal); (2) the input differential can be more negative than 25 mV, resulting in a logic O at the output; (3) the input differential is less than 25 mV (absolute value), which will result in an output of an undetermined state. In other words, the line receiver has a 50 mV "window" centered around zero, and a signal must fall outside this window to provide reliable information at the output.

The standard configuration for using the 75107/108 as a sense amp is shown in Fig. 8 with the voltage and current conventions used in this analysis.

FIG. 8: Illustrating use of 75107/108 Line Receivers as sense amplifiers for the MK 4006/4008 P.
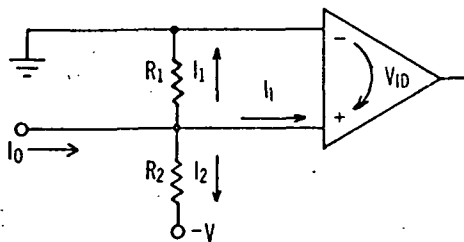
From the worst-case access at the *chip* level, one can use the interpolation technique described above to determine maximum "O" current level $[I_{OLC}(MAX)]$ and the minimum "1" current level $[I_{OH}(MIN)]$.

However, to use a worst-case approach to this design, in addition to the chip's characteristics, one must include in the "O" level current the effect of leakage from all outputs that are wired together. Also the input currents required by the 75107/108 (75 mA and 10 mA) must be included. Let us call this $I_{OLT}(MAX)$:

$$I_{OLT}(MAX) = I_{OLC}(MAX) + (N\text{-}1) (5\ \mu A) \qquad [1]$$

where N = number of outputs wired together

Using the maximum zero level at the line receiver input ($V_{ID} \leq -25mV = V_{ID}^-$), the following equation is derived:

$$I_{OLT}(MAX) = I_1 - I_2 + I_{IL}(MIN)$$
$$\text{and } I_{IL}(MIN) = 0\ \mu A \qquad [2]$$

therefore:

$$I_{OLT}(MAX) = \frac{V_{ID}^-}{R1} + \frac{V + V_{ID}^-}{R2} \qquad [3]$$

Using the minimum "1" level at the line receiver input ($V_{ID} \geq +25\ mV = V_{ID}^+$), the equation becomes

$$I_{OH}(MIN) = I_1 - I_2 + I_{IH}(MAX) \qquad [4]$$
$$\text{and } I_{IH}(MAX) = 75\ \mu A$$

$$I_{OH}(MIN) = \frac{V_{ID}^+}{R1} + \frac{V + V_{ID}^+}{R2} + 75\ \mu A \qquad [5]$$

Solving these equations ([3] and [5]) simultaneously yields R1 and R2.
As an example, assume a memory system with 4 outputs wired-ORed to a sense amplifier, requiring a chip access time of 460 nsec. Then the associated current and resistor values are:

$$I_{OLT}(MAX) = 152.3\ \mu A + 3\ (5\ \mu A) = 167.3\ \mu A$$
$$I_{OH}(MIN) = 511.12\ \mu A$$

Therefore:

$$R1 = 190\ \Omega$$
$$R2 = 16.5\ K\Omega$$

Sense amplifiers vary from the very fast, low-threshold types to the slower, high-threshold kind. The ideal choice will depend on the application. Fig. 1-A and the guidelines in this note are intended to help the designer tailor his sense amplifier design to meet the speed and cost requirements of his particular application.

It should also be noted that a portion of the output current from the memory chip is used to charge the capacitance on the data output. If the output impedance differs greatly from the specified load, this current must also be calculated.

APPENDIX C

DIGITAL INTERFACE CONTROL BIT ASSIGNMENTS

DIGITAL INTERFACE NO. __One__

WORD __0__

BIT	SIGNAL NAME	TO
0	Red Input Enhancement Data LSB 6	Red Enhancement Table
1	Red Input Enhancement Data 5	Red Enhancement Table
2	Red Input Enhancement Data 4	Red Enhancement Table
3	Red Input Enhancement Data 3	Red Enhancement Table
4	Red Input Enhancement Data 2	Red Enhancement Table
5	Red Input Enhancement Data MSB 1	Red Enhancement Table
6	Green Input Enhancement Data LSB 6	Green Enhancement Table
7	Green Input Enhancement Data 5	Green Enhancement Table
8	Green Input Enhancement Data 4	Green Enhancement Table
9	Green Input Enhancement Data 3	Green Enhancement Table
10	Green Input Enhancement Data 2	Green Enhancement Table
11	Green Input Enhancement Data MSB 1	Green Enhancement Table
12	Blue Input Enhancement Data LSB 6	Blue Enhancement Table
13	Blue Input Enhancement Data 5	Blue Enhancement Table
14	Blue Input Enhancement Data 4	Blue Enhancement Table
15	Blue Input Enhancement Data 3	Blue Enhancement Table
16	Blue Input Enhancement Data 2	Blue Enhancement Table
17	Blue Input Enhancement Data MSB 1	Blue Enhancement Table
18	Load Sequencer Clock	Digital Multiplexer
19	Load Sequencer Reset	Digital Multiplexer
20	Channel TWO Write Enable	Red, Green, & Blue Enhancement Table
21	Channel THREE Write Enable	Red, Green & Blue Enhancement Table
22	Channel ONE Write Enable	Red, Green & Blue Enhancement Table

DIGITAL INTERFACE NO. __One__

WORD __1__

BIT	SIGNAL NAME	TO
0	Red Grid Data LSB 6	Red Enhancement Table
1	Red Grid Data 5	Red Enhancement Table
2	Red Grid Data 4	Red Enhancement Table
3	Red Grid Data 3	Red Enhancement Table
4	Red Grid Data 2	Red Enhancement Table
5	Red Grid Data MSB 1	Red Enhancement Table
6	Green Grid Data LSB 6	Green Enhancement Table
7	Green Grid Data 5	Green Enhancement Table
8	Green Grid Data 4	Green Enhancement Table
9	Green Grid Data 3	Green Enhancement Table
10	Green Grid Data 2	Green Enhancement Table
11	Green Grid Data MSB 1	Green Enhancement Table
12	Blue Grid Data LSB 6	Blue Enhancement Table
13	Blue Grid Data 5	Blue Enhancement Table
14	Blue Grid Data 4	Blue Enhancement Table
15	Blue Grid Data 3	Blue Enhancement Table
16	Blue Grid Data 2	Blue Enhancement Table
17	Blue Grid Data MSB 1	Blue Enhancement Table

DIGITAL INTERFACE NO. ___One___

WORD _____2_____

BIT	SIGNAL NAME	TO
0	Red Cursor Data LSB 6	Red Enhancement Table
1	Red Cursor Data 5	Red Enhancement Table
2	Red Cursor Data 4	Red Enhancement Table
3	Red Cursor Data 3	Red Enhancement Table
4	Red Cursor Data 2	Red Enhancement Table
5	Red Cursor Data MSB 1	Red Enhancement Table
6	Green Cursor Data LSB 6	Green Enhancement Table
7	Green Cursor Data 5	Green Enhancement Table
8	Green Cursor Data 4	Green Enhancement Table
9	Green Cursor Data 3	Green Enhancement Table
10	Green Cursor Data 2	Green Enhancement Table
11	Green Cursor Data MSB 1	Green Enhancement Table
12	Blue Cursor Data LSB 6	Blue Enhancement Table
13	Blue Cursor Data 5	Blue Enhancement Table
14	Blue Cursor Data 4	Blue Enhancement Table
15	Blue Cursor Data 3	Blue Enhancement Table
16	Blue Cursor Data 2	Blue Enhancement Table
17	Blue Cursor Data MSB 1	Blue Enhancement Table

DIGITAL INTERFACE NO. One

WORD 3

BIT	SIGNAL NAME	TO
0	Grid Channel Select one	Digital Multiplexer
1	Grid Channel Select two	Digital Multiplexer
2	Grid Channel Select three	Digital Multiplexer
3	Grid Channel Select four	Digital Multiplexer
4	Grid Channel Select five	Digital Multiplexer
5	Grid Channel Select six	Digital Multiplexer
6	Grid Channel Select seven	Digital Multiplexer
7	Grid Channel Select eight	Digital Multiplexer
8	Cursor Channel Select one	Digital Multiplexer
9	Cursor Channel Select two	Digital Multiplexer
10	Cursor Channel Select three	Digital Multiplexer
11	Cursor Channel Select four	Digital Multiplexer
12	Cursor Channel Select five	Digital Multiplexer
13	Cursor Channel Select six	Digital Multiplexer
14	Cursor Channel Select seven	Digital Multiplexer
15	Cursor Channel Select eight	Digital Multiplexer
16	Matting Channel Select one	Digital Multiplexer
17	Matting Channel Select two	Digital Multiplexer
18	Matting Channel Select three	Digital Multiplexer
19	Matting Channel Select four	Digital Multiplexer
20	Matting Channel Select five	Digital Multiplexer
21	Matting Channel Select six	Digital Multiplexer
22	Matting Channel Select seven	Digital Multiplexer
23	Matting Channel Select eight	Digital Multiplexer

DIGITAL INTERFACE NO. One

Word 5

BIT	SIGNAL NAME	TO
0	Channel One Analog Select 1	Analog Distributor
1	Channel One Analog Select 2	Analog Distributor
2	Channel One Analog Select 3	Analog Distributor
3	Channel One Analog Select 4	Analog Distributor
4	Channel One Analog Select 5	Analog Distributor
5	Channel One Analog Select 5 6	Analog Distributor
6	Channel One Analog Select 6 7	Analog Distributor
7	Channel One Analog Select 7 8	Analog Distributor
8	Channel One Analog Select 8 9	Analog Distributor
9	Channel One Analog Select 9 10	Analog Distributor
10	Channel One Analog Gain Half	Analog Distributor
11	channel One Analog Gain Third	Analog Distributor
12	Channel Two Analog Select 1	Analog Distributor
13	Channel Two Analog Select 2	Analog Distributor
14	Channel Two Analog Select 3	Analog Distributor
15	Channel Two Analog Select 4	Analog Distributor
16	Channel Two Analog Select 5	Analog Distributor
17	Channel Two Analog Select 6	Analog Distributor
18	Channel Two Analog Select 7	Analog Distributor
19	Channel Two Analog Select 8	Analog Distributor
20	Channel Two Analog Select 9	Analog Distributor
21	Channel Two Analog Select 10	Analog Distributor
22	Channel Two Analog Gain Half	Analog Distributor
23	Channel Two Analog Gain Third	Analog Distributor

BIT	SIGNAL NAME	TO
0	Channel Three Analog Select 1	Analog Distributor
1	Channel Three Analog Select 2	Analog Distributor
2	Channel Three Analog Select 3	Analog Distributor
3	Channel Three Analog Select 4	Analog Distributor
4	Channel Three Analog Select 5	Analog Distributor
5	Channel Three Analog Select 6	Analog Distributor
6	Channel Three Analog Select 7	Analog Distributor
7	Channel Three Analog Select 8	Analog Distributor
8	Channel Three Analog Select 9	Analog Distributor
9	Channel Three Analog Select 10	Analog Distributor
10	Channel Three Analog Gain Half	Analog Distributor
11	Channel Three Analog Gain Third	Analog Distributor
12	Single Channel Select One	Video Sequencer
13	Single Channel Select Two	Video Sequencer
14	Single Channel Select Three	Video Sequencer
15	Super Two Control	Video SEquencer
16	Super THree Control	Video Sequencer
17	Address Mux One Read	Address Multiplexer
18	Address Mux One Write	Address Multiplexer
19	Address Mux Two Read	Address Multiplexer
20	Address Mux Two Write	Address Multiplexer
21	Address Mux Three Read	Address Multiplexer
22	Address Mux Three Write	Address Multiplexer
23	Matting Control	Video Sequencer

DIGITAL INTERFACE NO.____Two____

WORD_____0____

BIT	SIGNAL NAME	TO
0	Cursor Vertical Size 1	Digital Cursor
1	Cursor Vertical Size 2	Digital Cursor
2	Cursor Vertical Size 4	Digital Cursor
3	Cursor Vertical Size 8	Digital Cursor
4	Cursor Vertical Size 16	Digital Cursor
5	Cursor VErtical Size 32	Digital Cursor
6	Cursor Vertical Size 64	Digital Cursor
7	Cursor Vertical Size 128	Digital Cursor
8	Cursor Horizontal Size 1	Digital Cursor
9	Cursor Horizontal Size 2	Digital Cursor
10	Cursor Horizontal Size 4	Digital Cursor
11	Cursor Horizontal Size 8	Digital Cursor
12	Cursor Horizontal Size 16	Digital Cursor
13	Cursor Horizontal Size 32	Digital Cursor
14	Cursor Horizontal Size 64	Digital Cursor
15	Cursor Horizontal Size 128	Digital Cursor
16	Cursor Select Rectangular Area	Digital Cursor
17	Cursor Select Rectangular Outline	Digital Cursor
18	Cursor Select Crosshair	Digital Cursor

DIGITAL INTERFACE NO.___Two____

WORD____2____

BIT	SIGNAL NAME	TO
0	Cursor Position Line Number 1	Digital Cursor
1	Cursor Position Line Number 2	Digital Cursor
2	Cursor Position Line Number4	Digital Cursor
3	Cursor Position Line Number 8	Digital Cursor
4	Cursor Position Line Number 16	Digital Cursor
5	Cursor Position Line Number 32	Digital Cursor
6	Cursor Position Line Number 64	Digital Cursor
7	Cursor Position Line Number 128	Digital Cursor
8	Cursor Position Line Number 256	Digital Cursor
9	Cursor Position Line Number 512	Digital Cursor
10	Cursor Position Pixel Number 1	Digital Cursor
11	Cursor Position Pixel Number 2	Digital Cursor
12	Cursor Position Pixel Number 4	Digital Cursor
13	Cursor Position Pixel Number 8	Digital Cursor
14	Cursor Position Pixel Number 16	Digital Cursor
15	Cursor Position Pixel Number 32	Digital Cursor
16	Cursor Position Pixel Number 64	Digital Cursor
17	Cursor Posititon Pixel Number 128	Digital Cursor
18	Cursor Position Pixel Number 256	Digital Cursor
19	Cursor Position Pixel Number 512	Digital Cursor

DIGITAL INTERFACE NO. __Two__

WORD __3__

BIT	SIGNAL NAME	TO
0	Level Discriminator One Analog Video Select 1	Level Discriminator One
1	Level Discriminator One Analog Video Select 2	Level Discriminator One
2	Level Discriminator One Analog Video Select 3	Level Discriminator One
3	Level Discriminator One Analog Video Select 4	Level Discriminator One
4		
5		
6		
7		
8		
9		
10		
11		
12	Level Discriminator One Upper Level Set 1	Level Discriminator One
13	Level Discriminator One Upper Level Set 2	Level Discriminator One
14	Level Discriminator One Upper Level Set 4	Level Discriminator One
15	Level Discriminator One Upper Level Set 8	Level Discriminator One
16	Level Discriminator One Upper Level Set 16	Level Discriminator One
17	Level Discriminator One Upper Level Set 32	Level Discriminator One
18	Level Discriminator One Lower Level Set 1	Level Discriminator One
19	Level Discriminator One Lower Level Set 2	Level Discriminator One
20	Level Discriminator One Lower Level Set 4	Level Discriminator One
21	Level Discriminator One Lower Level Set 8	Level Discriminator One
22	Level Discriminator One Lower Level Set 16	Level Discriminator One
23	Level Discriminator One Lower Level Set 32	Level Discriminator One

DIGITAL INTERFACE NO. __Two__

WORD __4__

BIT	SIGNAL NAME	TO
0	T.V. Line Number 1	Fast Storage
1	T.V. Line Number 2	Fast Storage
2	T.V. Line Number 4	Fast Storage
3	T.V. Line Number 8	Fast Storage
4	T.V. Line Number 16	Fast Storage
5	T.V. Line Number 32	Fast Storage
6	T.V. Line Number 64	Fast Storage
7	T.V. Line Number 128	Fast Storage
8	T.V. Line Number 256	Fast Storage
9	T.V. Line Number 512	Fast Storage
10	Data Word 32	Fast Storage
11	Data Word 16	Fast Storage
12	Data Word 8	Fast Storage
13	Data Word 4	Fast Storage
14	Data Word 2	Fast Storage
15	Data Word 1	Fast Storage
16	Load Clock	Fast Storage
17	End Loading Signal	Fast Storage

DIGITAL INTERFACE NO. __Two__

WORD __5__

BIT	SIGNAL NAME	TO
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16	Video Disk Modulator Enable. Signal System One	DR-10A Interface
17	Video Disk Modulator Enable. Signal System Two	DR-10A Interface
18	Video Disk Modulator Enable. Signal System Three	DR-10A Interface
19	Video Disk Modulator Enable. Signal System Four	DR-10A Interface
20	Video Disk Timing Track Playback Enable	DR-10A Interface
21	Video Disk Timing Track Record Enable	DR-10A Interface

BIT	SIGNAL NAME	TO
0	Video Disk Head Stepping System One Step	DR-10A Interface
1	Video Disk Head Stepping. System One Direction	DR-10A Interface
2	Video Disk Head Stepping System One Reset	DR-10A Interface
3	Video Disk Head Stepping System Two Step	Dr-10A Interface
4	Video Disk Head Stepping System Two Direction	DR-10A Interface
5	Video Disk Head Stepping System Two Reset	DR-10A Interface
6	Video Disk Signal System One Write Enable Head A	DR-10A Interface
7	Video Disk Signal System One Write Enable Head B	DR-10A Interface
8	Video Disk Signal System One Playback Enable Head A	DR-10A Interface
9	Video Disk Signal System One Playback Enable Head B	DR-10A Interface
10	Video Disk Signal System Two Write Enable Head A	DR-10A Interface
11	Video Disk Signal System Two Write Enable Head B	DR-10A Interface
12	Video Disk Signal System Two Playback Enable Head A	DR-10A Interface
13	Video Disk Signal System Two Playback Enable Head B	DR-10A Interface
14	Video Disk Signal System Three Write Enable Head A	DR-10A Interface
15	Video Disk Signal System Three Write Enable Head B	DR-10A Interface
16	Video Disk Signal System Three Playback Enable Head A	DR-10A Interface
17	Video Disk Signal System Three Playback Enable Head B	DR-10A Interface
18	Video Disk Signal System Four Write Enable Head A	DR-10A Interface
19	Video Disk Signal System Four Write Enable Head B	DR-10A Interface
20	Video Disk Signal System Four Write Enable Head C	DR-10A Interface
21	Video Disk Signal System Four Playback Enable Head A	DR-10A Interface
22	Video Disk Signal System Four Playback Enable Head B	DR-10A Interface
23	Video Disk Signal System Four Playback Enable Head C	DR-10A Interface

and High Performance

with a slew rate of 10V per μsec. These models have a low temperature coefficient of 30ppm/°C.

This series features 8, 10, and 12 bit current output units with output settling times of 150 nanoseconds. Both unipolar and bipolar operation are selectable by external pin connection. These converters have a low 15ppm/°C temperature coefficient and are packaged in an extremely compact case.

These models have 8, 10, and 12 bit resolutions with fast voltage output settling times of 2 μsec. Unipolar and bipolar operation are selectable by external pin connection. Temperature coefficient is 20ppm/°C.

This series is identical to the DAC-V series with the addition of an input storage register. Digital input data applied at the storage register inputs does not cause a change at the output until the strobe pulse enables the storage elements.

GENERAL SPECIFICATIONS COMMON TO ALL MODELS IN THE TABLE:

- Operating Temperature Range   0°C to +70°C
- Storage Temperature Range   −55°C to +85°C
- Inputs are DTL/TTL Compatible
- For Bipolar Outputs Offset Binary Coding is Used (2's Complement Coding can be used by inverting the MSB input)
- Voltage Output Models have Output Buffer Amplifiers
- BCD Coded Models Are Unipolar Only
- Specified Accuracies are Obtained Using External Gain and Offset Adjustments
- All Models Use 2 DILS-2 Dual-In-Line Strips for Sockets

For extended temperature range models, see page 55.

LINEARITY	ACCURACY	FS TEMP. COEFFICIENT	REFERENCE VOLTAGE	POWER REQUIREMENT	CASE SIZE	BULLETIN NO.	PRICE (1-9)
±½LSB	±0.2% FS ±½LSB	±100ppm/°C	Internal (5)	+15V DC @ 10mA −15V DC @ 10mA (6)	2"×1"×.375"	DA9BT10405	$14.95 $14.95
±½LSB	±0.2% FS ±½LSB	±50ppm/°C	Internal	+15V DC @ 15mA −15V DC @ 10mA	2"×2"×.375"	DA9BT10405	$29.00 $29.00 $29.00 $29.00
±½LSB	±0.2% FS ±½LSB						$39.00 $39.00
±½LSB	±0.1% FS ±½LSB	±50ppm/°C	Internal	±15V DC @ 20mA	2"×2"×.375"	DA9BT10405	$49.00 $49.00 $49.00 $49.00
±½LSB	±.025% FS ±½LSB						$75.00 $75.00
±½LSB	±.025% FS ±½LSB	±30ppm/°C	Internal	±15V DC @ 25mA	2"×1.5"×.375"	DHBCT10405	$65.00 $79.00 $89.00 $89.00
±½LSB	±.05% FS ±½LSB	±15ppm/°C	Internal	±15V DC @ 20mA	2"×1"×.375"	DAICT10405	$69.00 $79.00 $89.00 $69.00 $89.00
±½LSB	±.01% FS ±½LSB	±20ppm/°C	Internal	±15V DC @ 30mA	2"×2"×.375"	DVRCT10405	$79.00 $99.00 $119.00 $79.00 $119.00
±½LSB	±.01% FS ±½LSB	±20ppm/°C	Internal	±15V DC @ 30mA +5V DC @ 180mA	2"×2"×.375"	DVRCT10405	$99.00 $129.00 $149.00 $109.00 $149.00

(5) Reference is derived from +15V DC power supply. For stable internal reference add suffix "R" to model number and add $2.00 to list price.

(6) −15V DC supply required for "R" version only.

See D/A Converter Specification Guide for detailed information on specifying model numbers for ordering purposes.