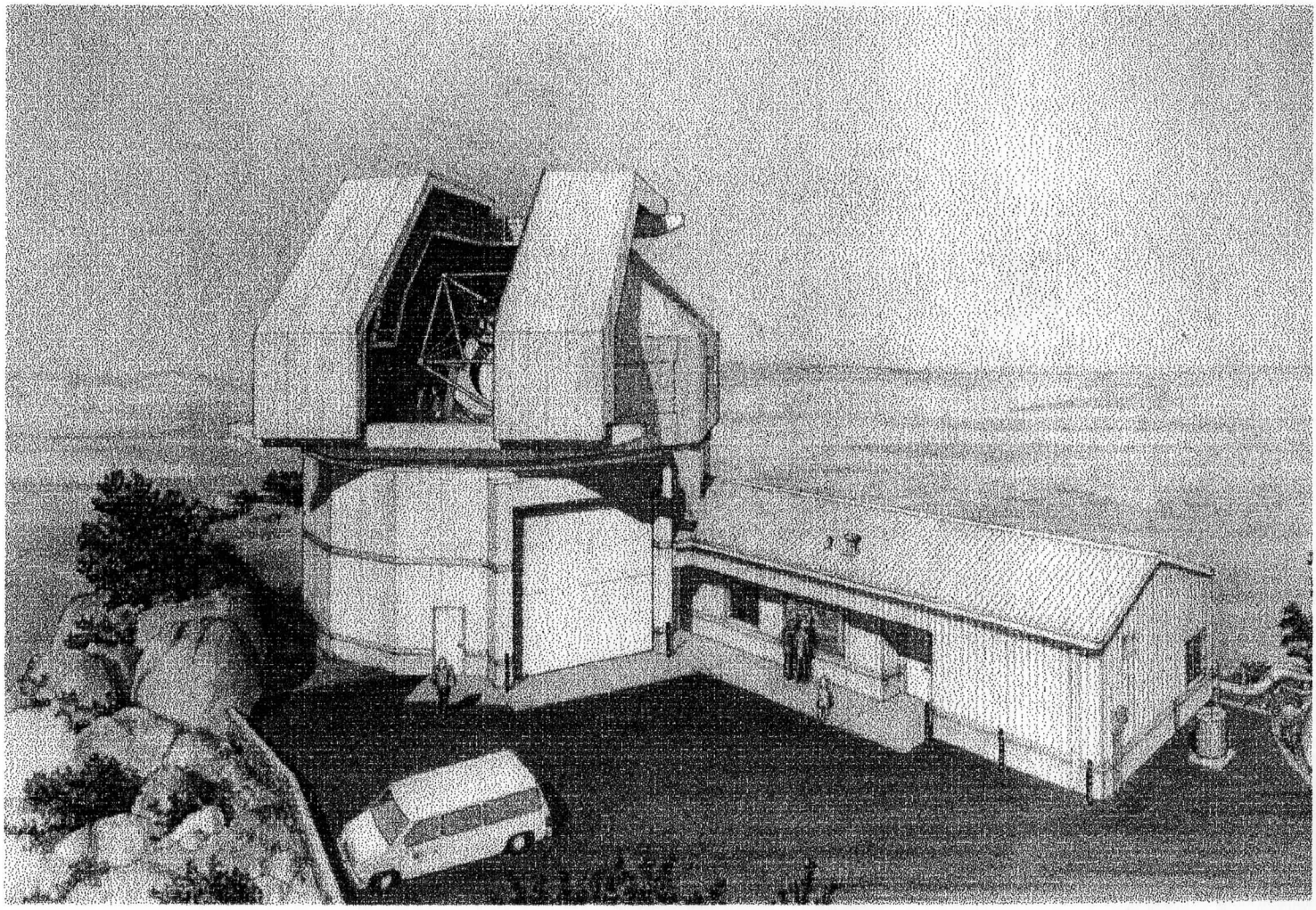
The Schwerdtfeger Li
University of Wisconsin-M
1225 W Dayton Stre
Madison, WI 53706

WIYN Telescope Control System



Maintenance Manual

Table of Contents

WIYN Telescope Control System Maintenance Manual

The Schwerdtfeger Library
University of Wisconsin-Madison
1225 W. Dayton Street
Madison, WI 53706

Preliminary Issue
March 1995

Space Science and Engineering Center
University of Wisconsin - Madison
1225 West Dayton Street
Madison, WI 53706
Telephone: (608) 263-8890
Fax: (608) 263-6738

1 Introduction to the WIYN Telescope Control System
2 Main Drive and NIR Servos
3 Dome Servo Subsystem
4 Encoder Interface Module
5 Optics support structure Control Subsystem (OCS)
6 Instrument Adapter Subsystem
7 Time Code Receiver
8 Serial Opto-isolator
9 Appendices
10 Index

AVERY® READY INDEX™ INDEXING SYSTEM

Copyright© 1995 Space Science and Engineering Center (SSEC)
University of Wisconsin - Madison
All Rights Reserved

Permission is granted to make and distribute verbatim copies of this document, provided the copyright notice and this permission are preserved on all copies.

SSEC makes no warranty of any kind with regard to the software or accompanying documentation, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. SSEC does not indemnify any infringement of copyright, patent, or trademark through use or modification of this software.

Mention of any commercial company or product in this document does not constitute an endorsement by SSEC. Many of the designations used by manufacturers and sellers to distinguish their products are claimed as trademarks. Where those designations appear in this document, and SSEC was aware of the trademark claim, the designations are printed in caps or initial caps.

The information in this document is subject to change without notice. Considerable effort has been expended to make this document accurate and complete, but SSEC cannot assume responsibility for inaccuracies, omissions, manufacturers' claims or their representations.

Preface

The WIYN Telescope Control System controls the WIYN Telescope's azimuth and elevation movements, Nasmyth Instrument port positioning and dome positioning.

This manual is a collection of hardware documentation describing the hardware designed by the University of Wisconsin - Madison's Space Science and Engineering Center. Commercial hardware is documented by the respective manufacturer. Each chapter in this manual provides these levels of description:

- Overview
- Functional Description
- Detailed Circuit Description

This three-tier approach allows all users (technicians, managers, etc.) to progress through this manual to the technical level of detail desired. That is, systems managers may use only the first or second level of detail, while technicians may use all levels of detail.

This documentation complements the documentation provided in the *WIYN Drawings* binder. Every effort has been made to provide accurate, complete and current documentation in this manual. However, if there is a discrepancy between information contained in this manual and information contained in the *WIYN Drawings* binder, use the information in the *WIYN Drawings* binder.

The Schwerdtfeger Library
University of Wisconsin-Madison
1225 W Dayton Street
Madison, WI 53706

Master Table of Contents

Chapter 1. Introduction to the WIYN Telescope Control System 1-1

Telescope Design 1-1
WIYN Observatory Characteristics 1-1
Telescope Control Features 1-2
Introduction Organization 1-2
Hardware Introduction 1-3
Bridge/Router 1-3
Device Controller Assembly 1-3
Instrument Adapter Subsystem 1-7
Optics Support Structure Control Subsystem 1-9
System Status Display 1-10
Primary Mirror Controller 1-10
Software Introduction 1-11
Not available at this time

Chapter 2. Main Drive and NIR Servos 2-1

Overview 2-3
TCC/DCC, Analog I/O and Servo Amplifier 2-3
Servo Motor, Optical Encoder, Index Sensor and Encoder Interface 2-3
Digital I/O 2-4
Control Logic and DC Drive Power Subsystem 2-4
Functional Description 2-5
DC Drive Power Subsystem 2-7
Servo Amplifier Subsystem 2-7
Servo Electronics Subsystem 2-9
Detailed Circuit Description 2-13
DC Drive Power Subsystem 2-17
Batteries 2-17
Battery Chargers 2-17
Battery Charger Monitor 2-18
Power Relays and Control Logic 2-20
Low Voltage Power Supplies 2-23
Servo Amplifier Subsystem 2-24
Servo Amplifier Subassembly 2-24
Current Monitors 2-26
DC Drive Power Test Load 2-26
Servo Electronics Subsystem 2-27
Emergency Stop Switch Interface 2-29
Tachometer Interface 2-30

SES Control Logic 2-34
Emergency Stop Relays 2-41
Power Control 2-42
Internal Power Supplies 2-42
Brake Drivers 2-43
Sensor Switch Interface 2-44
Dome Control Logic 2-44

Chapter 3. Dome Servo Subsystem 3-1
Overview 3-1
Inverters 3-3
TCC/DCC Computer 3-3
Digital I/O Interface Board 3-4
VSIO Board 3-4
Serial Opto-isolator Board 3-4
Maintenance Handpaddle 3-4
Dome Clamps 3-5
Motor Brakes 3-5
Dome Control Logic 3-5
Encoder 3-5
Functional Description 3-7
Dome Control Logic 3-7
Maintenance Handpaddle 3-8
Serial Opto-isolator 3-11
Detailed Circuit Description 3-13
Dome Control Logic 3-17
Inverter AC Power Control 3-21

Chapter 4. Encoder Interface Module 4-1
Overview 4-1
Functional Description 4-3
Position Generator 4-4
Index Sensor Interface 4-5
Time Signal Generator 4-5
VME Bus Interface 4-5
Detailed Circuit Description 4-7
Schematic Conventions 4-7
Logic Conventions 4-7
Position Generator 4-8
Index Sensor Interface 4-11
Time Signal Generator 4-13
VME Bus Interface 4-14

Chapter 5. Optics support structure Control Subsystem (OCS) 5-1
Overview 5-2
Functional Description 5-3
Support Subsystems Background 5-3
STD Bus Boards 5-7

Custom Interfaces 5-9
Detailed Circuit Description 5-27
Thermocoupler Interface 5-24
Secondary Mirror Stepper Motor Interface 5-29
Secondary Mirror Vacuum Support Load Cell Interface 5-29
Secondary Mirror LVDT Interface 5-31
Tertiary Mirror Fold Mechanism Interface 5-32
Tertiary Mirror Vacuum Support Load Cell Interface 5-34
Tertiary Mirror Rotator Interface 5-35
Counterbalance Interface 5-40
Flat Field Lamp Interface 5-42
Vacuum/Air Bag Solenoid Interface 5-43
Mirror Cover Interface 5-44
Circuit Board Configuration 5-46

Chapter 6. Instrument Adapter Subsystem 6-1

To be Completed

Chapter 7. Time Code Receiver 7-1

Introduction 7-1
Electrical Interfaces 7-3
TPRO-VME Module 7-3
IRIG-B Time Code Input 7-3
Time Code Output 7-3
Timing Signal Outputs 7-4
Connector Pin Assignments 7-4
TPRO-VME Setup 7-6
Software Addresses 7-6
External Time Stamping 7-7
FIFO Buffer Configuration Mode 7-7
Rate Output Selection 7-7
TPRO-VME Installation 7-8
Electrical Specifications 7-9

Chapter 8. Serial Opto-isolator 8-1

To be completed

Appendices

Appendix A. Referenced Drawings
Appendix B. Copley Model 220/230 Servo Amplifiers
Appendix C. Interlocks and Recoveries
Appendix D. WIYN Purchased Equipment Manual List

Figures

Figure 1-1. WIYN Telescope Control System Functional Block Diagram 1-4
Figure 2-1. Main Drive or NIR Servo Simplified Block Diagram 2-2
Figure 2-2. Main Drive and NIR Servos Functional Block Diagram 2-6
Figure 2-3. Servo Electronics Subsystem Functional Block Diagram 2-8

Figure 2-4. Main Drive and NIR Servo Control 2-15
Figure 2-5. Emergency Stop Switch Interface Wiring 2-28
Figure 2-6. DC Drive Power Control 2-45
Figure 3-1. Dome Servo Subsystem Functional Block Diagram 3-2
Figure 3-2. Dome Control Logic Functional Block Diagram 3-9
Figure 3-3. Dome Control Logic Detailed Functional Block Diagram 3-15
Figure 4-1.Encoder Interface Module 4-1
Figure 4-2. Encoder Interface Board Functional Block Diagram 4-2
Figure 4-3. Encoder Tracker Arbiter State Diagram 4-10
Figure 5-1. OCS Functional Block Diagram 5-4
Figure 5-2. Secondary Mirror Stepper Motor Interface Block Diagram 5-8
Figure 5-3. Secondary Mirror Vacuum Support Load Cell Interface Block Diagram 5-10
Figure 5-4. Secondary Mirror LVDT Interface Block Diagram 5-12
Figure 5-5. Tertiary Mirror Fold Mechanism Interface Block Diagram 5-14
Figure 5-6. Tertiary Mirror Rotator Interface Block Diagram 5-16
Figure 5-7. Counterbalance Interface Block Diagram 5-18
Figure 5-8. Flat Field Lamp Interface Block Diagram 5-20
Figure 5-9. Vacuum/Air Bag Solenoid Interface Block Diagram 5-22
Figure 5-10. Mirror Cover Interface Block Diagram 5-24
Figure 5-11. OCS Logic Board Conceptual Logic Diagram 5-47

Tables

Table 2-1. Main Drive Relay Failure Symptoms 2-23
Table 2-2. Main Drive and NIR Servo Outputs 2-25
Table 2-3. Azimuth Overspeed Threshold Reference Voltages 2-31
Table 2-4. Elevation Overspeed Threshold Reference Voltages 2-32
Table 2-5. SES Power Supplies 2-43
Table 2-6. Brake Drivers Relays 2-43
Table 3-1. Maintenance Handpaddle Interface Direction Logic 3-17
Table 4-1. Encoder Signal Routing 4-9
Table 4-2. Index Sensor Signal Routing 4-12
Table 4-3. VME Base Address Coding 4-15
Table 4-4. Encoder Interface Module Memory Map 4-16
Table 5-1. OCS STD Bus Boards 5-7
Table 5-2. Stepper Motor Responses 5-29
Table 5-3. Rotator Control Signal Truth Table 5-39
Table 5-4. Mirror Cover Opening Logic Truth Table 5-45
Table 5-5. Mirror Cover Closing Logic Truth Table 5-45
Table 7-1. User I/O Connector (J1) 7-4
Table 7-2. Coaxial Time Code Output Connector (J5) 7-5
Table 7-3. Coaxial Time Code Input Connector (J6) 7-5
Table 7-4. Electrical Specifications 7-9

Chapter 1
Table of Contents

Introduction to the WIYN Telescope Control System 1-1

Telescope Design 1-1
WIYN Obsevatory Characteristics 1-1
Telescope Control Features 1-2
Introduction Organization 1-2

Hardware Introduction 1-3

Bridge/Router 1-3
Device Controller Assembly 1-3
Telescope and Device Control Computer 1-5
Servo Electronics 1-6
Time Code Receiver 1-6
Instrument Adapter Subsystem 1-7
Motion Controller 1-8
IAS Computer 1-8
Image Processor 1-9
Distribution Amplifiers 1-9
Video Router 1-9
Optics Support Structure Control Subsystem 1-9
System Status Display 1-10
Primary Mirror Controller 1-10

Software Introduction 1-11

Not available at this time

Figures

Figure 1-1. WIYN Telescope Control System Functional Block Diagram 1-4

Introduction to the WIYN Telescope Control System

WIYN is a consortium consisting of the University of Wisconsin, Indiana University, Yale University and the National Optical Astronomy Observatories (NOAO). It was formed to develop the WIYN 3.5 m Telescope located at the Kitt Peak National Observatory in Arizona.

Telescope Design

The WIYN Telescope is a Cassegrainian design with tertiary mirrors that can intercept the light beam between the secondary mirror and the Cassegrain focal plane and reflect it through either of the hollow elevation axis support bearings. Attached to each bearing is a Nasmyth Instrument Rotator (NIR) which functions as a standard scientific instrument mount. One NIR port is called the MOS (Multi-Object Spectrograph) NIR; the other port is called the WIYN NIR. Several remotely operated instruments on the WIYN NIR port, such as video cameras, filters and calibration sources etc., aid in automatic telescope tracking, focusing and calibration. The Control System controls the telescope's azimuth, elevation, dome positioning and NIR positioning systems. It also controls the instruments on the WIYN NIR.

WIYN Observatory Characteristics

The WIYN observatory consists of a telescope housing with its east wing, and a local weather station mounted on a tower approximately 100 feet from the telescope. The telescope housing contains a First Level, Second Level and Observing Level. The First Level is the ground floor; the Observing Level is the top floor. The exterior above the Observation Level floor is called the Dome which is rotatable. The east wing contains the Control Room, Instrument Lab, Computer Room, Mechanical Room and Office. In this manual, the approximate physical locations of hardware components in the observatory are described by room names (east wing) or compass direction and floor level (telescope housing).

Telescope Control Features

The primary operator interface to the telescope is the Observation Control Computer (OCC) console located in the Control Room. All telescope subsystems can be controlled and monitored from this console. Except for opening and closing the Shutter Doors, the telescope can also be operated remotely via an Internet connection to the OCC. System Status Display, Video Monitors and Maintenance Hand Paddles furnish additional data and operator interfaces needed for effective systems control.

Introduction Organization

This introduction to the WIYN Telescope Control System consists of a:

- Hardware Introduction
- Software.Introduction

Hardware Introduction

Figure 1-1 on the next page is a functional block diagram of the telescope control system hardware. The main systems in Figure 1-1 are the:

- Bridge/Router
- Device Controller Assembly
- Instrument Adapter Subsystem
- Optics Support Structure Control Subsystem
- System Status Display
- Primary Mirror Controller

Bridge/Router

An Ethernet Local Area Network (LAN) provides the primary communications pathways between telescope subsystems. A local Bridge/Router, connected to four subnets and located in the Computer Room, controls LAN traffic. One subnet supports a connection to the Mountain LAN via the Fiber Optic Adapter located in the Computer Room. Another subnet contains ports for connection to Science Instrument (SI) systems. The remaining subnets connect to the Engineering Data Computer located in the Control Room, and the Telescope Control System.

Device Controller Assembly

Much of the telescope control electronics is located in three electronics enclosures located on the northeast side of the second level. The Device Controller Assembly (DCA) occupies the left two enclosures and consists of these sections:

- Telescope and Device Control Computer
- Servo Electronics
- Time Code Receiver

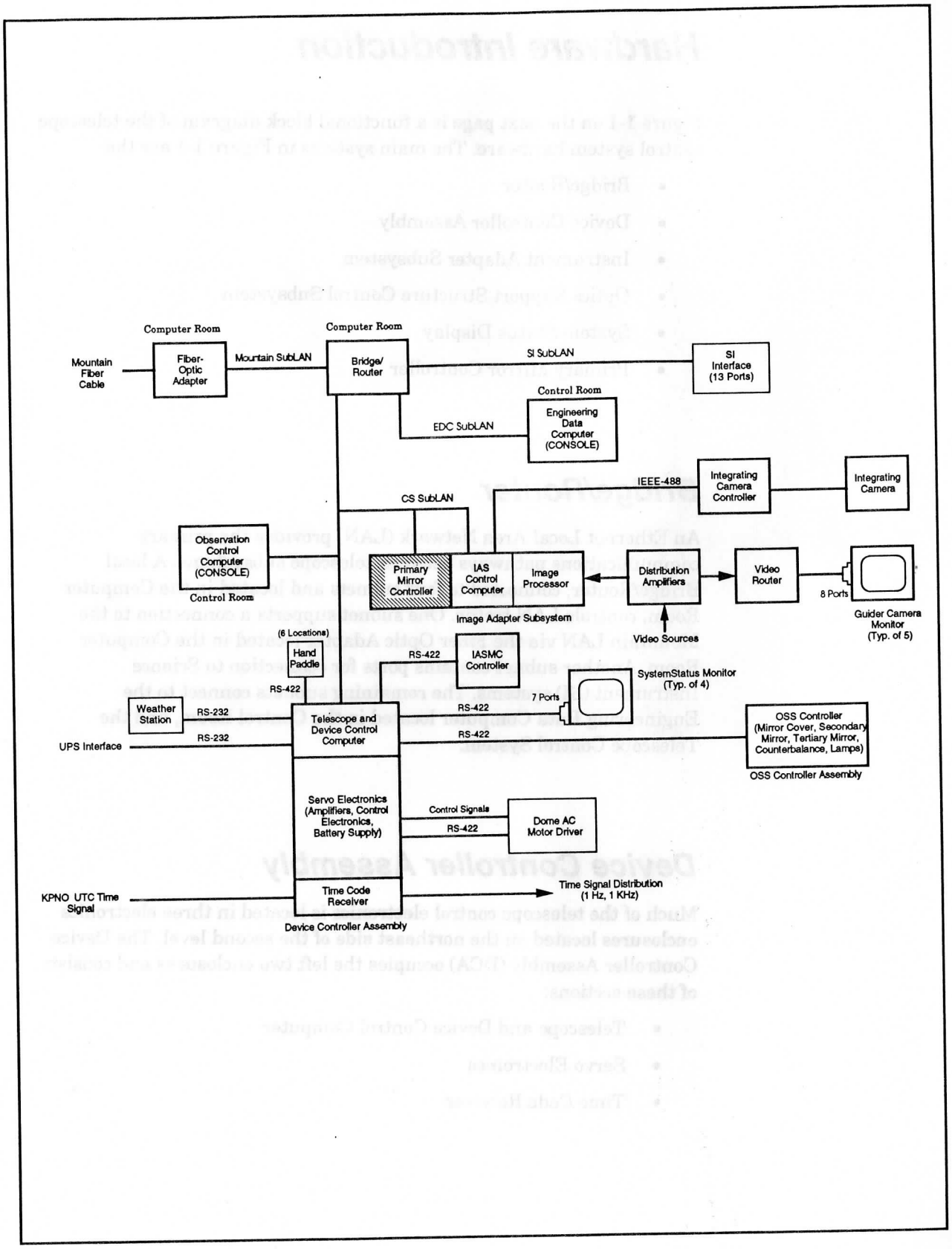


Figure 1-1. WIYN Telescope Control System Functional Block Diagram

Telescope and Device Control Computer

The middle cabinet contains a VME backplane card cage which contains the Telescope and Device Control Computer and its associated support cards. The Telescope and Device Control Computer provides real-time control of five telescope pointing axes, and all communications and processing functions associated with the Device Controller Assembly block in Figure 1-1.

The Telescope and Device Control Computer runs two software processes, the Telescope Control Computer (TCC) process and the Device Control Computer (DCC) process. The TCC process performs these functions:

- receives local weather data from the Weather Station
- receives status from the Uninterruptable Power Supply (UPS) located in the Mechanical Room
- provides system status to four status monitors located throughout the observatory
- provides inputs to the Optical Support Structure Controller Assembly which operates mirror covers, counterbalances, secondary mirror focus, and tertiary mirror positioning, etc.
- communicates with the Telescope Hand Paddles
- provides position and tracking inputs to the DCC process
- links the Device Controller Assembly with other telescope systems via the CS SubLAN
- sends commands to and receives telemetry from the Instrument Adapter Subsystem Motion Controller (IASMC)

The DCC process performs these functions:

- controls the azimuth servo
- controls the elevation servo
- controls the MOS and WIYN Nasmyth Instrument Rotator (NIR) servos
- controls the dome servo
- receives tracking inputs from the TCC process

Hereafter, the TCC and DCC processes and the computer they run on are collectively called the *TCC/DCC*.

Servo Electronics

The Servo Electronics section of the Device Controller Assembly consists of Servo Amplifiers, Control Electronics and a Battery Supply. The Servo Amplifiers and the Battery Supply occupy the left electronics cabinet; the Control Electronics is located in the middle cabinet. The Servo Electronics block produces the drive power for the azimuth, elevation, MOS NIR and WIYN NIR servo motors. The four servo amplifiers that drive these motors are identical and are controlled by the Control Electronics.

The Control Electronics receives position inputs from the DCC process running on the Telescope and Device Control Computer and generates drive signals for the four DC servo amplifiers described above and the dome AC servo. The dome AC servo contains an external intelligent controller called the Dome AC Motor Driver which receives speed and direction input from the Control Electronics. The Dome AC Motor Driver powers two AC servo motors which position the dome.

The four DC servo amplifiers have high source and sink current requirements but relatively low average power requirements. To meet these requirements, the servo amplifiers are powered directly from a 48 VDC lead-acid battery. The battery is maintained in a charged state by a charging system which supplies slightly more power than the combined average power of the four DC servos.

Time Code Receiver

Universal time is indicated by a Time Code Receiver (TCR) located on a common backplane with the Telescope and Device Control Computer. The TCR is referenced to the KPNO (Kitt Peak National Observatory) UTC (Universal Time Code) Time Signal which is a standard modulated IRIG-B (Inter-Range Instrumentation Group - Format B) time code signal. The Time Code Receiver generates 1 Hz and 1 KHz timing signals which are available at several ports throughout the observatory for operators' use.

Instrument Adapter Subsystem (IAS)

The Instrument Adapter Subsystem (IAS) provides many of the common functions (acquisition, focusing, tracking, calibration etc.) required by most observing instruments on the WIYN port.

Several of these functions are accomplished using cameras and image processing electronics which are part of the IAS . For example, telescope tracking is aided by images from the guider camera. If a star is near a desired observation field, it can be selected as a guide star. On the image, the guide star appears at a particular scan line and picture element (pixel). Any change in the guide star's position on successive images indicates telescope tracking errors. Any change in position of the guide star is converted to tracking errors which are sent to the Telescope Device and Control Computer. These tracking errors are used to modify the azimuth and elevation servo drive signals to bring the guide star back to its original position on the guider camera's image. This effectively keeps the observation field stationary.

The focusing camera generates a split image which is used to generate a focus correction signal. This correction signal is used by the Optics Support Structure Controller Subsystem to reposition the secondary mirror.

The Telescope Control System uses the IAS outputs to:

- acquire an observation field
- acquire guide stars on the edge of the observation field
- track the guide stars
- derotate the image (best effort)
- focus the telescope (best effort)
- calibrate the telescope

The IAS consists of optical hardware located on the WIYN NIR and several electronic components located in the right-most electronics enclosure cabinet on the northeast side of Level 2. The optical instruments consist of several video cameras, optical filters, spectral calibration sources and atmospheric dispersion compensators. The electronic components are:

- Motion Controller
- IAS Computer
- Image Processor
- Distribution Amplifiers
- Video Router

The electronics enclosure cabinet contains a VME backplane cardcage, Distribution Amplifiers and Video Router. The VME cardcage contains the Motion Controller, IAS Computer and Image Processor. The Primary Mirror Controller (PMC) is a VME device that is also located in the VME cardcage. However, it is not part of the IAS.

Motion Controller

The Motion Controller controls the positioning of these optical instruments located on the WIYN NIR:

- a dark slide to block light from entering the IAS instruments box
- Atmospheric Dispersion Compensator/Corrector (ADC)
- a slide to remove ADC lenses from the telescope beam
- guide and focus cameras
- color and ND filter wheels, and calibration lamps for each camera
- a deep seeing integrating camera (Princeton) for acquiring faint objects and wavefront sensing
- spectral calibration lamps for each instrument
- a fold mirror on a slide to direct light to the Science Instruments (SI) and the integrating camera

IAS Computer

The IAS Computer:

- provides overall control of the Instrument Adapter Subsystem
- communicates with the remainder of the Control System via the CS SubLAN
- receives commands to implement imaging tasks
- communicates with the Integrating Camera Controller via an IEEE-488 interface
- communicates with the Image Processor via the VME backplane
- sends image outputs from the Integrating Camera Controller to the Image Processor

The integrating camera is primarily an observing instrument, whereas the remaining optical devices on the WIYN port control or calibrate the telescope. The IAS Computer sends commands to and receives telemetry from the Integrating Camera Controller. It also receives video images from this controller which it can pass to the CS SubLAN or Image Processor.

Image Processor

The Image Processor receives seven sources of video images from from the Distribution Amplifiers and an eighth source from the output of the Integrating Camera Controller (via the IAS Computer). It computes centroid information on selected stars from the Acquisition/Guider and Guider/Focus cameras and passes this information to the Telescope Device and Control Computer which uses this information to calculate tracking corrections for the azimuth, elevation and NIR servos.

Distribution Amplifiers

The Distribution Amplifiers block in Figure 1-1 receives video inputs from two IAS cameras (focus and guider) and five other sources, and sends them to the Image Processor and Video Router

Video Router

The Video Router receives the seven video inputs from the Distribution Amplifiers, processed video from the Image Processor and video from a dome camera, and routes selected video to eight data ports throughout the observatory. Five Video Monitors with co-located Control Ports can be plugged into any five of the eight data ports. Any of the nine inputs to the Video Router can be selected for display via the Control Port.

Optics Support Structure Control Subsystem

The Optics Support Structure Control System is housed in an enclosure mounted above the center section of the Optics Support Structure. It provides device control for:

- secondary and tertiary mirror air/vacuum supports
- secondary mirror position actuators
- mirror covers
- tertiary mirror rotator and fold mechanism
- counterbalances
- flat field lamps
- telescope temperature monitors

System Status Display (SSD)

The SSD provides four 14-inch VGA monitors which display a minimum of two display pages. Seven ports are available throughout the observatory for SSD monitor connection.

Primary Mirror Controller

Software Introduction

Chapter 2
Table of Contents

Main Drive and NIR Servos 2-1

Overview 2-3

TCC/DCC, Analog I/O and Servo Amplifier 2-3
Servo Motor, Optical Encoder, Index Sensor and Encoder Interface 2-3
Digital I/O 2-4
Control Logic and DC Drive Power Subsystem 2-4

Functional Description 2-5

DC Drive Power Subsystem 2-7
Servo Amplifier Subsystem 2-7
Servo Electronics Subsystem 2-9
Emergency Stop (E.S.) Switch Interface 2-9
Tachometer Interface 2-9
Sensor Switch Interface 2-10
SES Control Logic 2-10
Emergency Stop Relays 2-12
Power Control 2-12
Internal Power Supplies 2-12
Brake Drivers 2-12

Detailed Circuit Description 2-13

DC Drive Power Subsystem 2-17

Batteries 2-17
Battery Chargers 2-18
Battery Charger Monitor 2-18
Power Relays and Control Logic 2-20
Power Relays 2-20
Control Logic 2-22
Low Voltage Power Supplies 2-23

Servo Amplifier Subsystem 2-24

Servo Amplifier Subassembly 2-24
Current Monitors 2-26

DC Drive Power Test Load 2-26

Servo Electronics Subsystem 2-27

Emergency Stop Switch Interface 2-29
Tachometer Interface 2-30
Input Conditioning Circuits 2-31
Overspeed Threshold Reference Generator 2-31
Comparator Circuits 2-33
Comparator to TTL Interface 2-33
Overspeed Latch 2-33
SES Control Logic 2-34
Emergency Stop Logic 2-34
Interlock Logic 2-35
Drive Power Monitors 2-38
Watchdog Timer Logic 2-38
Power Control Logic 2-39
Brake Control Logic 2-39
Servo Amplifier Enable Logic 2-40
Reset Logic 2-40
Emergency Stop Relays 2-41
Power Control 2-42
Internal Power Supplies 2-42
Brake Drivers 2-43
Sensor Switch Interface 2-44
Dome Control Logic 2-44

Appendices

Appendix A. WIYN Drawings (Separate)
Appendix B. Copley Model 220/230 Servo Amplifiers
Appendix C. Interlocks and Recoveries

Figures

Figure 2-1. Main Drive or NIR Servo Simplified Block Diagram 2-2
Figure 2-2. Main Drive and NIR Servo Functional Block Diagram 2-6
Figure 2-3. Servo Electronics Subsystem Functional Block Diagram 2-8
Figure 2-4. Main Drive and NIR Servo Control 2-15
Figure 2-5. Emergency Stop Switch Interface Wiring 2-28
Figure 2-6. DC Drive Power Control 2-45

Tables

Table 2-1. Main Drive Relay Failure Symptoms 2-23
Table 2-2. Main Drive and NIR Servo Outputs 2-25
Table 2-3. Azimuth Overspeed Threshold Reference Voltages 2-31
Table 2-4. Elevation Overspeed Threshold Reference Voltages 2-32
Table 2-5. SES Power Supplies 2-43
Table 2-6. Brake Drivers Relays 2-43

Main Drive and NIR Servos

The Main Drive and NIR Servos consist of these four servos:

- telescope azimuth positioning
- telescope elevation positioning
- WIYN Nasmyth Instrument Rotator port positioning
- MOS Nasmyth Instrument Rotator port positioning

This chapter documents the following subsystems which control the servo positioning systems listed above:

- DC Drive Power Subsystem
- Servo Amplifier Subsystem
- Servo Electronics Subsystem (SES)

This chapter describes the Main Drive and NIR Servos at the functional level, and SSEC designs at the functional and detailed circuit description levels. Detailed descriptions of remaining components are provided by their respective manufacturers.

The SES and DC Drive Power Subsystem are designed and built by UW-Madison's Space Science and Engineering System (SSEC). The servo amplifiers, manufactured by Copley Controls Corporation, are components of the Servo Amplifier Subsystem which is also designed and built by SSEC.

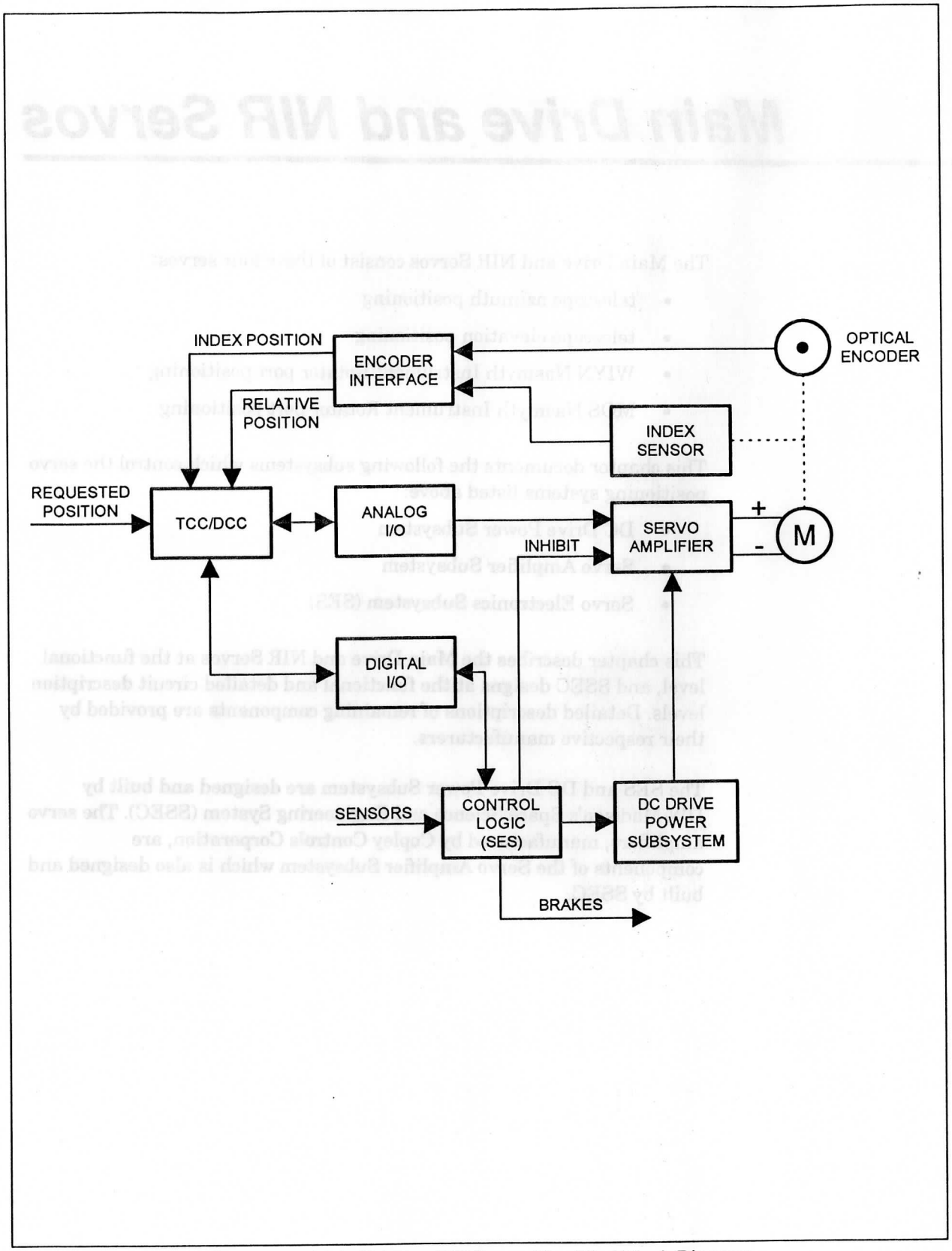


Figure 2-1. Main Drive or NIR Servo Simplified Block Diagram

Overview

Figure 2-1 on the adjacent page is a simplified block diagram of a Main Drive servo or NIR servo. These servos are similar and each consists of these functional blocks:

- Telescope Control Computer/Device Control Computer (TCC/DCC)
- Analog I/O
- Servo Amplifiers
- Servo Motors
- Optical Encoders
- Index Sensor
- Encoder Interface
- Digital I/O
- Control Logic
- DC Drive Power Subsystem

TCC/DCC, Analog I/O and Servo Amplifier

The TCC/DCC computes a digital demand value which is based on the difference between the requested position and current position. This demand value is converted to an analog voltage by the Analog I/O block and passed to the Servo Amplifier. The Servo Amplifier, operating in the current mode, converts the input drive voltage to an output motor current. The TCC/DCC and Analog I/O are commercial VME bus cards. Refer to the respective manufacturer's documentation for details on these cards. The Servo Amplifiers are also commercial devices which are documented by their manufacturer.

Servo Motor, Optical Encoder, Index Sensor and Encoder Interface

The motor is coupled to the device being rotated, an Optical Encoder and Index Sensor. The Optical Encoder generates a precise number of pulses per arc-second of load rotation. The Encoder Interface counts these pulses to determine Relative Position. During initialization, each servo is rotated until an index pulse is received which latches the contents of the pulse counter in the Encoder Interface. The latched count is called the Index Position Count. The TCC/DCC determines absolute position by comparing the Relative Position Count to the Index Position count.

The Servo Motor, Optical Encoder and Index Sensor are commercial components which are documented by their respective manufacturers; the Encoder Interface is a custom design which is described in Chapter 4.

Digital I/O

The Digital I/O is a commercial VME bus card that interfaces the TCC/DCC to the Control Logic. It contains serveral I/O input ports which provide the TCC/DCC with status output bits from the Control Logic. The Digital I/O contains several output ports which drive control inputs to the Control Logic.

Control Logic and DC Drive Power Subsystem

A consideration in the design of the Main Drive and NIR servos was minimizing custom electronics. However, because of a large telescope's unique safety considerations and drive power requirements, the Control Logic and DC Drive Power Subsystem blocks in Figure 2-1 are custom designs.

The Control Logic block shuts down the servos if a dangerous condition is detected by its external sensors. It does this by removing the 48 VDC power from the Servo Amplifiers and by removing AC power from the brake control solenoids (applies the brakes). Because operators and technicians are often in close proximity to moving telescope components, many safety and interlock features are built into the Control Logic. If an interlock condition exists, such as trying to elevate the telescope while the Elevation Latch Pin is engaged, the Control Logic outputs an inhibit signal to the respective Servo Amplifier (Elevation Servo Amplifier in this example) until the interlock condition is cleared.

The Control Logic block in Figure 2-1 is called the Servo Electronics Subsystem (SES). It provides the safety interlocks and sensor interfaces to minimize the possibility of injury to personnel and damage to telescope components. The SES receives control inputs from the TCC/DCC and sensor inputs from numerous servo-related devices in the observatory. The SES controls power to the servo amplifiers and application of brakes and clamps.

The servo amplifiers require a power supply capable of sourcing large currents for acceleration and sinking large currents for regenerative braking during deceleration. However, these servos require small currents at idle and constant speed. An innovative custom servo power supply design, based on lead-acid batteries and a recharging system, accommodates the servo amplifier power requirements while reducing power supply size and cost. It also provides servo power during AC power failures. The DC Drive Power Subsystem provides 48 VDC at currents of up to 50 amps for the servo amplifiers.

Functional Description

Figure 2-2 on the next page is a Functional Block Diagram of the Main Drive and NIR Servos. Refer to it during this functional description.

The following components in the Main Drive and NIR Servos are described:

- DC Drive Power Subsystem
- Servo Amplifier Subsystem
- Servo Electronics Subsystem (SES)

These subsystems are located in the left and middle equipment racks on the northeast side of the Second Level. The DC Drive Power and Servo Amplifier Subsystems are located in the left rack; the Servo Electronics Subsystem is located in the center rack along with a VME crate containing the TCC/DCC and its associated interface boards (see Figure 2-1).

The Dome Servo Subsystem, which consists of Dome Inverters, Dome Drive Motors, brakes, clamps, the Dome Handpaddle and Dome Control Logic (part of the SES), is described in Chapter 3, the Dome Control Logic chapter.

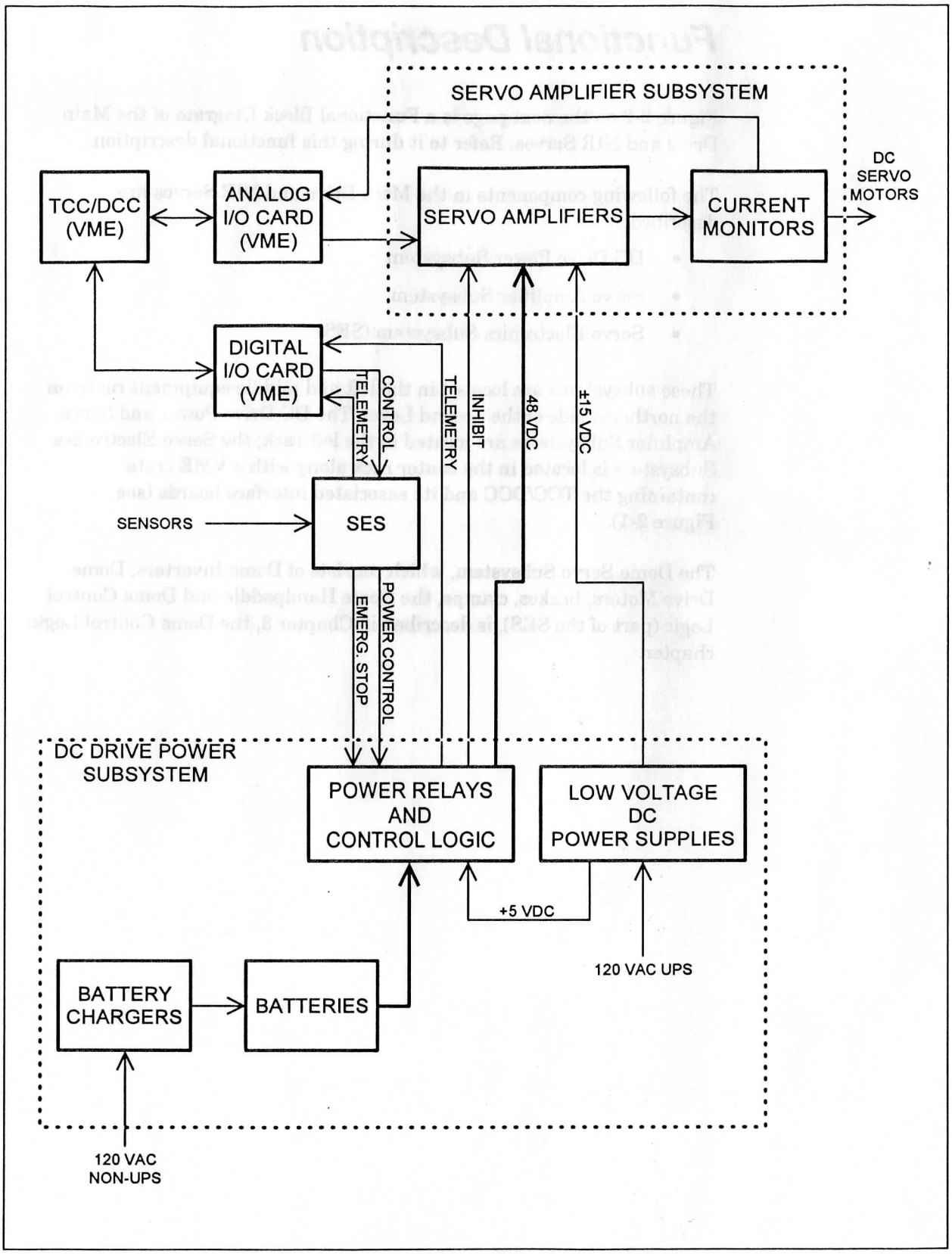


Figure 2-2. Main Drive and NIR Servos Functional Block Diagram

DC Drive Power Subsystem

The DC Drive Power Subsystem provides 48 VDC power for the servo amplifiers. Four sealed, lead-acid, 12-volt batteries are series connected to provide the 48 VDC servo amplifier power. Connected across each battery is a separate 12-volt Battery Charger that keeps the batteries fully charged when 120 VAC power is present. The chargers provide enough power to recharge the batteries after a power failure and supply the Main Drive and NIR Servo Amplifiers. Because the peak currents required during acceleration are very high, the batteries momentarily supply the current when the demand exceeds charger capability.

A Battery Charger Monitor detects failed battery chargers by comparing each battery's voltage to a precision reference. Upon detection of a failed charger, the Battery Charger Monitor passes a telemetry signal to the TCC/DCC indicating a failed charger. In addition, the Battery Charger Monitor also detects failed batteries. If servo operation continues after a charger fails, the respective battery eventually becomes discharged. Upon detection of the dead battery, the Battery Charger Monitor disables the DC Drive Power Subsystem, preventing battery damage.

The 48 VDC power is applied to the Main Drive and NIR Servo Amplifiers via AC power relays in the Power Relays and Control Logic block which are controlled by the Power Control block in the SES.

Servo Amplifier Subsystem

The Servo Amplifiers control the current to the Azimuth, Elevation and NIR servo motors in response to analog voltage inputs from the Analog I/O board. Each Main Drive and NIR servo motor is powered by one or more Copley Controls Corporation model 220 servo amplifiers. The model 220 is available in two versions, a master unit (model 220H) and a slave unit (model 220SH). Each master and slave amplifier can provide up to 12 amps of output current. When more output current is required than a master unit can provide, model 220SH slave units can be added in parallel with and controlled by the master unit.

Because of the telescope's mass, dual azimuth and elevation servo motors are required to achieve specified acceleration and velocity rates. Furthermore, each azimuth motor requires more current than a single servo amplifier can deliver. Azimuth motor current requirements are met by adding a slave servo amplifier to each azimuth master amplifier. Thus, the six servo motors (two azimuth, two elevation, a WIYN NIR and a MOS NIR) are powered by six master servo amplifiers and two slaves.

Current Monitors, designed and built by SSEC, provide Azimuth and Elevation motor current telemetry to the TCC/DCC.

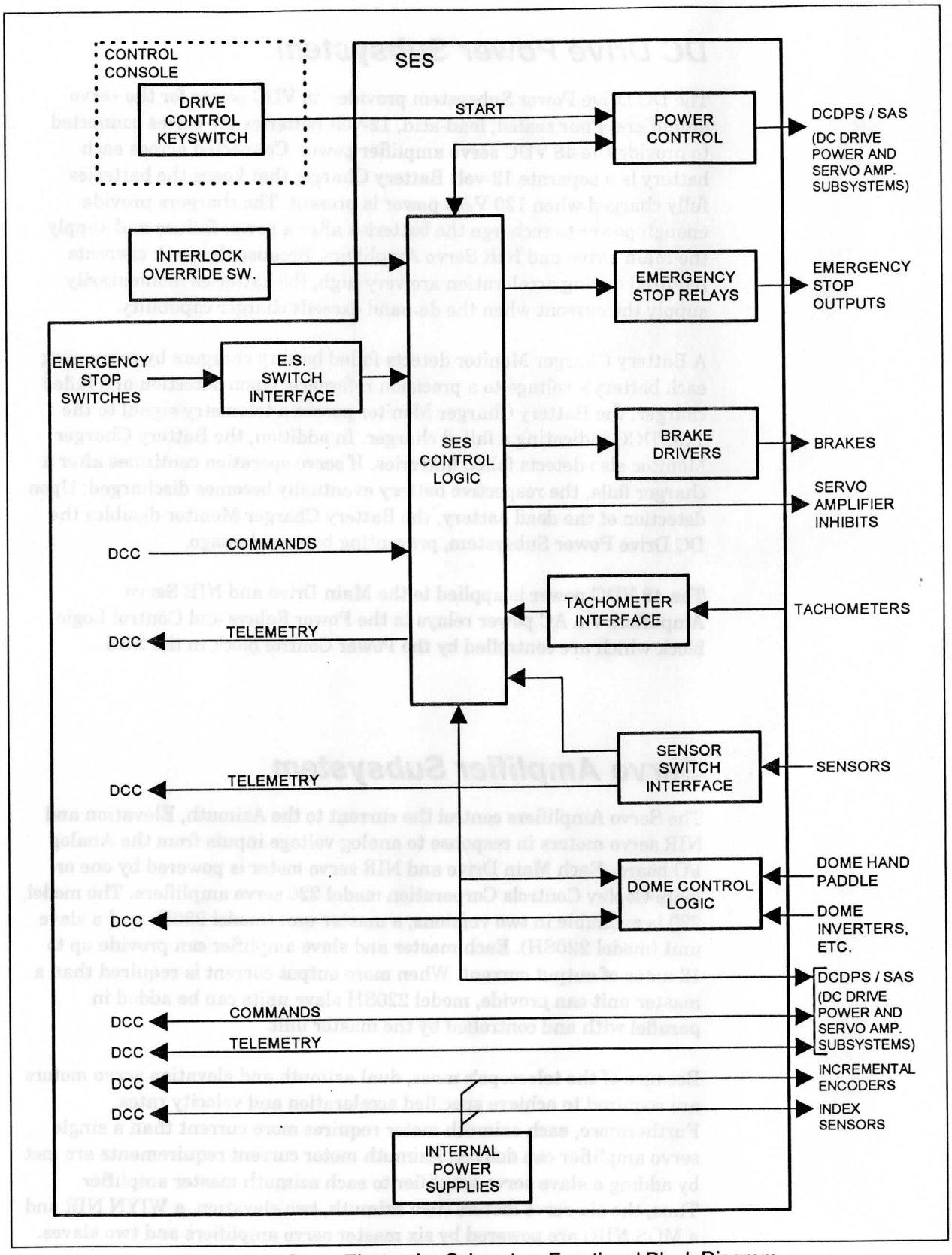


Figure 2-3. Servo Electronics Subsystem Functional Block Diagram

Servo Electronics Subsystem

The Servo Electronics Subsystem (SES block in Figure 2-2) is expanded and shown in Figure 2-3 on the adjacent page. It consists of these functional blocks:

- Emergency Stop (E.S.) Switch Interface
- Tachometer Interface
- Sensor Switch Interface
- SES Control Logic
- Emergency Stop Relays
- Power Control
- Internal Power Supplies
- Brake Drivers

Emergency Stop (E.S.) Switch Interface

Pressing any of the red-labeled EMERGENCY STOP switches distributed throughout the observatory removes the 48 VDC power from all Main Drive and NIR Servos and applies all brakes.

The Emergency Stop Switch Interface couples the Emergency Stop switches to the SES Control Logic. It indicates Emergency Stop if an Emergency Stop button is pressed or there is a short or open circuit in the Emergency Stop Switch wiring. Circuit wiring fault detection is a safety feature that prevents servo operation if an electrical fault occurs in the Emergency Stop Switch wiring.

Tachometer Interface

Tachometers on the telescope sense azimuth and elevation velocities. A failure in the Azimuth or Elevation control logic or Servo Amplifiers can cause a runaway. If this occurs, the respective tachometer's output exceeds a threshold value which is detected by the Tachometer Interface block. The Tachometer Interface latches the runaway status which is an input to the SES Control Logic. The SES Control Logic removes power from the Azimuth and Elevation Servo Amplifiers, and engages the brakes. Power remains off until the status latches in the Tachometer Interface are reset via the Drive Control Keyswitch.

Sensor Switch Interface

The Sensor Switch Interface provides noise immunity, isolation and transient protection for 47 observatory sensor switches. Some interface outputs are used only as telemetry inputs to the TCC/DCC some are used only by the SES Control Logic and some are used by both. Sensor switch inputs to this block are:

- Azimuth Clockwise and Counterclockwise Hard and Soft Limit switches
- Elevation Up and Down Hard and Soft Limit switches
- Elevation 20°, 30° and 85° Tilt switches
- Azimuth, Elevation and NIR Brake Pressure switches
- Elevation Latch Pin switch
- Tape switch
- Lift Platform switch
- Control Panel ON and Start switches
- Main Drive Lockout switch
- Dome Control MAINT and COMP switch (refer to Chapter 3, the Dome Control Logic chapter)
- NIR Clockwise and Counterclockwise Limit switches
- NIR Center switches
- Dome Inverter Fault switches (refer to Chapter 3, the Dome Control Logic chapter)
- NIR Latch Pin switches
- Dome Maintenance Handpaddle Speed, Clamp, Clockwise and Counterclockwise switches (refer to Chapter 3, the Dome Control Logic chapter)
- Dome Motor Low Velocity Limit switches
- Dome Clamp Pressure switch (refer to Chapter 3, the Dome Control Logic chapter)
- Interlock Override switch

SES Control Logic

The SES Control Logic consists of:

- Emergency Stop Logic
- Interlock Logic
- Drive Power Monitors
- Watchdog Timer Logic
- Power Control Logic

- Brake Control Logic
- Servo Amplifier Enable Logic
- Power Reset Logic

Emergency Stop Logic

The Emergency Stop Logic combines the outputs of the E.S. Switch Interface, the Emergency Stop Command from the TCC/DCC, and the internal watchdog timer to form the Emergency Stop Relay drive. The watchdog timer inhibits the servo drives if it fails to be clocked by the TCC/DCC.

Interlock Logic

The Interlock Logic provides inputs to the Brake Control and Servo Amplifier Enable Logic sections (described below). It combines the latched overspeed status from the Tachometer Interface with the telescope hard limit switches, Tape switch and Lift Platform switch outputs from the Sensor Switch Interface to form the interlock inhibit signals.

Drive Power Monitors

The Drive Power Monitors section develops TCC/DCC telemetry signals from the 48 VDC power inputs to the Main Drive and NIR Servo Amplifiers.

Watchdog Timer Logic

The Watchdog Timer Logic receives a toggle input from the TCC/DCC. If it fails to receive this input, the TCC/DCC is not working properly. If this happens, the Watchdog Timer removes power from the servo amplifiers, and applies the brakes.

Power Control Logic

The Power Control Logic gates main drive and NIR power control signals from the TCC/DCC with the interlock inhibit signals to produce control outputs to the DC Drive Power Subsystem. An active emergency inhibit overrides the respective TCC/DCC input. In the DC Drive Power Subsystem, these signals control relays in the high side of the AC power relays which complete the DC path between the DC Drive Power Subsystem and the Servo Amplifier Subsystem.

Brake Control Logic

The Brake Control Logic combines brake release signals from the TCC/DCC with the inhibit signals to form the Brake Drivers inputs. An active interlock inhibit overrides the TCC/DCC's brake release signal and applies the associated brake.

Servo Amplifier Enable Logic

The Servo Amplifier Enable Logic combines servo enable signals from the TCC/DCC with the interlock inhibit signals to form the servo amplifier inhibit inputs. An active interlock inhibit overrides the TCC/DCC's enable signal, inhibiting the associated servo amplifier.

Power Reset Logic

The Power Reset Logic resets several SES Control Logic latches and initializes the Dome Control Logic when AC power is initially applied to the SES (refer to Chapter 3, the Dome Control Logic chapter).

Emergency Stop Relays

Refer to Figures 2-2 and 2-3. For safety purposes, there are multiple ways of turning off the Main Drive and NIR Servo Amplifiers. The Emergency Stop Relays remove the 48 VDC drive power from these amplifiers and applies the brakes in response to the Emergency Stop switches. This safety circuitry involves only switches and relays. Emergency Stop operation is independent of the TCC/DCC. Redundant SES circuitry is provided.

Power Control

Refer to Figures 2-2 and 2-3. As another safety precaution, the Power Control circuits remove the 48 VDC drive power from the Main Drive and NIR Servo Amplifiers in response to the Interlock Logic and Emergency Stop Logic.

The Drive Control Keyswitch located on the Control Console must be turned to the momentary START position to activate the Power Control circuits which apply 48 VDC power to the servo amplifiers.

Internal Power Supplies

The SES chassis houses eight low voltage power supplies designated PS1 through PS8. They provide DC power for servo-related devices and logic.

Brake Drivers

Driven by the Brake Control Logic, the Brake Drivers apply 120 VAC to solenoid valves in the air supply lines to the brake mechanisms.

Detailed Circuit Description

This Detailed Circuit Description discusses the logic of each block shown in Figures 2-2 and 2-3 on pages 2-6 and 2-8, respectively.

Safety hazards are also noted in this description. Safety features and hardware interlocks are designed into the Main Drive and NIR Servos to protect personnel in the immediate vicinity of moving telescope components and the telescope itself. During preventive or corrective maintenance, do not operate the telescope with safety logic or safety related devices defeated. If telescope servo operation is required during preventive or corrective maintenance, use extreme caution when moving any part of the telescope. For example, the telescope can be damaged if it is slewed while hard and soft limit switches are defeated.

Much of the Main Drive and NIR Servo circuitry is mounted on two PWBs (Printed Wiring Boards) and two wire wrap boards. Regardless of the board type, integrated circuits are referenced by U designators. Discrete resistors, capacitors and transistors are referenced by R, C and Q designators, respectively. Board mounted Main Drive and NIR Servo component locations are shown in these drawings:

- SES Sensor Switch Interface PWB (4421-0098)
- SES Wire Wrap Board Layout (4421-0101)
- DC Drive Power Wire Wrap Board (4421-0045)
- Current Monitor Printed Wiring Board (4421-0022)

References to schematic circuit symbols of a multiple section device usually use the symbol ID followed by a hyphen and letter designator, e.g. section A of a 26LS33 line receiver IC located at U6 is called U6-A. If a letter designator is not used, pin numbers are referenced. Single function ICs are referenced by the circuit symbol alone.

Decimal points (.) in resistor and capacitor values are replaced by K and u, respectively. This prevents misinterpretation of a component's value due to overlooking a decimal point. For example, a 4990 ohm resistor is shown as 4K99 (4.99K ohms); a 0.1μ capacitor is shown as u1.

Signal names are in uppercase letters and numbers, e.g. NPM. A logic signal name ending with an overscore or trailing slash represents an active low signal, e.g. $\overline{\text{WNE}}$ or WNE/. In this discussion, all logic states are described as high and low. An *asserted* logic signal is a signal in its active state.

Figure 2-4 on page 2-15 combines the DC Drive Power, Servo Electronics and Servo Amplifier Subsystems into a single schematic. It shows most logic as functional blocks which are clearly labeled on the subsystem or logic board schematic. It also shows signal and power interconnections between the subsystems. Thus, Figure 2-4 should be very useful for rapidly isolating servo problems to a specific subsystem or even to the component level. Because Figure 2-4 is primarily power and control oriented, most telemetry signal paths are not shown.

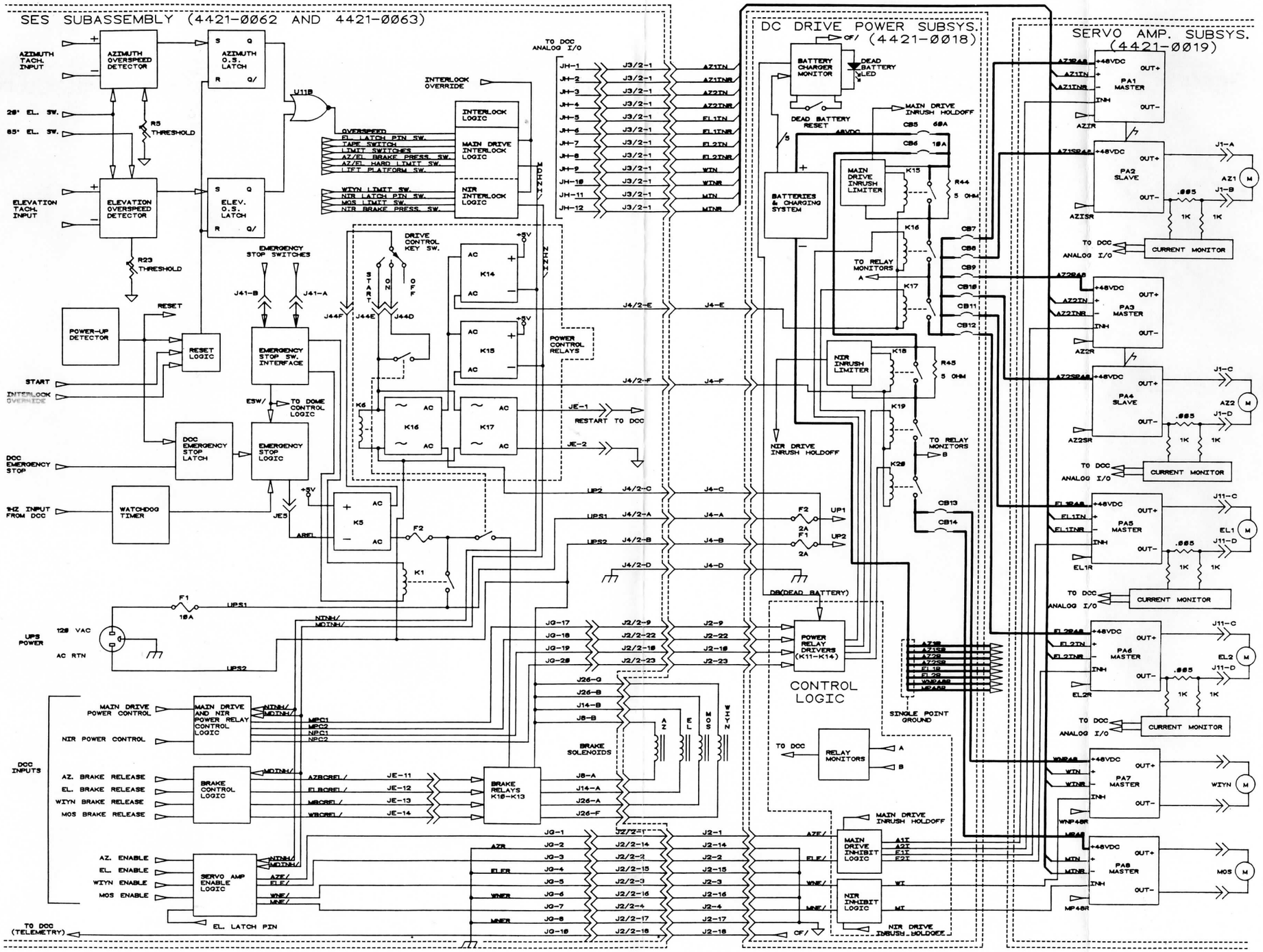


Figure 2-4. Main Drive and NIR Servo Control

DC Drive Power Subsystem

Refer to drawing 4421-0018, the DC Drive Power Subsystem schematic, and drawing 442-0033, the Battery Charger schematic in the *WIYN Drawings* binder (see *Appendix A*). In addition, the following documents provide location information:

- DC Drive Power Rack Detail (4421-0029)
- DC Drive Power Subsystem Connector Panel (4421-0040)
- DC Drive Power Wire Wrap Board (4421-0045)
- DC Drive Power Test Load Subassembly (4421- 0047)
- DC Drive Power Subsystem Relay Subassembly (4421-0024)

The DC Drive Power Subsystem consists of these sections:

- Batteries
- Battery Chargers
- Battery Charger Monitor
- Battery Charger Monitor
- Power Relays and Control Logic
- Low Voltage Power Supplies

Batteries

Refer to sheet 1 of schematic 4421-0018 in the *WIYN Drawings* binder (see *Appendix A*). Four sealed lead-acid 12-volt batteries located in the bottom of the left equipment cabinet are series connected to provide a nominal voltage of 48 volts. Total battery voltage ranges from about 44 volts at 50 amps to about 56 volts at no load. A low voltage sensor detects battery voltages below 40 volts.

Battery life is expected to be about five years and they should be replaced regularly. Replacement batteries must be the same Gates G12V50W15H type or equivalent. These batteries have high peak current capacity and also accept large charging and regenerative braking currents. Not all UPS-type batteries share these properties.

Battery Chargers

Refer to sheet 1 of schematics 4421-0033 and 4421-0036 in the *WIYN Drawings* binder (see *Appendix A*). Four modified XENOTRONICS 12-volt battery chargers keep the batteries fully charged when 120 VAC power is available. The battery chargers are temperature compensated and deliver higher charge voltage during low temperatures. Diagram 4421-0036 is a schematic of the unmodified charger; 4421-0033 is a schematic of the modified chargers. If a battery charger is replaced, verify that the modification steps in *Appendix B* are performed or perform those steps prior to installation.

Battery Charger Monitor

The Battery Charger Monitor consists of four floating dual detectors whose outputs are optically isolated and NORed together to form CF/ (Charger Failure) and DB (Dead Battery).

CF/ is a telemetry signal which warns the operator of a possible charger failure. CF/ may go active low momentarily during high servo amplifier current loads caused by rapid accelerations of the telescope in azimuth or elevation. Also, high wind loads on the telescope can sometimes cause CF/ to go low momentarily even during low speed tracking conditions. Momentary CF/ alarms under these conditions are normal and automatically clear when the total current load returns to a level which can be supplied by the Battery Chargers. However, if CF/ goes low and stays low, one or more battery chargers failed.

If a Battery Charger fails, the respective battery continuously discharges during Main Drive and NIR servo operation. If the nominal 12-volt battery discharges to 6.00 volts, DB goes high and shuts off the main drive power to the servo amplifiers.

Refer to drawing 4421-0143; the Battery Charger Monitor schematic and drawing 4421-0141, the Battery Charger Monitor subassembly. Each battery and its associated charger are monitored by a dual voltage detector circuit which drives the inputs of a dual opto-isolator. Since each detector circuit is identical, only the detector for battery B4 and its charger is described. The detectors for B1 through B3 are identical. The B4 to BRTN potential is nominally about 13.75 volts DC. this voltage is impressed across the dual detector consisting of:

- comparator A7
- diodes D7 and D8
- resistors R23 through 28
- the input side of dual opto-isolator A8

Diode D7 prevents reverse potentials across the remainder of the detection circuits which may result if a battery is severely discharged as a result of a failed charger.

Resistor R22 and zener diode D8 provide a zener regulated 6.8 VDC input to A7.

A7 is a dual comparator. Its noninverting inputs are driven by taps on a voltage divider consisting of R23 through R26. A7's inverting inputs (not shown in drawing 4421-0143) are driven by a 1.25-volt band-gap reference. If the noninverting input is more positive than this reference, the respective inverter's output is low. That is, if the voltage at B4 drops below 13.0 volts, A7's pin 14 goes high; if the voltage at B4 drops below 6.00 volts, A7's pin 13 goes high. R26 is selected to trim the voltage trip points to these values. R5, R12 and R19 are selected to achieve the same trip points for the remaining comparators. That is, the selected resistor in each voltage divider compensates for resistor tolerance in the remaining divider resistors. The comparator with the pin 2 input is the dead battery detector; the comparator with the pin 3 input is the charger fail detector. Since the input to each comparator is normally higher than the band-gap reference, both comparators normally have low outputs.

The comparators drive the cathodes of the opto-isolator LEDs. The output side of each opto-isolator consists of a photo-transistor and collector resistor connected between signal ground and +5 volts from PS1. Since both cathodes are normally low, both transistors are normally on and their collectors are normally low.

The pin 6 output of each opto-isolator is the Charger Fail signal for its respective charger and battery. These normally low outputs are NORed together by A9 (input pins 9, 10, 11 and 12) to produce CF/.

The pin 8 output of each opto-isolator is the Dead Battery signal for its respective charger and battery. These normally low outputs are NORed together by A9 (input pins 2, 3, 4 and 5) to drive the set input of a set/reset latch consisting of A10. A10 NAND gates whose output pins are 3 and 11 are wired as a set/reset latch. When power is initially applied, the latch can come up in either state. This latch is reset via the Dead Battery Reset switch located on the Servo Amplifier Subassembly Connector Panel. The NOR gate whose output is pin 1 has normally low inputs. If a battery's voltage falls below 6 VDC, dead battery's respective input to the NOR gate goes high, driving the NOR gate's output low. This sets the latch, causing the NAND gate whose outpout is pin 11 to go high. The NAND gates whose outputs are pins 6 and 8 are wired in parallel and function as an inverter. They drive the cathode of the Dead Battery LED with inverted DB. Since a dead battery sets the latch, the LED's cathode is pulled low if a dead battery is detected. This causes the Dead Battery Warning LED to be illuminated.

Power Relays and Control Logic

Refer to Figure 2-4 and drawing 4421-0018. The power relays and control logic are shown on sheets 1 and 2, respectively, of drawing 4421-0018 in the *WIYN Drawings* binder (see *Appendix A*).

Power Relays

Main Drive power relays K16 and K17 control DC power to the Azimuth and Elevation Servo Amplifiers; NIR power relays K19 and K20 control DC power to the MOS and WIYN NIR Servo Amplifiers. Relay K15 and resistor R44, and relay K18 and resistor R45 limit the inrush current when power is initially applied. The Main Drive power relay control is described; the NIR power relay control is identical.

Relays K16 and K17

K16 and K17 must energize to apply power to the Main Drive Servo Amplifiers. Two relays are used for redundancy. If one relay fails to open when de-energized, the other relay will remove power from the servo amplifiers. The Main Drive Relay Monitor described on page 2-22 detects failures in either relay and passes this telemetry information to the TCC/DCC.

Refer to Figure 2-4. Both sides of the power relay coils are controlled. The common connection between relays K15, K16 and K17 goes to UPS AC RTN (AC return side of the UPS 120 VAC supply) via:

- connector J4 pin E on the DC Drive Power Subsystem Connector Panel
- to connector J4/2 pin E on the SES Connector Panel
- through the AC terminals of SES solid-state relay K14
- through the AC terminals of SES solid-state relay K16
- to connector J4/2 pin C on the SES Connector Panel
- back to the DC Drive Power Subsystem via connector J4 pin C
- through fuse F1
- to DC Drive Power Subsystem connector J4 pin B
- to connector J4/2 pin B on the SES to AC RTN

This routing is a safety feature to ensure that no servo subassembly or subsystem can be removed without removing power from the servo amplifiers.

SES relays K14, K15 and K16 are controlled by the hardware interlock circuits and Emergency Stop Logic. If SES relay K14 or K15 is de-energized, the Main Drive power relays or the NIR power relays in the DC Drive Power Subsystem de-energize, respectively. If SES relay K16 is de-energized, all power relays in the DC Drive Power Subsystem de-energize.

The Power Relay Drivers section of the Control Logic (described on page 2-22) drives the high side of the Main Drive and NIR power relays. K21 and K22 discharge the Servo Amplifier Subsystem filter capacitors through R46 and R47, respectively, when DC power is turned off. R46 discharges the Main Drive filter capacitors; R47 discharges the NIR filter capacitors.

Inrush Relay K15

Inrush relay K15 is open when K16 and K17 initially close. The servo amplifier filter capacitors begin charging through resistor R44 which limits the peak charge current to about 10 amps. The inrush control circuitry inhibits the servo amplifiers while K15 is de-energized. This ensures very little current flow through R44 after the capacitors charge.

Refer to the MD Inrush Limiter circuitry on sheet 2 of drawing 4421-0018 in the *WIYN Drawings* binder (see *Appendix A*). Assuming a battery voltage of 48 VDC, the voltage at the junction of R3 and R4 is a constant 2.23 volts. The top of R6 connects to the servo amplifier side of R44 through fuse F4. When relays K16 and K17 initially close, the voltage at F4 rises exponentially from 0 VDC toward 48 VDC while the charge current through R44 decays from about 10 amps toward 0 amps. R6 and R7 form a voltage divider such that the voltage at pin 4 of comparator A1 is less than A1's pin 5 until the voltage at F4 exceeds 43.7 VDC. Until this happens, A1's pin 2 is high which causes a low at the output of inverter A5-A.

When the voltage at F4 exceeds 43.7 volts, A1's pin 2 goes low, which enables solid state relay K1. When K1 energizes, it applies UP1 (high side of the 120 VAC UPS power) to K15. Assuming the other side of K15's coil is at AC Return (see Relays K16 and K17 above), K15 energizes and shorts R44, applying full battery voltage to the Main Drive and NIR Servo Amplifiers. The remaining MD Inrush Limiter Logic prevents these amplifiers from being enabled for an additional 0.1 seconds.

When the voltage at F4 exceeds 43.7 volts, A1's pin 2 goes low and A5-A's output goes high. Because of the charge on C17, this causes a short duration negative pulse at the output of NAND gate A10-B which triggers timer A2. A2 is wired as a one-shot flip-flop having a pulse width of 0.1 seconds. The positive going 0.1 second pulse at the output of A2 is inverted by inverter A5-B. The rising trailing edge of A5-B's output clocks latch A3 0.1 seconds after the voltage at F4 exceeds 43.7 volts. The high at A3's D-input at the time it is clocked causes its $\overline{Q}$-output to go low.

$\overline{AZE}$ and $\overline{ELE}$ are Main Drive Servo Amplifier enable inputs from the TCC/DCC. They are gated by inverted-input AND gates A4-A and A4-D, respectively. If $\overline{AZE}$ and $\overline{ELE}$ are low when A3's $\overline{Q}$ output goes low, the A4-A and A4-D outputs go high and de-energize solid state relays K3 through K8, enabling the servo amplifiers. That is, K3 - K8 inhibit their respective servo amplifier when they are energized.

Control Logic

Refer to sheet 2 of schematic diagram 4421-0018. The Control Logic portion of the Power Relays and Control Logic consists of the:

- Power Relay Drivers
- MD (Main Drive) and NIR Relay Monitors
- Low Voltage Sensor

Power Relay Drivers

The Power Relay Drivers logic applies UP1 (high side of the UPS 120 VAC supply) to power relays K16, K17, K19 and K20. TCC/DCC output signals MPC1 and MPC2 (Main Power Control 1 and 2, respectively) drive inverters A5-C and A8-C, respectively. These inverters drive solid state relays K11 and K12 which apply 120 VAC power to Main Drive power relays K16 and K17. DC power is applied to the control input of relays K11 and K12 via transistor Q1 which is controlled by the Dead Battery signal (DB) from the Baterry Charger Monitor. If a dead battery is detected, DC power to K11 and K12 is removed which opens K16 and K17. The NIR Power Relay Drivers operation is identical to the Main Drive Relay Driver.

MD and NIR Relay Monitors

The MD Relay Monitor is identical to the NIR Relay Monitor. Therefore, only the MD Relay Monitor is described.

MRF (Main Relay Failure) is a telemetry output to the TCC/DCC. It is valid only when MPC1, the Main Drive Power Relay control signal, is low (Main Drive Power Relays are disabled). At this time, K16 and K17 should be disabled and their contacts should be open. Table 2-1 on the next page shows all possible contact conditions for K16 and K17 and the resulting potential at point A (connection between the K16 and K17 contacts).

K16 Contacts	K17 Contacts	Point A Potential	Comments
open	open	floating	normal
open	closed	grounded	via R46 and K21, or R2
closed	open	battery	
closed	closed	about 42 volts	voltage divider formed by R44, R46 and K21

Table 2-1. Main Drive Relay Failure Symptoms

Refer to the MD Relay Monitor logic schematic on sheet 2 of 4421-0018 in the *WIYN Drawings* binder (see *Appendix A*). Two voltage dividers bias two comparators in the A6 quad comparator. R24, R25 and R26 bias pin 6 at 2.0 volts and pin 5 at 10 volts. If point A is floating (normal condition), R21, R22 and R23 bias pins 4 and 7 at 2.5 volts which drives both comparators high.

The open collector comparators are wire-ORed together via RN2 which functions as a shared collector load resistor. If either amplifier has a low output, its open collector transistor is on and its output voltage is low.

If point A is grounded (see Table 2-1) A6's pin 1 drives the output low. If point A is greater than 40 volts, A6's pin 2 drives the output low. Thus, A7-B's pin 5 goes low for all possible abnormal contact combinations. When MPC1 is low, A7-B's output is an inversion of its pin 5 input. The TCC/DCC reads the contact status before asserting relay drive signals.

Low Voltage Sensor

The Low Voltage Sensor circuitry is shown in drawing 4421-0018. Comparator A1 detects battery voltage below about 41.57 VDC.

A1's pin 10 is biased at 5 VDC by voltage reference A9. R36 and R37 bias A1's pin 11 at 12.03% of the battery voltage. Thus, if the battery voltage drops below 41.57 VDC, A1's pin 11 voltage falls below the 5 VDC reference on pin 10 and the inverter's output goes low. Inverter A8-A inverts the output of A1 and passes it to the TCC/DCC.

Low Voltage Power Supplies

Refer to sheet 1 of drawing 4421-0018 in the *WIYN Drawings* binder (see *Appendix A*). PS1 and PS2 are identical commercial low voltage supplies. Powered by 120 VAC UPS power via fuses F1 and F2, they provide +15, -15 and +5 VDC for the DC Drive Power Subsystem control and logic circuits shown on sheet 2 of the drawing. PS1 provides +15 and +5 VDC; A11 is internally mounted in PS1 to provide +5 VDC from the +15 VDC output. PS2 provides -15 VDC.

Servo Amplifier Subsystem

The Servo Amplifier Subsystem is located in the 24.5-inch space directly below the blower assembly in the left-most electronics rack on the northeast side of the Second Level. It consists of:

- Servo Amplifier Subassembly (schematic diagram 4421-0019)
- Current Monitors (schematic diagram 4421-0020)
- DC Drive Power Test Load (drawing 4421-0047)

Related *WIYN Drawings* are (see the *WIYN Drawings* binder and *Appendix A*):

- DC Drive Power Rack Detail (4421-0029)
- Servo Amplifier Subassembly (drawing 4421-0026)
- Current Monitor Printed Wiring Board (drawing 4421-0022)

Servo Amplifier Subassembly

Refer to schematic diagram 4421-0019 in the *WIYN Drawings* binder (see *Appendix A*). Six Copley model 220H master servo amplifiers and two Copley model 220SH slave amplifiers drive the six Main Drive and NIR servo motors. Located inside each master unit is a plug-in header labeled PJ5 containing the passive gain and compensation components. For proper values, refer to the Copley 220 Servo Amplifier Gain/Compensation Configuration (drawing 4421-0076) In the *WIYN Drawings* binder (see *Appendix A*). For complete technical information on the Copley master and slave amplifiers, refer to the manufacturer's documentation. The amplifier-related documentation provided here is specific to the WIYN application.

The Azimuth axis requires more drive power than a single amplifier can provide. A unique Copley master slave building block feature allows efficient output power increases by adding slave amplifiers to a master unit. Each Azimuth drive motor is powered by a master and one slave which provide a peak output current of 18 amps to each Azimuth drive motor. Each elevation drive motor is powered by a master unit which provides up to 12 amps to each Elevation drive motor. Each NIR is driven by a single motor powered by a single master unit which provides up to 3 amps of drive current. While each master or slave unit can provide output currents of 12 amps, actual peak current outputs are determined by the PJ5 header component values. Table 2-2 on the next page summarizes the Main and NIR Servo drives.

Servo	Drive Motors	Master Units	Slave Units	Peak Drive Current
Azimuth	2	2	2	36 Amps *
Elevation	2	2	0	24 Amps *
WIYN NIR	1	1	0	3 Amps
MOS NIR	1	1	0	3 Amps

* Total for two motors

Table 2-2. Main Drive and NIR Servo Outputs

Refer to drawing 4421-0026. The six master and two slave amplifier modules are mounted on a 19-inch by 21-inch vertical aluminum plate. Sixteen 6800 MFD power supply filter capacitors, four Current Monitor subassemblies, four current shunts and eight protection resistors are mounted along the lower edge of the plate.

Refer to schematic diagram 4421-0019 in the WIYN Drawings binder (see *Appendix A*). The 48 VDC input power from the DC Drive Power Subsystem is connected to 1J7-4 (+) and 1J7-5 (-) of each master and slave unit. Two 6800 MFD filter capacitors are connected across the power input terminals of each unit, resulting in 81,600 MFD across the Main Drive Power input and 27,200 MFD across the NIR power input. These capacitors provide a path for high frequency amplifier current.

Each master and slave unit receives +15 VDC and -15 VDC low voltage inputs from PS1 and PS2, respectively, in the DC Drive Power Subsystem.

Control inputs are connected only to the master units. Those inputs required by slave units are provided by the respective master unit via a 9-inch 7-conductor interconnecting cable which connects 2J2 on the master unit to 1P1 on the slave unit. Master unit control inputs consist of a drive voltage from the TCC/DCC via the Analog I/O Board and Inhibit signals from the DC Drive Power Subsystem. The amplifier is inhibited by shorting 1P1-7 to 1P1-6. The DC Drive Power Subsystem processes TCC/DCC enable inputs and Inrush Holdoff signals into inhibit relay drive signals (see sheet 2 of schematic diagram 4421-0018).

The master and slave units have two modes of operation: Current Source and Voltage Source. Mode selection is via internal switch S1. This switch should by set to the Current Source position for the WIYN application.

Current Monitors

Each Azimuth and Elevation drive output is monitored by a Current Monitor. The monitor provides an analog voltage input to the Analog I/O board that is proportional to the motor current. The analog voltage is converted to digital telemetry data and passed to the TCC/DCC.

Refer to sheet 1 of schematic diagram 4421-0019. Azimuth drive motor current passes through 0.005 ohm current shunt resistor R1. At maximum Azimuth motor drive current (18 amps), R1 develops 0.09 volts. This voltage is impressed across the inputs of the Current Monitor via safety resistors R2 and R3. These resistors isolate the servo output from Current Monitor malfunctions such as short circuits, etc.

Refer to schematic drawing 4421-0020 in the *WIYN Drawings* binder (see *Appendix A*). The Current Monitor scales the small voltage across the current shunt to a larger voltage and references it to signal ground. Operational amplifier A1 amplifies the IN+ to IN- voltage difference by a factor of 51. Isolation amplifier A2 has an input and output section which are isolated from each other. A1 connects to the input section which also provides fully isolated +15 VDC and -15 VDC power for operational amplifier A1. A1's output is modulated by an internal oscillator and transformer coupled to the output section which demodulates the transformer input and passes it to the HI OUT and LO OUT terminals. External to A2, LO OUT is connected to 15R which is at signal ground. Thus, HI OUT is referenced to signal ground.

A1 has a gain of 51 and A2 has unity gain. Thus, the Current Monitor provides 0.255 volts/amp. The output impedance of A2 is about 1K ohm so a high impedance load is required to maintain accuracy. A2 in each Current Monitor drives a high input impedance analog to digital converter channel on the TCC/DCC Analog I/O board. See drawing 4421-0088 for additional Analog I/O board information.

DC Drive Power Test Load

Drawing 4421-0047 in the *WIYN Drawings* binder (see *Appendix A*) shows the DC Drive Power Test Load which provides a suitable load test resistor for each servo amplifier. Test points permit measurement of voltages across the loads. The loads are connected by disconnecting the servo motor cable(s) from the Servo Amplifier Subassembly and connecting the special jumper cable from the Servo Amplifier Subassembly to the test load.

The blower must be in operation when test loads are used. Continuous operation at maximum current may cause load resistors to overheat and will eventually discharge the batteries.

Servo Electronics Subsystem

The Servo Electronics Subsystem is a 14-inch high by 19-inch wide assembly located near the bottom of the middle equipment rack on the northeast side of the Second Level. It consists of a vertical connector panel subassembly mounted in front of a horizontal shelf. Mounted on the shelf are three subassemblies and eight power supplies. The front panel layout is shown in drawing 4421-0100; the shelf layout is shown in drawing 4421-0109 in the *WIYN Drawings* binder (see *Appendix A*).

These three custom subassemblies are mounted on the shelf:

- SES Wire Wrap Board Subassembly
- SES Sensor Switch Interface Subassembly
- SES Fuse and Relay Subassembly

The SES Wire Wrap Board Subassembly is the Servo Electronics Subsystem Logic Board. Its parts layout and schematic are drawings 4421-0101 and 4421-0063, respectively, in the *WIYN Drawings* binder (see *Appendix A*).

The SES Sensor Switch Interface parts layout and schematic are drawings 4421-0098 and 4421-0080, respectively, in the *WIYN Drawings* binder (see *Appendix A*); the SES Fuse and Relay Subassembly parts layout and schematic are drawings 4421-0135 and 4421-0062, respectively, in the *WIYN Drawings* binder (see *Appendix A*).

Hereafter, the Servo Electronics Subsystem is referred to as the SES; the Servo Electronics Subsystem Logic Board is referred to as the SES logic board; the SES Sensor Switch Interface is referred to as the sensor switch interface; the SES Fuse and Relay Subassembly is referred to as the fuse and relay board.

The SES consists the following logic functions in Figure 2-3. The noted schematic diagrams are in the *WIYN Drawings* binder (see *Appendix A*).

- Emergency Stop (E.S.) Switch Interface (4421-0098)
- Tachometer Interface (part of 4421-0101)
- SES Control Logic (part of 4421-0101)
- Emergency Stop Relays (part of 4421-0135)
- Power Control (part of 4421-0101)
- Internal Power Supplies
- Brake Drivers
- Sensor Switch Interface (4421-0098)
- Dome Control Logic

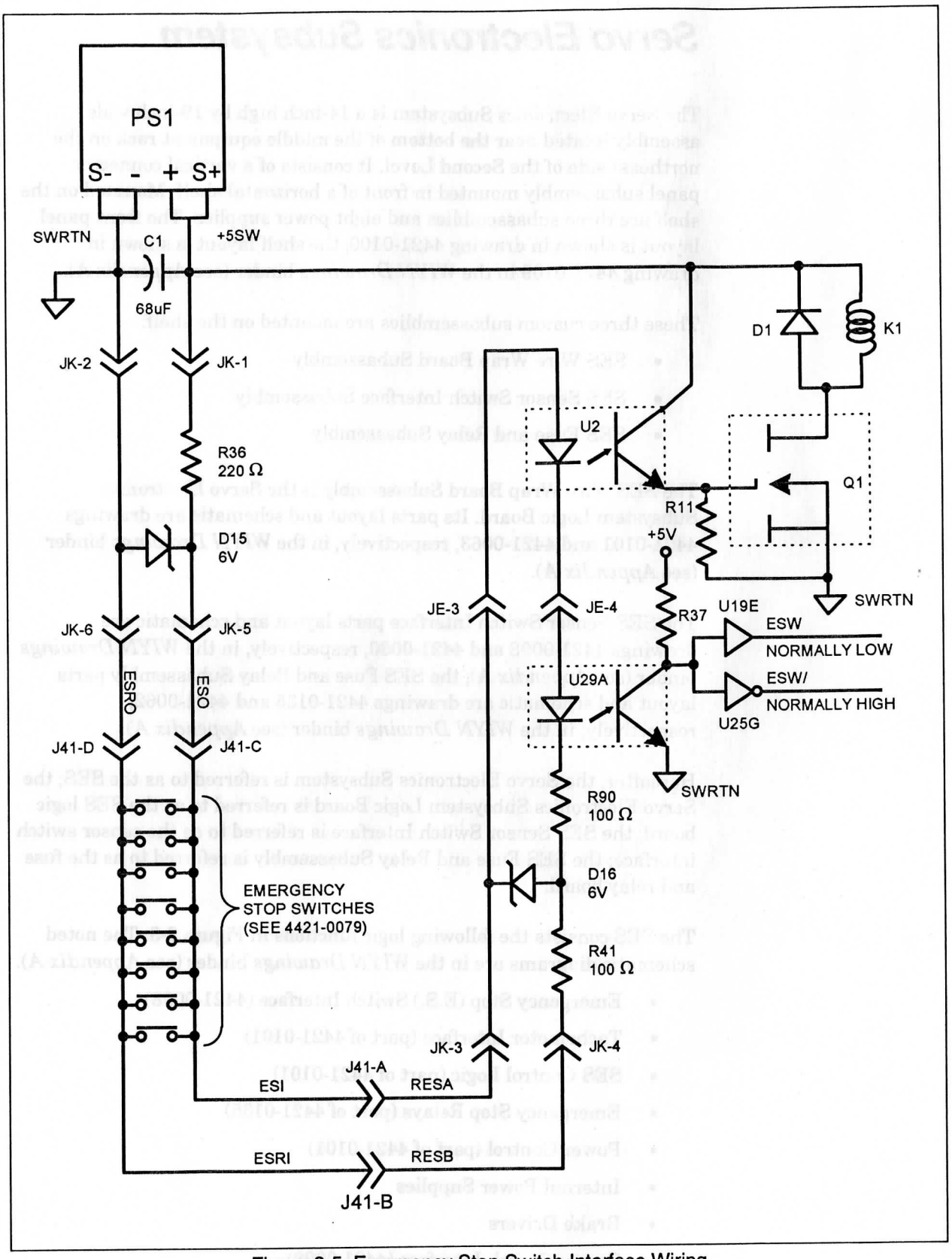


Figure 2-5. Emergency Stop Switch Interface Wiring

Emergency Stop Switch Interface

The Emergency Stop Switch Interface connects the Emergency Stop switches located throughout the observatory to the Emergency Stop Logic in the SES Control Logic section. It outputs an emergency stop signal to the SES Control Logic if one or more Emergency Stop switches are pressed, or there is an open or short in the interface wiring. Thus, for safety reasons, this logic prevents Main Drive or NIR Drive power from being applied to the servo amplifiers unless the interface is working properly.

The Emergency Stop Switch circuitry involves:

- schematic diagram 4421-0079, the Emergency Stop Switch Wiring Diagram
- schematic diagram 4421-0062 (shows fuse and relay board components and the low voltage power supplies)
- schematic diagram 4421-0063 (SES logic board components)

Figure 2-5 on the adjacent page describes the Emergency Stop Switch Interface by showing all connectors and components of the Emergency Stop Switch Interface.

PS1, the SES Switch Interface Power supply, provides 5 VDC to the interface logic. The PS1 outputs enter the SES logic board on pins JK-1 and -2 and exit on JK-5 and -6. R36 and 6-volt zener diode D15 on the SES logic board provide transient voltage protection for PS1 by limiting transients to about 6 volts peak (see the top center of 4421-0063 sheet 2).

JK-5 and -6 connect to the output end of the Emergency Stop switch wiring via pins C and D of SES front panel connector J41. The input end of the Emergency Stop Switch wiring connects to JK-3 and -4 on the SES logic board via SES connector J41-A and -B. Thus, PS1 is effectively connected to JK-3 and-4 via R36 if no Emergency Stop switches are pressed.

Refer to sheet 1 of schematic 4421-0063 and Figure 2-5. R41 and D16 serve the same function as R36 and D15 described above. Opto-isolators U29-A located on the SES logic board and U1 located on the fuse and relay board are series connected. Thus, with no Emergency Stop switches pressed, PS1 supplies 5 VDC to a series circuit consisting of R36, the photo diode in U1, the photo diode in U29-A, R40 and R41. Therefore, both opto-isolators are on. This causes ESW to be normally low and ESW/ to be normally high. ESW is a telemetry output to the TCC/DCC; ESW/ is an input to the SES Control Logic (see page 2-34).

If an Emergency Stop switch is pressed or the switch wiring is shorted, no voltage is applied across the JK-3 and -4 pins and the opto-isolators are off. This drives ESW high and ESW/ low. If the switch wiring is open, the series bias path between PS1 and the opto-isolators is broken which also turns off the opto-isolators.

Opto-isolator U1 is part of the Emergency Stop Relay logic. When U1 is on, Q1 is forward biased and relay K1 (see schematic diagram 4421-0062) is energized. K1's contacts provide AC control power to relay K16 whose AC power terminals are in the AC return path for the power relays in the DC Drive Power Subsystem (see page 2-20). Thus, an Emergency Stop switch closure or a fault in the Emergency Stop wiring removes power from the Main Drive and NIR Servo Amplifiers. This method of removing servo amplifier drive power does not rely on any logic board components. ESW/ (see the Emergency Stop Logic on page 2-34) provides an alternate method of removing power from the Main Drive and NIR Servo Amplifiers.

Tachometer Interface

The Tachometer Interface consists of the AZ OVERSPEED (Azimuth Overspeed) and EL OVERSPEED (Elevation Overspeed) processors shown on sheet 2 of schematic 4421-0063.

The Azimuth and Elevation Tachometers provide DC output voltages proportional to speed. The DC polarity is a function of direction. If the tachometer exceeds a preset threshold, the SES removes power from the drives and applies the brakes. Maximum allowed speed, and therefore threshold voltage, is a function of elevation angle. The SES detects the state of the 20° and 85° Elevation Tilt switches and adjusts the overspeed threshold accordingly.

Each processor consists of these circuits:

- Input Conditioning Circuits
- Overspeed Threshold Reference Generator
- Comparator Circuits
- Comparator to TTL Interface
- Overspeed Latch

Since the Azimuth and Elevation Overspeed Processors are identical, only the Overspeed Threshold Reference Generators are described for each processor.

Input Conditioning Circuits

The Azimuth Tachometer's differential output (AZ TACH OUT+ and AZ TACH OUT-) drives instrumentation amplifier U2 through a filter and transient protection circuit. U2 reduces common mode noise and converts the tachometer's output to a single ended input to comparators U1-A and U1-B via R5, the Azimuth Overspeed Threshold Adjustment. The output of U2 is also output to the Audio Warning Subsystem via R57 and pin 8 of connector JM.

Overspeed Threshold Reference Generator

Azimuth Overspeed Threshold Reference Generator

The Azimuth Overspeed Threshold Reference Generator consists of voltage reference U9, operational amplifiers U5-A and U5-B, and their associated discrete components.

U9 provides a precision 5 VDC reference for the remainder of the Overspeed Threshold Reference Generator circuits. U9 powers a voltage divider consisting of R15, R14, R13 and Q1. EL20, an output from the sensor switch interface, is high if the 20° Tilt Switch is open (elevation is below 20°). This turns on Q1, effectively placing R13 in parallel with R14 which results in 0.93 VDC at pin 3 of U5-A. Above 20°, elevation, Q1 is off which disconnects R13 from ground. This raises the U5-A pin 5 voltage to 3.57 VDC.

U5-A, a non-inverting unity gain amplifier, buffers the threshold reference applied to its pin-3 input. U5-B, a unity gain inverter, inverts the output of U5-A. U5-A and U5-B provide equal and opposite polarity overspeed reference voltages to U1-B and U1-A, respectively. Table 2-3 below defines the threshold reference inputs to the comparators.

Elevation	U1-B pin 5	U1-A pin 6
20° and lower	+ 0.93 VDC	- 0.93 VDC
Above 20°	+ 3.57 VDC	- 3.57 VDC

Table 2-3. Azimuth Overspeed Threshold Reference Voltages

When the telescope's elevation is below 20°, parts of the telescope can strike Observation Floor personnel during azimuth slewing. As a result, the threshold levels must be reduced for low elevation angles to protect personnel. This is a hardware safety feature.

Elevation Overspeed Threshold Reference Generator

The Elevation Overspeed Threshold Reference is modified by the 20° and 85° Tilt Switches. When the telescope is being elevated toward the zenith, the Elevation Tachometer outputs a positive voltage. When the elevation is decreasing, the Elevation Tachometer outputs a negative voltage. Above 85° and below 20°, the respective threshold voltage must be reduced so the telescope comes to a safe stop without hitting the hard stop if a servo runaway occurs.

Refer to sheet 2 of schematic 4421-0063. The positive threshold voltage is formed from the U9 precision 5-volt reference by resistors R16, R17, R18 and transistor Q2. Below 85°, EL85 (sensor switch interface output of the 85° Tilt Switch) is high, biasing Q2 off. This results in +2.89 volts at the junction of R16 and R17. Above 85°, EL85 is low which turns on Q2 and places R18 in parallel with R17. This results in +0.77 volts at the junction of R16 and 17. Operational amplifier U5-D functions as a unity gain buffer.

The negative threshold voltage is formed from the U9 precision 5-volt reference by resistors R33, R51, R31 and transistor Q3. Operational Amplifier U5-C functions as an inverting amplifier with a gain of -2.87 times the voltage at the junction of R33 and R51. Above 20°, EL20 (sensor switch interface output of the 20° Tilt Switch) is low, biasing Q3 off. This results in +1.016 volts at the junction of R33 and R51 and an output from A5-C of -2.92 volts. Below 20°, EL20 is high which turns on Q3. This places R31 in parallel with R51 which results in +0.269 volts at the junction of R51 and R31, and an output of -0.77 volts.

Table 2-4 summarizes the elevation overspeed threshold references.

Elevation	U1-C pin 9	U1-D pin 10
20° and lower	+ 2.89 VDC	- 0.77 VDC
21° to 84°	+ 2.89 VDC	- 2.92 VDC
85° and above	+ 0.77 VDC	- 2.92 VDC

Table 2-4. Elevation Overspeed Threshold Reference Voltages

Comparator Circuits

Comparators U1-B and U1-A have open collector outputs which are wire-ORed together. The output goes high only when both comparators bias their respective output transistor off. At that time, the output voltage is pulled to nearly 5 VDC via R11, D12 and R34 because no comparator current flows through R11 and D12. Because the comparators' negative power supply pin (pin 12) is powered by -15 VDC, the low output voltage approaches -15 VDC if the R5 input exceeds the azimuth overspeed threshold reference voltage for either comparator. U1-B, the positive overspeed detector, detects excessive clockwise speeds; U1-A, the negative overspeed detector, detects excessive counterclockwise speeds. Resistors R8 and R9 provide about 2 millivolts of hysteresis bias to ensure fast and reliable switching. R5 allows precise adjustment of the overspeed threshold.

Comparator to TTL Interface

The -15 VDC comparator output during overspeed conditions is not compatible with TTL circuits. D11 and D12 limit the minimum input to U8-B and U4-A to 0 VDC. D11 limits the voltage at the D11 and D12 cathodes to -0.6 VDC. Since D12 is conducting at this time, its anode is 0.6 VDC positive with respect to its cathode, making its anode 0 VDC. When both comparators are off, practically no current flows through R11 and D12, making the junction between R34 and D12 about +4.8 VDC. Thus the voltages at this junction are either 0 VDC or +4.8 VDC.

Overspeed Latch

NAND gates U4-A and U4-B form the Azimuth Overspeed Latch. U4-A's pin 1 is the set input; U4-B's pin 5 is the reset input. The set and reset inputs are normally high. At power-up, the reset input momentarily goes low, resulting in a low at U4-A's output and a high at U4-B's output. This is the normal condition (reset state) for the Azimuth Overspeed Latch. Buffer U8-C provides Azimuth Overspeed Latch telemetry to the TCC/DCC.

If a comparator senses an overspeed condition, the set input goes low, turning on the Azimuth Overspeed LED and setting the latch which remains set until $\overline{MR}$ (see page 2-41) goes low. AOS (Azimuth Overspeed), the output of U4-A, causes the Interlock Logic to remove power from the Main Drive Servo Amplifiers and apply the brakes. The purpose of the Overspeed LED is to allow easy adjustment ofthe overspeed threshold

SES Control Logic

The SES Control Logic block shown in Figure 2-3 consists of these logic blocks on sheet 1 of drawing 4421-0063.

- Emergency Stop Logic
- Interlock Logic
- Drive Power Monitors
- Watchdog Timer Logic
- Power Control Logic
- Brake Control Logic
- Servo Amplifier Enable Logic
- Reset Logic

Emergency Stop Logic

The Emergency Stop Logic consists of the following components on sheet 1 of schematic diagram 4421-0063:

- opto-isolator U29-A
- inverter U25-G
- NAND gate U21-D (shown as an inverted-input OR gate)
- inverter U25-H
- NAND gate U21-C (shown as an inverted-input OR gate)
- NAND gates U21-A and U21-B
- inverter U23-D
- NOR gate U16-D

The photo-diode side of opto-isolator U29-A is part of the Emergency Stop Switch Interface (see page 2-29); the photo-transistor side of opto-isolator U29-A is part of the Emergency Stop Logic. Normally, the transistor is on and its collector voltage is low. Buffer U19-E provides Emergency Stop Switch telemetry to the TCC/DCC and inverter U25-G presents a normally high input to U21-D.

If the console operator issues an Emergency Stop Command, the Observation Control Computer in the Control Room directs the TCC/DCC to assert TES/ (TCC/DCC Emergency Stop) which sets the Emergency Stop Command Latch consisting of NAND gates U21-A and U21-B. The latch provides a low input to U21-D when it is set. The latch remains set until it is reset by a low output from U16-D. U23-D provides Emergency Stop Latch telemetry to the TCC/DCC.

U16-D's output is low while the Drive Control Keyswitch is in the START position (U16-D's pin 12 input) or RESET is high (U16-D's pin 11 input - see RESET on page 2-41). Thus, after an Emergency Stop Command has been issued, the Main Drive and NIR Servos are restarted by momentarily turning the Drive Control Keyswitch to the START position.

U21-D combines the normally high outputs from the Emergency Stop Command Latch and U25-G (Emergency Stop Switch status) to form a normally low composite emergency stop input to inverter U25-H.

Inverted-input OR gate U21-C combines the normally high composite emergency stop input with the normally high Watchdog Timer output (see page 2-38) to form normally low AREL (A Relay). Refer to Figure 2-4 on page 2-15 and schematic 4421-0062. AREL drives the low side of solid state relay K5 which provides 120 VAC UPS power to the control input of K16 via K6, the Start Relay. K16 is in the AC return path for all AC power relays in the DC Drive Power Subsystem (see page 2-20). Thus, if an Emergency Stop Switch is pressed, an Emergency Stop Command is issued, or the Watchdog Timer fails to by clocked by the TCC/DCC, AREL goes high and all AC power relays in the DC Drive Power Subsystem are de-energized. This removes drive power from all Main Drive and NIR Servo Amplifiers and applies all brakes.

Interlock Logic

The Interlock Logic consists of the Main Drive Interlock Logic and the NIR Interlock Logic. The Interlock Logic is shown in the upper-right corner of sheet 2 of schematic diagram 4421-0063. Refer to this drawing and Figure 2-4 on page 2-15.

The Interlock Logic generates two inhibit outputs, $\overline{\text{MDINH}}$ (Main Drive Inhibit) and $\overline{\text{NINH}}$ (NIR Inhibit). $\overline{\text{MDINH}}$, when asserted, inhibits the Azimuth and Elevation Servo Amplifiers, applies the Azimuth and Elevation Brakes by de-energizing K10 and K11 (Azimuth and Elevation Brake Control Relays, respectively - see schematic diagram 4421-0063), and removes power from the Main Drive power relays. Thus, the Azimuth and Elevation Servo Amplifiers are inhibited and unpowered, and the Azimuth and Elevation Brakes are set. $\overline{\text{NINH}}$ has the same affects on the NIR drives and brakes as $\overline{\text{MDINH}}$ has on the main drives and brakes.

Main Drive Interlock Logic

Inputs to the Main Drive Interlock Logic are:

- CWHL (ClockWise Hard Limit from the sensor switch interface)
- CCHL (CounterClockwise Hard Limit from the sensor switch interface)
- UHL (Up Hard Limit from the sensor switch interface)
- DHL (Down Hard Limit from the sensor switch interface)

- TS (Tape Switch from the sensor switch interface)
- MR/ (Master Reset from the Reset Logic)
- AOS (Azimuth OverSpeed from the Tachometer Interface)
- EOS (Elevation OverSpeed from the Tachometer Interface)
- MDLO (Main Drive LockOut from the sensor switch interface)
- ILOR (Interlock Logic OverRide from the sensor switch interface)
- LP (Lift Platform from the sensor switch interface)

NOR gates U11-C and U11-D and NAND gate U17-B (shown as an inverted-input OR gate) combine CWHL, CCHL, UHL and DHL into a normally low input to NAND gate U22-A. If any of these signals is asserted high, U22-A's pin 1 goes high. The other input to U22-A is ILOR which is normally high. ILOR is low if the Interlock Override Switch on the SES Connector Panel (see drawing 4421-0100) is in the OVERRIDE position. Thus, ILOR enables or disables the hard limit switches. Buffers U10-A through U10-D provide the TCC/DCC with limit switch telemetry.

If the telescope is driven into a hard limit, the interlock logic removes power from the Main Drive Servo Amplifiers, preventing further movement. When this happens, the telescope must be backed away from the limit switch which requires power to the servo amplifiers. ILOR allows the limit switches to be defeated which reapplies power to the servo amplifiers. DO NOT leave the Interlock Override Switch in the OVERRIDE position after the telescope is backed into safe operating regions.

U22-B combines the Lift Platform switch signal with the Interlock Override and Limit Switch signal output of U22-A. The Lift Platform is normally housed in the Observation Level floor. It elevates and supports NIR instruments during their installation and removal. If this lift platform remains up (extended) during telescope rotation, the telescope may strike the lift platform. If the platform is raised above its stowed position, it actuates the Lift Platform switch which is interfaced to the SES logic board by the sensor switch interface. LP,the output of the Lift Platform switch opto-isolator, is low when the platform is stowed. U23-F inverts LP to provide a normally high input to U22-B. Thus, U22-B outputs a normally low input to U16-C. Note that the Interlock Override switch has no effect on the Lift Platform signal. Buffer U19-F provides Lift Platform telemetry to the TCC/DCC.

The Tape switch is a safety feature located on the Observation Level. If work is being performed near or on the telescope at floor level about 90° from the telescope's elevation axis, the worker could be crushed if the telescope is driven to low elevation angles. The worker can stop the telescope by touching the Tape switch located near the minimum clearance area.

TS, the Tape switch opto-isolator output, is normally high. If the Tape switch is touched, its contacts close and TS goes low. NAND gates U18-C and U18-D form a set/reset latch that is reset by $\overline{MR}$ (Master Reset - see Reset Logic on page 2-41) and set if TS goes low. If TS goes low momentarily, U18-D's output goes high and stays high until $\overline{MR}$ goes low. Thus, U18-D provides a normally low input to NOR gate U11-A. Buffer U19-C provides Tape switch telemetry to the TCC/DCC.

The Main Drive Lockout switch located on the SES Connector Panel Assembly disables the Main Drive servos when the switch is in the LOCKOUT position. This switch is placed in the LOCKOUT position when work on the telescope is performed. MDLO, the Main Drive Lockout switch opto-isolator output, is low when the switch is in the NORMAL position. Thus, both inputs to NOR gate U11-A are low, making its output normally high.

AOS and EOS, the outputs of the Azimuth and Elevation Overspeed Processors, are NORed by U11-B. The normally low inputs to U11-B result in a normally high input to inverted-input OR gate U17-A.

Both inputs to U17-A are normally high, resulting in a normally low output. Thus, U11-A's output is low unless:

- the Tape switch has been touched
- the Main Drive Lockout switch is in the LOCKOUT position
- an azimuth or elevation overspeed has occurred

NOR gate U16-C combines its two normally low inputs to form the normally high output of $\overline{MDINH}$. Inverter U23-G provides interlock telemetry to the TCC/DCC. U16-C's output is high unless:

- the Tape switch is touched
- the Main Drive Lockout switch is in the LOCKOUT position
- an azimuth or elevation overspeed occurs
- the telescope's clockwise or counterclockwise hard limit is exceeded (can be overridden)
- the telescope's upper or lower hard limit is exceeded (can be overridden)
- the Lift Platform is extended

NIR Interlock Logic

The NIR Interlock Logic generates $\overline{NINH}$, the NIR servo inhibit signal. The inputs to this logic are:

- MCWL (MOS NIR ClockWise Limit from the sensor switch interface)
- MCCL (MOS NIR CounterClockwise Limit from the sensor switch interface)

- WCWL (WIYN NIR ClockWise Limit from the sensor switch interface)
- WCCL (WIYN NIR CounterClockwise Limit from the sensor switch interface)
- ILOR (Interlock Logic OverRide from the sensor switch interface)

NOR gates U16-A and U16-B, and inverted-input OR gate U17-C function as a four-input OR gate, combining the four normally low limit inputs into a normally low output to NAND gate U17-D. Buffers U10-E through U10-H provide limit switch telemetry to the TCC/DCC. The remaining input to U17-D is driven by ILOR which can block the limit switches from shutting down the NIR servos (see page 2-36). Inverter U23-H provides NIR Interlock telemetry to the TCC/DCC.

Drive Power Monitors

The Drive Power Monitors provide servo drive power telemetry to the TCC/DCC. They opto-isolate signals derived from the 48 VDC servo power supply in the DC Drive Power Subsystem.

Refer to schematic diagram 4421-0018 in the *WIYN Drawings* binder (see *Appendix A*). When K16 and K17 close, the 48 VDC power supply begins charging the capacitors in the Servo Amplifier Subassembly, causing the voltage at point MDP (Main Drive Power) to begin rising toward 48 VDC. Zener diode D1 and R1 limit signal MP to 5 volts. MP and MPR (Main Power and Main Power Return, respectively) exit the DC Drive Power Subsystem via J2-2 and J2-24, and enter the SES via J2/2-2 and J2/4-24, respectively. From J2/2-2 and J2/4-24, MP and MPR enter the SES logic board via JG-21 and JG-22, respectively. NP and NPR, the corresponding outputs from the NIR Inrush Limiter, exit the DC Drive Power Subsystem via J2-12 and J2-25, and enter the SES via J2/2-12 and J2/4-25, respectively. From J2/2-12 and J2/4-25, NP and NPR enter the SES logic board via JG-23 and JG-24, respectively.

Refer to sheet 2 of schematic diagram 4421-0063. MP and NP are opto-isolated by opto-isolators U29-B and U29-C, respectively. The isolator outputs are low when power is applied to the servo amplifiers. These signals are inverted by U25-D and U25-F.

Watchdog Timer Logic

Refer to sheet 2 of schematic diagram 4421-0063 in the *WIYN Drawings* binder (see *Appendix A*). The Watchdog Timer logic consists of U14 and U28-A. The TCC/DCC provides a 1 Hz square wave trigger input to watchdog timer U14. As long as U14 continues to receive these triggers, its pin 7 output is continuously high. Since D-latch U28-A is also clocked by the TCC/DCC input and its D-, PR- and CL-inputs are high, U28-A is normally set and its Q-output is high.

If U14 and U28-A fail to be clocked, U14's pin 7 output toggles. Since the latch is not being clocked, it is cleared by the toggle input to its CLR pin which causes AREL to go high,removing power from the Main Drive and NIR Servo Amplifiers (see Emergency Stop Logic on page 2-34).

Power Control Logic

The Power Control Logic is part of the logic labeled Power and Brake Control on sheet 2 of schematic diagram 4421-0063 in the *WIYN Drawings* binder (see *Appendix A*). Also see Figure 2-4 on page 2-15.

Since the Main Drive and NIR Power Control are identical, only the Main Drive Power Control logic is described.

The Power Control Logic gates power control signals from the TCC/DCC with the inhibit outputs of the Interlock Logic. The TCC/DCC inputs are MPC (Main Power Control) and NPC (NIR Power Control). U12-A NANDs the active high MPC input with $\overline{\text{MDINH}}$ (Main Drive Inhibit - see page 2-37). If $\overline{\text{MDINH}}$ is high (not inhibiting), U12-A passes a low input to inverter U20-A which outputs a high to buffers U19-A and U19-B. U19-A and U19-B output MPC1 and MPC2, respectively, to the DC Drive Power Subsystem.

Refer to Figure 2-4 and sheet 2 of schematic diagram 4421-0018 (DC Drive Power Subsystem). MPC1 and MPC2 drive inverters A5-C and A8-C, respectively, on schematic diagram 4421-0018. These inverters turn on solid state relays K11 and K12 which apply UPS 120 VAC power to the high side of Main Power relays K16 and K17, respectively.

Note that the redundant Main Power relays have separate control paths from the TCC/DCC to K16 and K17. They do not share any control signals, gates, buffers, inverters, control relays or wiring. This is a safety feature that minimizes the possibility of a single component failure which could prevent de-energizing at least one power relay.

Brake Control Logic

Each Main Drive and NIR servo has an associated brake system. The brake mechanisms use spring pressure to actuate a caliper type brake. The brakes are retracted by air pressure which is applied via 120 VAC solenoid valves. When AC power is removed, the air supply is shut off and the downstream air lines and associated brake mechanism are bled down, allowing the brake to be applied. The Brake Control Logic controls AC power to the brake solenoid valves.

The Brake Control Logic is part of the logic labeled Power and Brake Control on sheet 2 of schematic diagram 44210-0063. This logic provides control inputs to the solid state brake relays located on the fuse and relay board.

Since the Azimuth and Elevation Brake Control Logic is identical, only the Azimuth Brake Control Logic is described. AZBC (AZimuth Brake Control) is an active high brake release signal from the TCC/DCC. It is NANDed with $\overline{\text{MDINH}}$ (see Interlock Logic on page 2-35) by U12-C. If $\overline{\text{MDINH}}$ is high (no inhibit), $\overline{\text{AZBCREL}}$ (AZimuth Brake Control RELease), U12-C's output to the Azimuth Brake Control Relay goes low when AZBC is high. The inhibit input from the Interlock Logic allows the Interlock Logic to override the TCC/DCC brake release signals.

The NIR brake control logic only inverts the TCC/DCC's NIR brake control signals. That is, the NIR brake control logic is not inhibited by the Interlock Logic.

Servo Amplifier Enable Logic

Refer to Figure 2-4 on page 2-15 and sheet 2 of schematic diagram 4421-0063 in the *WIYN Drawings* binder (see *Appendix A*). The Servo Amplifier Enable Logic gates TCC/DCC active high servo amplifier enable signals with active low inhibit signals from the Interlock Logic. Since the Azimuth, and WIYN and MOS NIR enable logic are identical, only the Azimuth and Elevation Enable Logic circuits are described.

NAND gate U13-D provides an active low output (AZE/ - Azimuth Enable) to the DC Drive Power Subsystem if AZEC (Azimuth Enable from the TCC/DCC) is high and $\overline{\text{MDINH}}$ from the Interlock Logic is high (not inhibiting).

The Elevation Latch Pin must be retracted before the Elevation Servo Amplifier is enabled. When the pin is retracted, ELP, the Elevation Latch Pin switch output of the sensor switch interface, goes high. NAND gate U13-A and U13-B function as an AND gate which ANDs ELP with the normally high $\overline{\text{MDINH}}$. Thus, the pin 9 input of NAND gate U13-C is high if the latch pin is retracted and the Main Drive is not interlocked. U13-C drives ELE/ low if the pin 9 input and ELEC (Elevation Enable Control from the TCC/DCC) are high. Buffer U8-D provides Elevation Latch Pin telemetry to the TCC/DCC.

Reset Logic

Refer to sheet 2 of schematic diagram 4421-0063 in the *WIYN Drawings* binder (see *Appendix A*). The Reset Logic consists of:

- Power-on Reset Generator U15
- inverters U6-B and U6-G
- NOR gate U7-A

The Reset Logic generates two outputs, RESET and $\overline{\text{MR}}$ (Master Reset). RESET, ILOR and $\overline{\text{START}}$ are combined by NOR gate U7-A to form $\overline{\text{MR}}$.

RESET

Upon SES power-up, U15 generates RESET which is a 200-500 ms high output. It resets the Dome Control Logic (refer to Chapter 3, the Dome Control Logic chapter) and the Emergency Stop Command Latch (U21-A and U21-B). RESET is also an input to U7-A which is described below.

ILOR

ILOR, the opto-isolated Interlock Override Switch output, drives the pin 1 input of NOR gate U7-A via inverter U6-B. When the Interlock Override switch is in the NORMAL position, the input to U7-A is low.

START

The Drive Control Keyswitch located in the Control Room has three positions, OFF, ON and START. The spring loaded START position drives the Control Panel SS opto-isolator which outputs $\overline{\text{START}}$. When the switch is in the START position, $\overline{\text{START}}$ is low which causes a high at the pin 2 input of U7-A.

MR

$\overline{\text{MR}}$ is the output of NOR gate U7-A . Its inputs (RESET, inverted $\overline{\text{START}}$ and inverted ILOR) are normally all low causing $\overline{\text{MR}}$ to be normally high. $\overline{\text{MR}}$ is low if the Interlock Override switch is in the OVERRIDE position, the Drive Control Keyswitch is in the START position or power has just been applied. $\overline{\text{MR}}$ resets the overspeed and tape switch latches.

Emergency Stop Relays

Refer to schematic diagram 4421-0062 in the *WIYN Drawings* binder (see *Appendix A*). The Emergency Stop Relays are K1 through K5. These relays and their support components are located on the fuse and relay board (see drawing 4421-0135 for component locations).

K1's 5 VDC coil is powered by PS1 via driver transistor Q1. Q1 is biased by opto-isolator U1 which is part of the Emergency Stop Switches Interface (description begins on page 2-29). Because PS1 is powered by 120 VAC UPS power, K1 is energized and its contacts are closed at all times. UPS power is available except while an Emergency Stop Switch is being pressed. K1's contacts provide 120 VAC UPS power to K2, K5 and a K6 contact (K6 is part of the Power Control circuitry).

K2, when enabled by BREL, energizes K3 and K4 by passing 120 VAC UPS power to their coils. BREL, an output of the Emergency Stop Logic on sheet 2 of schematic diagram 4421-0063, is normally low and goes high if an Emergency Stop Switch is pressed or a software Emergency Stop Command is issued. The contacts of K3 and K4 are used by other observatory systems. Thus, the operation of K2, K3 and K4 has no effect on the Main Drive and NIR Servo operation.

K5 is controlled by AREL which is an output of the Emergency Stop Logic. This relay passes 120 VAC UPS power to the Power Control relays when it is enabled by the normally low AREL. It goes high if an Emergency Stop Switch is pressed, an Emergency Stop software command is issued or the TCC/DCC fails to clock the Watchdog Timer (see the Emergency Stop Logic on page 2-34).

Power Control

The Power Control Relays are K6, K14, K15 and K16. Refer to schematic diagram 4421-0062 in the *WIYN Drawings* binder (see *Appendix A*) and Figure 2-4 on page 2-15. These relays are wired such that K6 must be energized before the remaining relays can function. If K6 de-energizes during normal operation, the remaining Power Control relays also de-energize.

K6, the Start Relay, is a 120 VAC relay that receives power through K5 (see Emergency Stop Relays above). K6 is wired as a self-latching relay. For it to energize, the Drive Control Keyswitch on the Control Console must be turned to the START position which shorts J44-E to J44-F. Once the Drive Control Keyswitch is released, it returns to the ON position which shorts J44-F to J44-D. This applies 120 VAC to K6's coil via its own closed contacts. Note that the control input to K16 is in parallel with K6's coil. Therefore, K16 is enabled when K6 is energized.

Figure 2-6 on page 45 shows all relays in the path for the AC power relays K15 through K20 in the DC Drive Power Subsystem. Note that relays K14, K15 and K16 are in the AC RTN path for the power relay coils. De-energizing K16 de-energizes all power relays; de-energizing K14 de-energizes the Main Drive power relays; de-energizing K15 de-energizes the NIR power relays. K14 and K15 are controlled by $\overline{\text{MDINH}}$ and $\overline{\text{NINH}}$, respectively (see Interlock Logic on page 2-35).

Internal Power Supplies

Eight low voltage power supplies designated PS1 through PS8 are mounted to the Servo Electronics Subsystem shelf. Drawing 4421-0109 shows their locations, model numbers, purpose and output voltages. Table 2-5 on the next page summarizes this information.

Supply	Function	Output(s)	Model (Condor) *
PS1	Switch Interface	+5 VDC	HB5-3/OVP-A+
PS2	SES Logic	+5, +15, -15 VDC	HTAA16W-A+
PS3	Index Sensor	+12 VDC	HA15-0.9A
PS4	Azimuth1 Encoder	+5 VDC	HB5-3/OVP-A+
PS5	Azimuth2 Encoder	+5 VDC	HB5-3/OVP-A+
PS6	Elevation Encoder	+5 VDC	HB5-3/OVP-A+
PS7	MOS Encoder	+5 VDC	HB5-3/OVP-A+
PS8	WIYN Encoder	+5 VDC	HB5-3/OVP-A+

* or equivalent

Table 2-5. SES Power Supplies

Brake Drivers

Each Main Drive and NIR servo has an associated brake system. The brake mechanisms use spring pressure to actuate a caliper type brake. The brakes are retracted by air pressure which is applied via 120 VAC solenoid valves. When AC power is removed, the air supply is shut off and the downstream air lines and associated brake mechanism are bled down, allowing the brake to be applied. The Brake Control Logic controls AC power to the brake solenoid valves.

The Brake Drivers consists of solid state relays K10 through K13 which are located on the fuse and relay board and shown on schematic diagram 4421-0062. K6, the Start Relay (see Power Control on the adjacent page), supplies 120 VAC UPS power to the Brake Drivers relays. For safety purposes, power must be applied to the air solenoid valve to release the brake. Power is applied to a respective solenoid when a relay's brake release input is low. Table 2-6 summarizes the Brake Drivers.

Relay	Servo	Brake Release Signal
K10	Azimuth	AZBCREL/
K11	Elevation	ELBCREL/
K12	MOS NIR	MBCREL/
K13	WIYN NIR	WBCREL/

Table 2-6. Brake Drivers Relays

Sensor Switch Interface

The Sensor Switch Interface isolates the SES logic board and TCC/DCC from potentially damaging, spurious induced voltages that may be induced into the long wire runs connecting them to some sensor switches. It consists of four identical PWBs which interface 12 switches each. Forty-seven of the 48 switch interfaces are used. The four sheets in schematic diagram 4421-0080, which are identical except for inputs and outputs, describe the four boards. See the *WIYN Drawings* binder and *Appendix A*.

Refer to schematic diagram 4421-0080. Since each opto-isolator is identical, only the upper-left circuit on sheet 1 of 4421-0080 is described. Each opto-isolator circuit consists of 1/4 of a quad opto-isolator IC, an input network and an output collector load resistor. The +5 VDC output of PS1, the switch interface power supply, connects to the anode of each opto-isolator's photo diode. SW RTN (Switch Return), which connects to PS1's negative output terminal and is isolated from all other circuit grounds, connects to one side of each switch. The other side of each switch connects to the input network of a particular interface circuit. For example, closure of AZ CW Soft Limit (Azimuth Clockwise Soft Limit switch) completes the bias current path consisting of the 470 ohm and 150 ohm resistors, and the photo diode. The 6-volt zener diode and 470 ohm resistor limit spurious voltages to about 6 volts.

With the photo diode forward biased, the photo-transistor turns on and its output goes low. The output side of each opto-isolator circuit is powered by the +5 VDC output of PS2, the SES logic power supply.

Dome Control Logic

The Dome Control Logic is physically part of the SES logic board and is shown on sheet 2 of drawing 4421-0063, the SES logic board schematic. However, because it is functionally part of the Dome Servo Subsystem, it is described in Chapter 3, the Dome Servo Subsystem chapter.

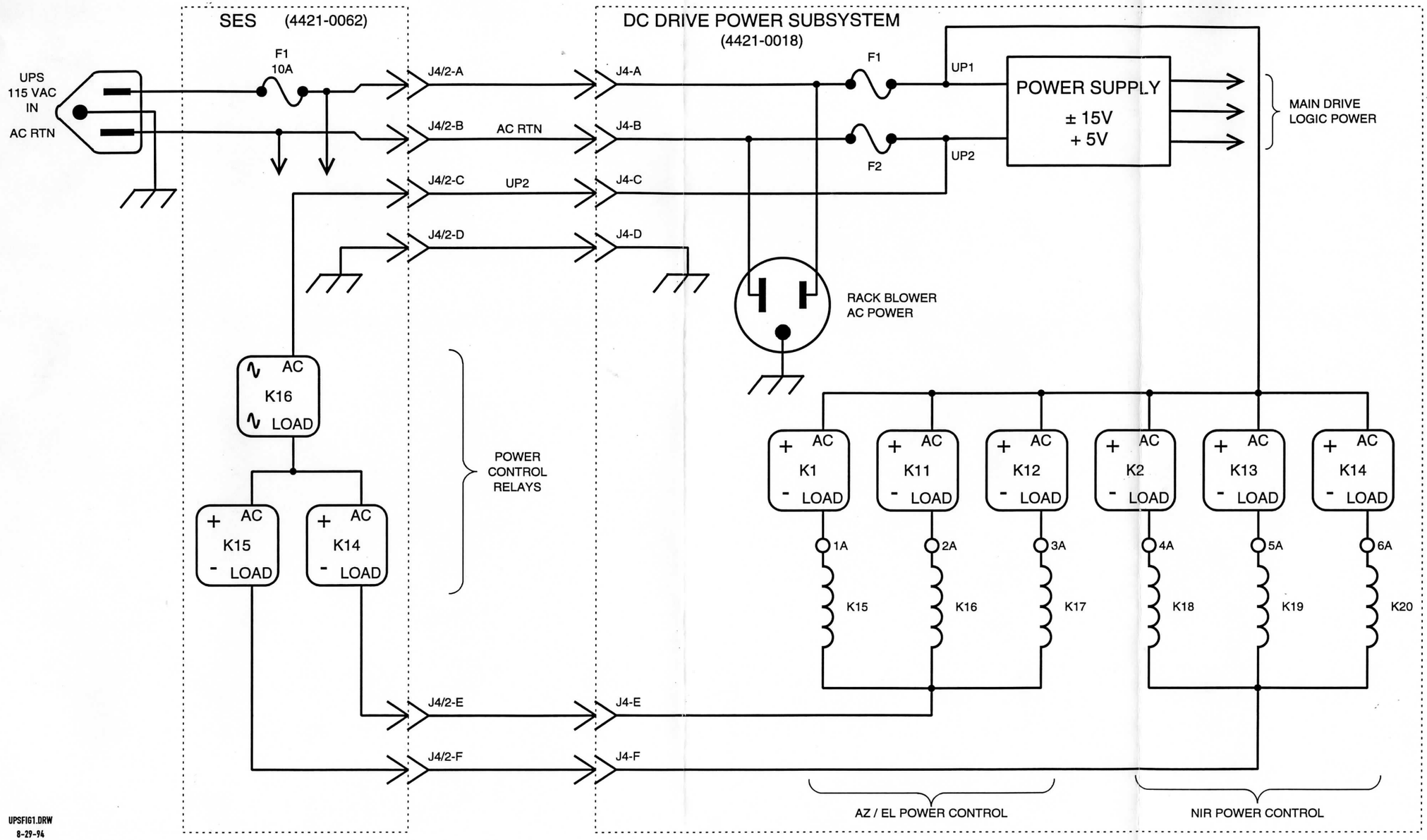


Figure 2-6. DC Drive Power Control

Chapter 3
Table of Contents

Dome Servo Subsystem 3-1

Overview 3-3

Inverters 3-3
TCC/DCC Computer 3-4
Digital I/O Interface Board 3-4
VSIO Board 3-5
Serial Opto-isolator Board 3-5
Maintenance Handpaddle 3-5
Dome Clamps 3-5
Motor Brakes 3-5
Dome Control Logic 3-6
Optical Encoder 3-6

Functional Description 3-7

Dome Control Logic 3-7
Maintenance Handpaddle Interface 3-7
Inverter Control Selector 3-7
Clamp Logic 3-8
Inverter Enable Logic 3-8
Operator Alarm Logic 3-8
Maintenance Handpaddle 3-11
Serial Opto-isolator 3-12

Detailed Circuit Description 3-13

Schematic Conventions 3-13
Logic Conventions 3-13
Dome Control Logic Interlocks 3-14
Dome Control Logic 3-17
Maintenance Handpaddle Interface 3-17
Inverter Control Selector 3-18
Clamp Logic 3-19
Inverter Enable Logic 3-20
Operator Alarm Logic 3-20
Inverter AC Power Control 3-21
Clamp Control Logic 3-21

Figures

Figure 3-1. Dome Servo Subsystem Functional Block Diagram 3-2
Figure 3-2. Dome Control Logic Functional Block Diagram 3-9
Figure 3-3. Dome Control Logic Detailed Functional Block Diagram 3-15

Tables

Table 3-1. Maintenance Handpaddle Interface Direction Logic 3-17

Dome Servo Subsystem

The Dome Servo Subsystem is an AC servo system that moves the dome so its shutter azimuth aligns with and tracks the telescope's azimuth during observations.

This chapter contains an overview of the Dome Servo Subsystem followed by functional and detailed circuit descriptions of the custom hardware components designed and built by the University of Wisconsin - Madison's Space Science and Engineering Center (SSEC). The remainder of the Dome Servo Subsystem hardware is commercial, off-the-shelf items which are documented by their respective manufacturer.

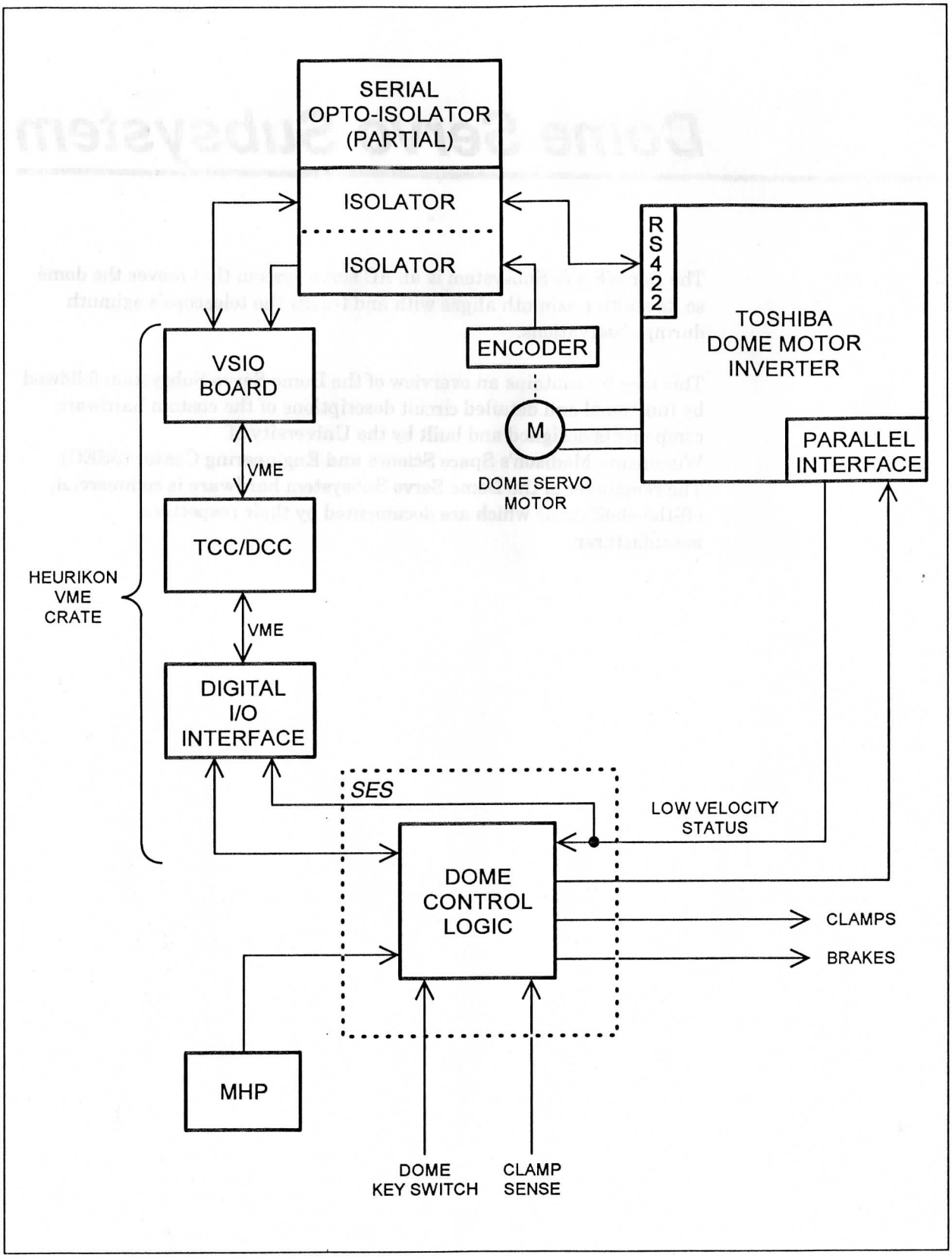


Figure 3-1. Dome Servo Subsystem Functional Block Diagram

Overview

Figure 3-1 on the adjacent page is a functional block diagram of the Dome Servo Subsystem which consists of these components:

- Inverters
- TCC/DCC (Telescope Control Computer/Device Control Computer)
- Digital I/O Interface Board
- VSIO Board
- Serial Opto-isolator Board (SSEC design)
- Maintenance Handpaddle (MHP - SSEC design)
- Dome Clamps
- Motor Brakes
- Dome Control Logic (SSEC design)
- Optical Encoder

Inverters

The dome is rotated by two 7.5 HP AC servo gearmotors powered by two Toshiba T-130G2-2080 inverters. The inverters control the speed and direction of the 208 VAC 3-phase motors by varying the phase, voltage and frequency inputs to their respective motors. These inverters are programmed and controlled via a serial RS-422 port or front panel keyboard and display. They can be controlled but not programmed through a parallel port. Both ports are available to the Telescope Control and Device Computer (TCC/DCC) but the serial port is currently the only port used by the TCC/DCC. The parallel port is currently used for dome positioning via the Maintenance Handpaddle. The parallel port also provides motor low velocity status, regardless of the port used to control the inverter.

The serial port has access to all programmable features of the inverters, but its response time is slower than the parallel port's. The parallel port features a fast response to any of seven preprogrammed motor speeds.

While the TCC/DCC currently uses only the serial port to control the Dome Motor Inverter, various combinations of serial and parallel port usage are possible. For example, by using both ports, the TCC/DCC could control inverter speed by reprogramming selectable speeds through the serial port, even while the dome is in motion, and select desired speeds through the parallel port.

The AC frequency is the primary speed controlling characteristic in an induction motor. These inverters are operated between 0.1 Hz and 100 Hz which results in a dome rotation rate of 0.004 to 4.0 degrees per second due to a 4500:1 gear reduction ratio between the motor and drive track.

TCC/DCC Computer

The Dome Servo Subsystem is controlled by the TCC/DCC which receives current dome position data from an absolute optical encoder coupled to the dome's drive track. The TCC/DCC uses current position and commanded position to compute:

- inverter output drive frequencies
- motor direction
- dome acceleration and deceleration rates
- dome clamp retraction and engaging timing
- motor brakes disengaging and engaging timing

The TCC/DCC passes the inverter-related results of these computations to both inverters.

Digital I/O Interface Board

The Digital I/O Interface is a VME bus board that interfaces the VME bus to parallel I/O ports. The port outputs to the Dome Control Logic are:

- three speed selection bits
- forward drive signal
- reverse drive signal
- clamp unlock signal
- clamp lock signal
- brake release signal

Digital I/O Interface Board inputs from the Dome Servo Subsystem are:

- dome low velocity limit status bit
- clamp air pressure sensor status bit
- Dome Inverter Failure status bit from each inverter
- Dome Key Switch position status bits

VSIO Board

The VSIO is a VME bus board that interfaces the VME bus to serial I/O ports. Because the inverters have different addresses, a single RS-422 port connects to both inverters via the Serial Opto-isolator. The VSIO board also receives dome position information from the optical Encoder via the Serial Opto-isolator.

Serial Opto-isolator Board

The Serial Opto-isolator Board provides isolation between the VME bus boards and connected external devices. In Figure 3-1, this board provides electrical isolation between the VSIO, and the inverters and Encoder.

Maintenance Handpaddle

The Maintenance Handpaddle is a handheld controller for testing the Dome Servo Subsystem independent of computer control. It has clockwise (CW) and counterclockwise (CCW) direction and clamp LOCK and UNLOCK pushbuttons, and a 7-position rotary speed selection switch.

Dome Clamps

When the dome is not being driven, two caliper brake units clamp the stiffener plate attached to the dome drive ring. The clamps are about 2.5 feet above the Observation level on the northeast and southwest sides of the dome. They are spring actuated and pneumatically released via a common solenoid valve. Clamp status is sensed via an air pressure sensor.

Motor Brakes

Each dome drive motor includes an integral brake which is electrically released before motor drive power is applied. The two brakes do not provide engaged/disengaged status to the controlling logic.

Dome Control Logic

The Dome Control Logic controls the Dome Clamps and Motor Brakes, and interfaces the Maintenance Handpaddle and TCC/DCC to the inverters. The Dome Key Switch on the SES panel selects the control source (TCC/DCC or Maintenance Handpaddle) for the inverters.

Optical Encoder

The TCC/DCC determines dome servo drive requirements by comparing the desired dome position with the present dome position. An absolute Optical Encoder coupled to the dome provides serial position information every 30 milliseconds via an RS-422 serial interface.

The encoder is located on the Observation level near the dome drive motor located on the northeast side of the observatory. It provides a serial five-byte position message every 30 milliseconds at a baud rate of 9600 bits per second. The transmission consists of a start byte, three data bytes and a checksum byte. The three data bytes provide 16 bits of binary position information. The data stream is optically isolated by one of the Opto-isolator channels before being passed to the VSIO board.

For additional information, refer to *Chapter 8*, the Serial Opto-isolator chapter.

Functional Description

This Functional Description describes these blocks in Figure 3-1 on page 3-2:

- Dome Control Logic
- Maintenance Handpaddle
- Serial Opto-isolator

Dome Control Logic

Figure 3-2 on page 3-9 is a functional block diagram of the Dome Control Logic block shown in Figure 3-1. It consists of these sections:

- Maintenance Handpaddle Interface
- Inverter Control Selector
- Clamp Logic
- Inverter Enable Logic
- Operator Alarm Logic

Maintenance Handpaddle Interface

The Maintenance Handpaddle Interface generates FWD (Forward), REV (Reverse) and BRAKE using the CW and CCW inputs. Because these inputs are generated by push buttons, BRAKE is inferred at all times except when CCW and CW are opposites. The Speed Bits are not processed by the Maintenance Handpaddle Interface.

Inverter Control Selector

The Inverter Control Selector selects the outputs of the Maintenance Handpaddle Interface (A input), the corresponding outputs of the TCC/DCC (B input) or the Default inputs (C inputs) to drive the speed and direction inputs of the inverters. Source selection is controlled by the Dome Key Switch. This switch has three positions, MAINTENANCE, COMPUTER and LOCK. When the switch is in the MAINTENANCE position, the A inputs are selected; when the switch is in the COMPUTER position, the B inputs are selected; when the switch is in the LOCK position, the C inputs (default values) are selected.

The default inputs set the speed to the lowest setting, turn off the FWD and REV direction signals, engage the brake and disable the inverters.

For simplicity, Figure 3-2 shows a single set of selector outputs. However, each inverter has a separate set of speed and direction signals. The two sets of Motor Brakes are wired in parallel and function as a single brake. Thus, only one BRAKE signal is generated.

Clamp Logic

The Clamp Logic uses the Dome Key Switch to select the source of the LOCK and UNLOCK signals. CLAMP is the output of a set/reset flip-flop which is controlled by RESET, Emergency Stop (ESW_) and the selected LOCK and UNLOCK signals. If the Dome Key Switch is in the COMPUTER position, CLAMP is also set by a software emergency stop or Watchdog timeout. When CLAMP is high, the Dome Clamp is engaged.

Inverter Enable Logic

The Inverter Enable Logic uses the status of BRAKE, CLAMP and selected LOCK to generate the inverter enable signals. When these signals are simultaneously low, the inverters are enabled.

Operator Alarm Logic

The Operator Alarm Logic provides an input to the observatory's Audio Warning Generation Subsystem if the Dome Clamps are engaged when the CW or CCW button on the Maintenance Handpaddle is pressed. Interlocks in the Dome Control Logic prevent the inverters from being enabled and the clamps from being released. The alarm indicates that the operator must release the clamps before the Dome Servo Subsystem will respond to the CW and CCW buttons. There is no operator alarm logic for the TCC/DCC inputs because the necessary interlocks are built into the TCC/DCC software.

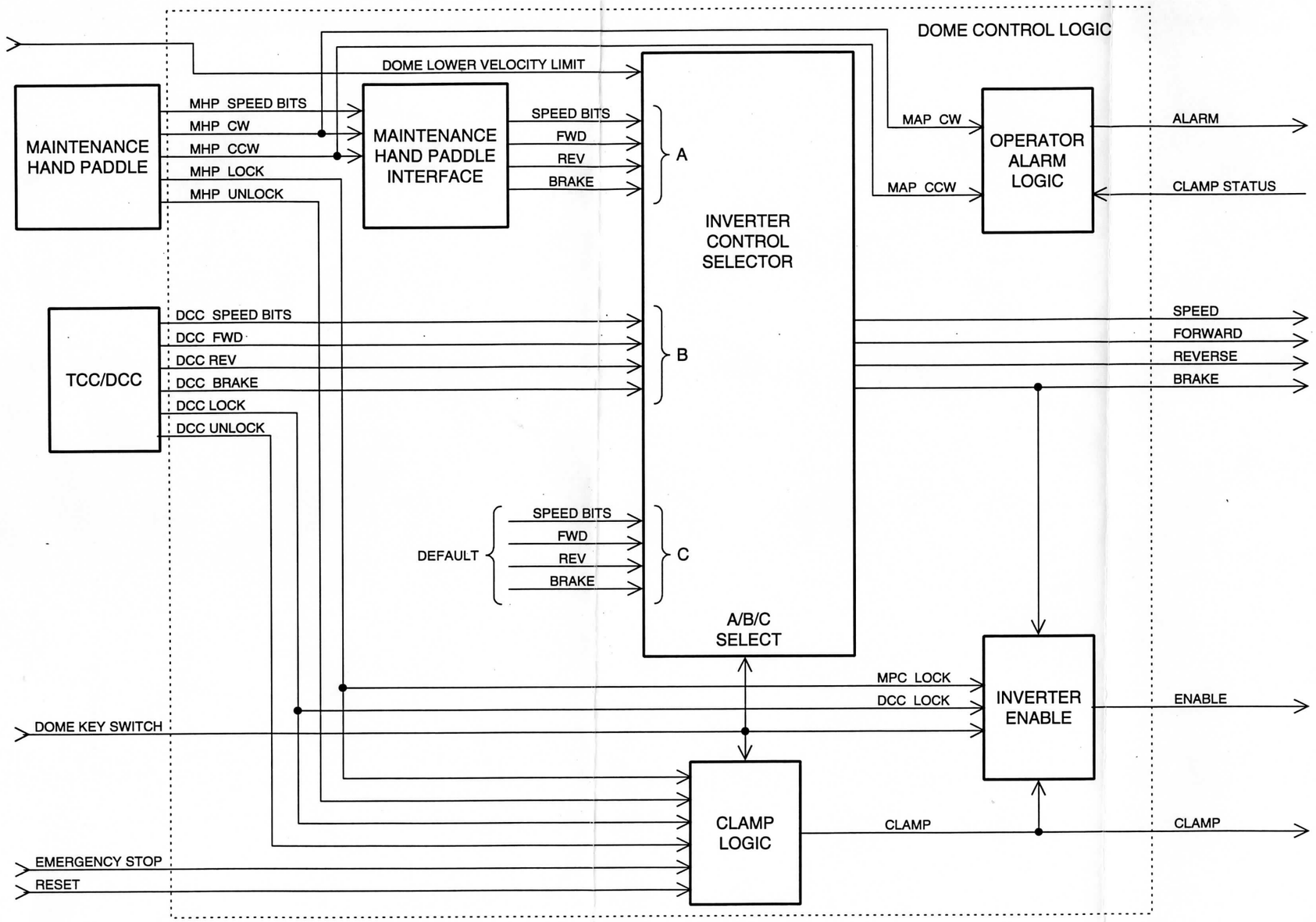


Figure 3-2. Dome Control Logic Functional Block Diagram

Maintenance Handpaddle

The Maintenance Handpaddle is a hand-held dome servo controller which controls dome movement during maintenance and testing. It is connected to one of four control ports via a 50-foot umbilical cable.

Two of the control ports are located on the Observing floor near each dome drive motor; one control port is located outside on the maintenance platform. These three control ports are wired in parallel to a plug which is connected to J35 on the SES front panel. J35 also functions as the fourth control port. To use this port, disconnect the plug connected to J35 (wired to the other three control ports) and connect the Maintenance Handpaddle directly to J35.

The Maintenance Handpaddle is a die-cast aluminum enclosure 2.06" deep by 4.70" wide by 7.39" long containing four normally-closed push-button switches and a seven-position rotary switch.

The rotary switch provides a 3-bit binary position code input to the Dome Control Logic for selecting one of seven preprogrammed speeds.

The push-button switches control the dome's clamps and direction of rotation (clockwise or counterclockwise). The push-button switches are labeled:

- CLAMP LOCK
- CLAMP UNLOCK
- MOVE CW
- MOVE CCW

The Dome servo is controlled by either the TCC/DCC computer or the Maintenance Handpaddle. To select the Maintenance Handpaddle as the source of control, rotate the Dome Control Keyswitch located in the top-center of the SES front panel to the MAINTENANCE position. To move the dome, select the desired speed, and press the CLAMP UNLOCK switch to retract the Dome Clamps. Then, press the MOVE CW or MOVE CCW switch and hold it to slew the dome clockwise or counterclockwise, respectively. Press the CLAMP LOCK button momentarily to clamp the dome.

Serial Opto-isolator

The Serial Opto-isolator optically isolates serial communications transmit and receive lines connected between the TCC/DCC's VSIO board and external devices. It can isolate 24 pairs of transmit/receive signals which may be any mix of RS-232 and RS-422 signals.

One channel of the Serial Opto-isolator isolates the transmit and receive lines between the VSIO board and the Dome Motor Inverters. Though there are two Dome Motor Inverters, only one communications channel is required because the two inverters have different I/O addresses and are thus able to be connected in parallel to the same communications channel. The Serial Opto-isolator is described in detail in *Chapter 8*.

Detailed Circuit Description

The custom electronics used in the Dome Servo Subsystem consists of the Maintenance Handpaddle, Opto-isolator and Dome Control Logic. Because of its simplicity, the Maintenance Handpaddle is not described further. Refer to its functional description on page 3-11 and drawing 4421-0092, its schematic diagram. Likewise, no additional Opto-isolator information is provided here. Refer to the Opto-isolator functional description on the previous page and *Chapter 8*.

This Detailed Circuit Description provides detailed information on:

- Dome Control Logic (located on the SES Logic board - see sheet 2 of drawing 4421-0063)
- Inverter AC Power Control
- Dome Clamp Control

SSEC drawings 4421-0096 in the *WIYN Drawings* binder (see *Appendix A*) is an Altera text design file (TDF). There is no schematic diagram in a TDF. Figure 3-3 on page 3-15 is a detailed functional drawing of the Dome Control Logic. Refer to it and the TDF during this Detailed Circuit Description which discusses the logic of each block shown in the functional block diagram in Figure 3-2 on page 3-9. Also refer to drawing 4421-0063, the Servo Electronics Subsystem Logic Board schematic diagram.

Schematic Conventions

The Dome Control Logic is contained in two Altera EPM5032DC-2 Erasable Programmable Logic Devices (EPLDs) located at U24 and U26 on the SES circuit board in the SES Assembly. For EPLD input and output signals, the external name may not be identical to the internal name. Signal names used in Figure 3-3 on page 3-15 are the signal names used in the TDF.

Logic Conventions

Logic signal names are indicated by all uppercase letters and numbers, e.g., SINT. A logic signal name ending with an underscore (_) or slash (/) represents an active low signal, e.g., LINT_ or LINT/.

Some conventions for describing the state of a logic signal are true or false, high or low, one or zero, and active or inactive. High and low is the convention used in this discussion because it best describes the physical condition of a logic signal and is better suited for troubleshooting.

When a signal is *asserted*, it is in its active state.

Dome Control Logic Interlocks

Certain dome control commands and logic contain interlocks which prevent equipment damage and personal injury. The status of the following devices or signals is used for interlocking output control signals in some modes of operation:

- Dome Key Switch position
- Inverter velocity low limit signal
- Dome clamp pressure switch signal
- COMPUTER mode watchdog time-out
- COMPUTER mode software stop command
- COMPUTER mode brake signal
- COMPUTER mode lock signal
- MAINTENANCE mode Emergency STOP button
- MAINTENANCE mode Maintenance Handpaddle LOCK button

The Dome Control Logic receives inputs from either the Maintenance Handpaddle or the TCC/DCC. The Dome Key Switch generates the KEY_MAINT_ and KEY_COMP_ signals which are active low signals used by the Dome Control Logic to determine control source. The switch positions and resulting output signals are:

- MAINTENANCE position or mode (KEY_MAINT_ signal is low)
- COMPUTER position or mode (KEY_COMP_ signal is low)
- LOCK position or mode (KEY_MAINT_ and KEY_COMP_ signals are high)

The SUBDESIGN section at the top of the TDF defines all inputs and outputs. The DEFAULT section describes the outputs after initialization and any time the outputs are interlocked. The remainder of the TDF describes these sections in Figure 3-3:

- Maintenance Handpaddle Interface
- Inverter Control Selector
- Clamp Logic
- Inverter Enable Logic
- Operator Alarm Logic

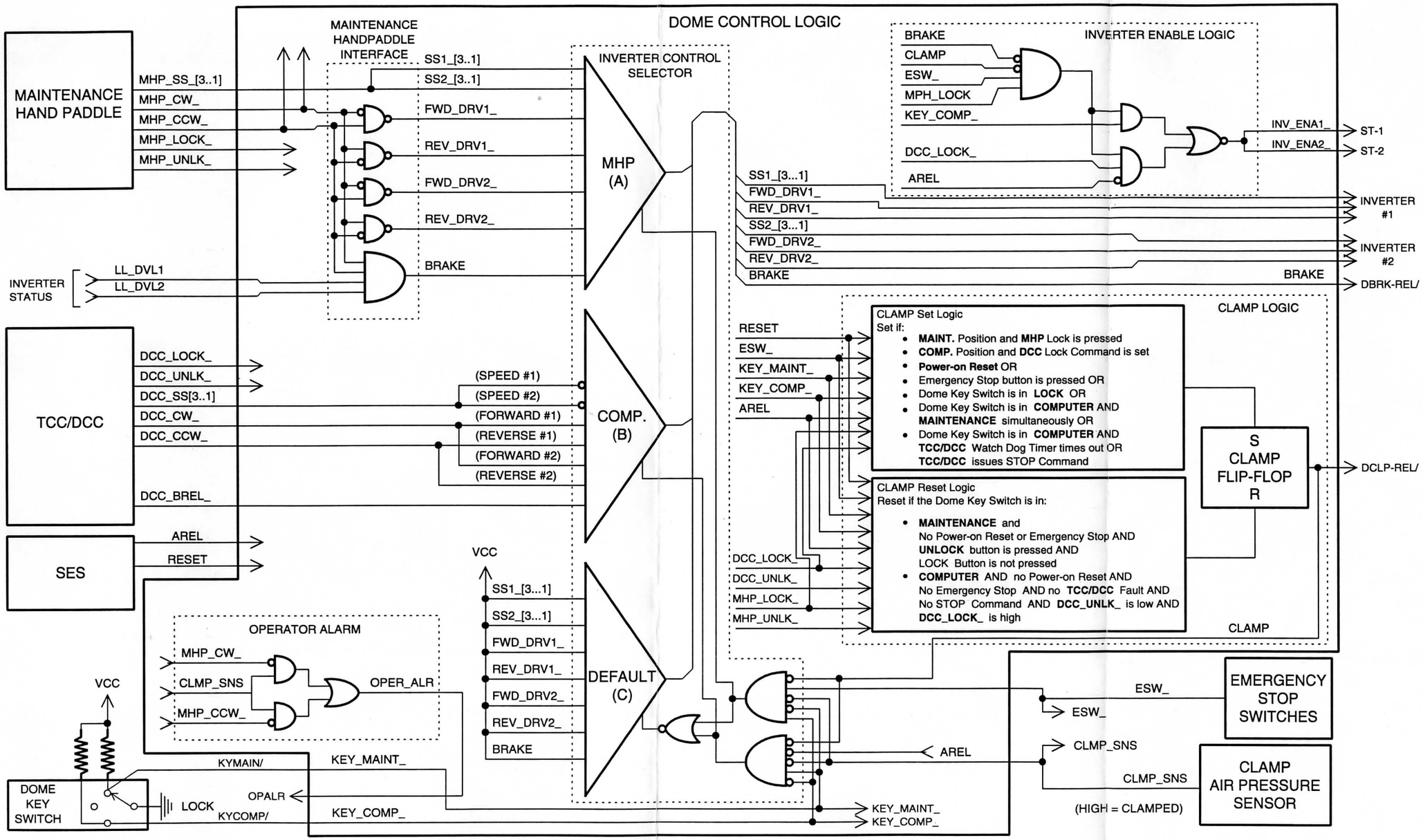


Figure 3-3. Dome Control Logic Detailed Functional Block Diagram

Dome Control Logic

Figure 3-2, the Dome Control Logic Functional Block Diagram shown on page 3-9, consists of these functional sections:

- Maintenance Handpaddle Interface
- Inverter Control Selector
- Clamp Logic
- Inverter Enable Logic
- Operator Alarm Logic

Maintenance Handpaddle Interface

The Maintenance Handpaddle Interface generates the forward and reverse signals for both inverters, and the brake signal. The forward and reverse drive signals are driven by MHP_CW_ and MHP_CCW_. Table 3-1 below describes the forward and reverse drive signals.

MHP_		FWD_		REV_	
CW_	CCW_	DRV1_	DRV2_	DRV1_	DRV2_
low	low	high	high	high	high
low	high	low	low	high	high
high	low	high	high	low	low
high	high	high	high	high	high

Table 3-1. Maintenance Handpaddle Interface Direction Logic

The brake is applied only after the dome has slowed to a safe low speed following the operator's release of the CW or CCW button. This is accomplished by ANDing the inverters' low velocity limit signals (LL_DVL1 and LL_DVL2) with MHP_CW_ and MHP_CCW_.

MHP_CW_ and MHP_CCW_ are inactive high when neither the CW nor the CCW buttons on the Maintenance Handpaddle are being pressed; LL_DVL1 and LL_DVL2 are high when the respective inverter's output frequency is below the programmed low speed threshold.

Inverter Control Selector

Dome speed, direction and braking are controlled by the Maintenance Handpaddle, TCC/DCC or Default. Each source generates a complete set of dome motion control signals. The Inverter Control Selector functions as a one-of-three multiplexer which selects Maintenance Handpaddle, TCC/DCC or Default controls to control dome motion. The Maintenance Handpaddle and TCC/DCC control equations are designed such that both sets can never be true simultaneously. However, both sets may be false simultaneously which cause all control output signals to go to their default settings. The KEY_MAINT_ and KEY_COMP_ outputs of the Dome Key Switch are the primary source selection signals.

WARNING

The software stop command has no effect when the Dome Key Switch is in the MAINTENANCE position.

Maintenance Handpaddle Interface Inputs

The AND/OR select logic selects the Maintenance Handpaddle Interface Inputs to drive the inverters if all conditions below are met.

- the Dome Key Switch is in the MAINTENANCE position
- emergency stop (ESW_), which can only be asserted via emergency stop buttons located throughout the observatory, is not asserted
- the CLAMP flip-flop is reset (unclamped)
- CLMP_SNS, the clamp pressure switch feedback signal, is high verifying the clamp is disengaged

Assuming the above conditions are met, the three-bit speed lines from the Maintenance Handpaddle are gated to the motor inverters. Now, if the CW button on the Maintenance Handpaddle is pressed, the forward drive signals to the motor inverters go active (FWD_DRV1_ and FWD_DRV2_); if the CCW button is pressed, the reverse drive signals go active (REV_DRV1_ and REV_DRV2_). If the CW and CCW buttons are pressed simultaneously, both sets of drive signals go inactive. The Maintenance Handpaddle outputs a full count for the slowest speed and a zero for the highest.

TCC/DCC Inputs

The AND/OR select logic selects the inputs from the TCC/DCC to drive the inverters if all conditions below are met.

- the Dome Key Switch is in the COMPUTER position
- emergency stop (ESW_), which can only be asserted via emergency stop buttons located throughout the observatory, is not asserted
- the CLAMP flip-flop is reset (unclamped)
- CLMP_SNS, the clamp pressure switch feedback signal is high verifying the clamp is disengaged
- AREL is low (the TCC/DCC watchdog time-out did not occur and the software stop command was not issued)

If these conditions are met, the brake, direction and speed bit signals are under control of the TCC/DCC. The speed bits function the same as when the Maintenance Handpaddle is in control. No hardware logic interlocks prevent forward and reverse drive signals from being applied simultaneously, or the brake from being applied while driving the dome at full speed. However, these are illegal software operations. Thus, the TCC/DCC employs software interlocks, while the Maintenance Handpaddle Interface employs hardware interlocks.

If the TCC/DCC control conditions are not met, the brake, speed bits, and forward and reverse direction signals go to their default conditions.

Clamp Logic

The Clamp Logic consists of a set/reset flip-flop labeled CLAMP, and associated AND/OR set and reset logic. The dome clamp is engaged when CLAMP is high (set) and disengaged when CLAMP is low (reset).

The CLAMP AND/OR logic uses the Dome Key Switch position to select the logic sources for its set and reset inputs. These switch positions are:

- LOCK
- MAINTENANCE
- COMPUTER

Set Logic

When the Dome Key Switch is in the LOCK position, the CLAMP flip-flop is set. It is set in the MAINTENANCE position if:

- the Maintenance Handpaddle clamp LOCK button is pressed, OR
- an SES reset occurs, OR
- an emergency stop occurs.

When the Dome Key Switch is in the COMPUTER position, the CLAMP flip-flop is set if:

- there is a TCC/DCC lock signal, OR
- the TCC/DCC Watchdog Timer times out (input to the AREL logic), OR
- the operator issues a software stop command (input to the AREL logic), OR
- an SES reset occurs, OR
- an emergency stop occurs.

Reset Logic

Once the flip-flop is set, it remains set even if the condition that initially set it passes. Assuming no CLAMP flip-flop setting condition is currently active, the CLAMP flip-flop is reset if:

- the Dome Key Switch is in the MAINTENANCE position and the UNLOCK button on the Maintenance Handpaddle is pressed, OR
- the Dome Key Switch is in the COMPUTER position, the DCC_UNLK_ signal is active and the watchdog Timer is not timed out.

Inverter Enable Logic

The first equations in the TDF define the inverter enables. These conditions must all be met before the inverters can be enabled:

- emergency stop (ESW_) must not be asserted
- the motor brakes must be disengaged
- the Maintenance Handpaddle clamp LOCK button must be released

In addition, if the Dome Key Switch is in the COMPUTER position,

- DCC_LOCK_ cannot be asserted
- the TCC/DCC watchdog timer must not be timed out
- the software stop command cannot be active

If any condition is not met, the inverter enable signal goes to its default disabled setting as defined in the DEFAULT section of the TDF.

Operator Alarm Logic

The last equation defines the OPER_ALR signal which alerts the operator that the maintenance Handpaddle CW or CCW button is being pressed while the clamp pressure switch indicates the clamp is engaged. The signal enables an alarm output from the audio system.

Inverter AC Power Control

Each Dome Inverter contains an integral AC power relay which must be energized to apply power to the remainder of the respective inverter. Relay excitation power is 120 VAC UPS power which is controlled by circuits in the SES.

Refer to drawing 4421-0062, the Servo Electronics Subsystem Power Distribution drawing. In the SES, connector J34 pin F provides AC power to a power relay in each Dome Motor Inverter. This pin receives 120 VAC UPS power via the Dome Keyswitch. When the Dome Keyswitch is in the MAINTENANCE position, J34-F is powered via relay K4; when the Dome Keyswitch is in the COMPUTER position, J34-F is powered via relay K6; when the Dome Keyswitch is in the LOCK position, AC power is disconnected from J34-F.

Refer to drawing 4421-0062. When the Dome Keyswitch is in the MAINTENANCE position, K1, K2 and K4 must be energized to apply AC power to J34-F. K4 energizes if K1 and K2 energize. K1 and K2 are part of the Main Drive and NIR power control logic. For information on control of K1, refer to the Emergency Stop Switch Interface description on page 2-27; for information on the control of K2, refer to the Emergency Stop Relays description on page 2-39.

Refer to drawing 4421-0062. When the Dome Keyswitch is in the COMPUTER position, K1, K5 and K6 must be energized to apply AC power to J34-F. These relays are part of the SES Power Control circuitry which is shared by the Main Drive and NIR Servos. For information on K1 and K5, refer to the Emergency Stop Relays description on page 2-39; for information on K6, refer to the Power Control description on page 2-40.

Clamp Control Logic

The Dome Clamps engage via spring pressure and release via air pressure. Air pressure is supplied to both clamp mechanisms via a common 120 VAC air solenoid valve. This valve is powered by 120 VAC UPS power via K7 in the SES Fuse and Relay Assembly (see drawing 4421-0062). Power is applied to K7's AC input terminal anytime AC power is applied to the Dome Inverter Power Relays (described above). Thus, K7 can release the clamps anytime power is applied to the inverters. When AC power is applied to K7, the clamps are released if the enable input to K7 (DCLP-REL/ - Dome CLamP RELease) is low. This signal is an output of the CLAMP flip-flop in the Dome Control Logic (see Clamp Logic on page 3-19).

Chapter 4
Table of Contents

Encoder Interface Module 4-1

Overview 4-1

Functional Description 4-3

Position Generator 4-3
Line Receivers 4-3
Quadrature Decoder 4-4
Encoder Tracker 4-4
Index Sensor Interface 4-5
Time Signal Generator 4-5
VME Bus Interface 4-5

Detailed Circuit Description 4-7

Schematic Conventions 4-7
Logic Conventions 4-7
Position Generator 4-8
Line Receivers 4-8
Quadrature Decoder 4-8
Encoder Tracker 4-9
Index Sensor Interface 4-11
Input Filter and AMP03 Differential Amplifier 4-12
Amplifier Output Filter and Limiter 4-12
Comparator 4-13
Time Signal Generator 4-13
VME Bus Interface 4-14
VME Interrupter 4-15
Address Decoder 4-15
Index Status Register 4-15
Interrupt Vector Register 4-17
Wait State Generatior 4-17

Figures

Figure 4-1.Encoder Interface Module 4-1
Figure 4-2. Encoder Interface Board Functional Block Diagram 4-2
Figure 4-3. Encoder Tracker Arbiter State Diagram 4-10

Tables

Table 4-1. Encoder Signal Routing 4-9
Table 4-2. Index Sensor Signal Routing 4-12
Table 4-3. VME Base Address Coding 4-15
Table 4-4. Encoder Interface Module Memory Map 4-16

Encoder Interface Module

The Encoder Interface Module (EIM) is a component of the position feedback chain for the telescope pointing servo system which is part of the WIYN Telescope Control System (TCS). The EIM is a VME bus circuit card that is installed in a Heurikon HSE/10 VME enclosure in Servo Rack II.

Overview

The EIM processes signals from five rotary incremental optical encoders, four magnetic displacement sensors and the time code receiver card. It contains slave and interrupter functional modules as described in the ANSI/IEEE 1014 VME specification.

Figure 4-1 is an outline of the EIM card.

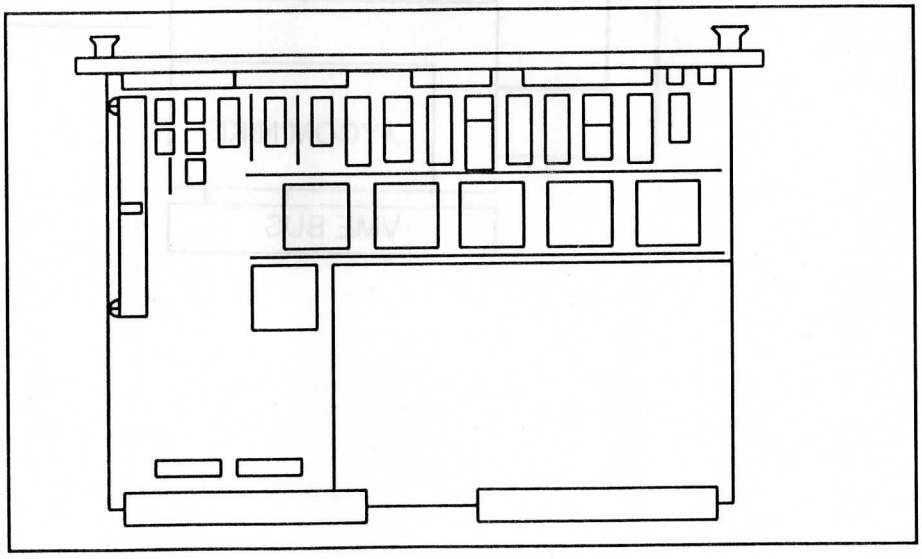


Figure 4-1. Encoder Interface Module

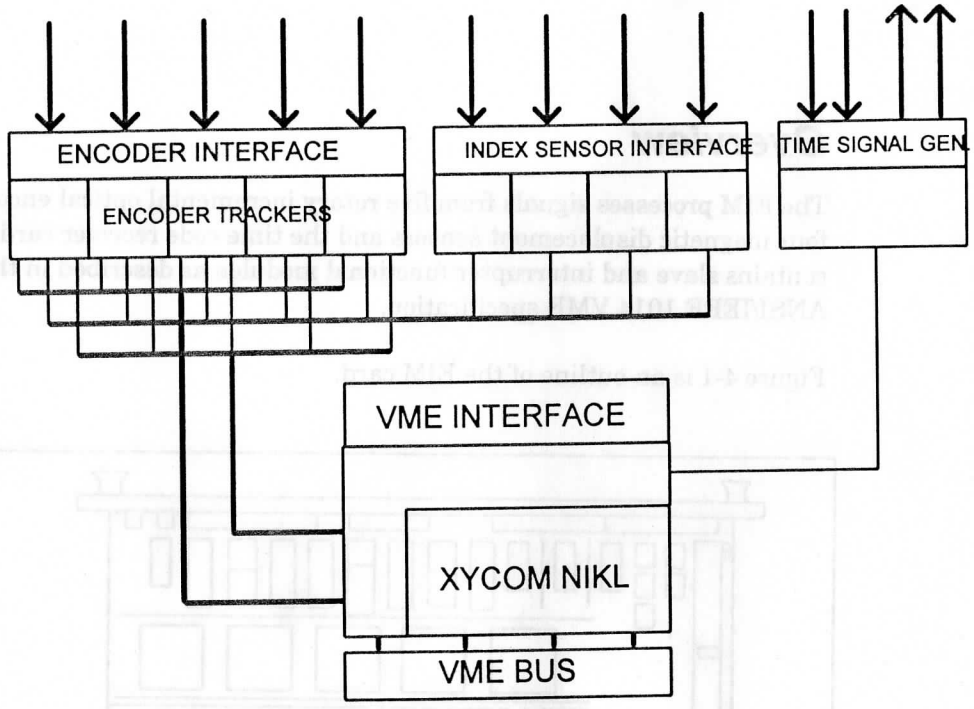


Figure 4-2. Encoder Interface Module Block Diagram

Functional Description

Refer to Figure 4-2. The EIM consists of these four functional sections:

- Position Generator
- Index Sensor Interface
- Time Signal Generator
- VME Bus Interface

Optical encoders provide position feedback in the Azimuth, Elevation, and two Nasmyth Instrument Rotator servo positioning systems. Two encoders on the azimuth axis sense azimuth rotation independently. They are mounted such that together, they cancel motion caused by slight tipping of the telescope's azimuth axis due to wind loading, imbalances, etc. The Telescope Control Computer (TCC) uses the difference between the requested position (operator input) and the current position (encoder position input) as a major criteria in forming the servo drive signals.

Position Generator

The Position Generator consists of five identical sections, one for each encoder. Each section forms a 32-bit reference position word and a 32-bit relative position word for the TCC.

The TCC compares the reference position word to the relative position word to compute absolute angular position. Each Position Generator section consists of:

- two Line Receivers
- a Quadrature Decoder
- an Encoder Tracker

Line Receivers

The Line Receivers convert differential inputs to TTL levels for use by the Quadrature Decoder and Encoder Tracker sections.

Quadrature Decoder

The Line Receivers section outputs two quadrature outputs. They are identical except one signal leads the other as a function of the direction of rotation. Thus, either signal can provide incremental change pulses to the Encoder Tracker section but both signals are required to determine the direction of the position change.

The Quadrature Decoder generates incremental change pulses and a direction signal from the quadrature inputs which are used by the Encoder Tracker.

Encoder Tracker

The Encoder Tracker receives these inputs:

- incremental change pulses from the Quadrature Decoder
- a direction signal from the Quadrature Decoder
- a 5 millisecond clock from the Time Signal Generator
- an index pulse from the Index Sensor Interface.

Using these inputs, the Encoder Tracker generates a relative position word and an index reference word for the TCC. The Encoder Tracker contains these functions:

- 32-bit binary up/down counter
- 32-bit Relative Position Latch
- 32-bit Index Reference Latch

The counter is incremented or decremented by the encoder pulses as a function of the direction of rotation. The counter's up/down control is driven by the direction control signal from the Quadrature Decoder.

The counter's output count is not referenced to any physical reference on the rotatable device. That is, its count is meaningless until a particular count can be assigned to the index position of the rotatable device. During initialization, the device is rotated until the Index Sensor outputs a pulse which strobes the counter's output into the Index Reference Latch. This latch provides the TCC with the count associated with the index position.

The Relative Position Latch is strobed every 5 milliseconds by a clock input from the Time Signal Generator. This latch provides near real-time relative position for the TCC.

The TCC determines absolute position by subtracting the index reference count from the relative position count.

Index Sensor Interface

The Index Sensors are Sony PD-10 Magnesensors. They generate an analog signal with a repeatable, precise, position dependent, zero volt crossing. Each Index Sensor consists of a magnet mounted on the movable telescope component and a sensor mounted on a fixed position in close proximity to the path of the magnet on the rotating device. As the magnet passes the sensor, an analog signal is induced into the sensor which is filtered, amplified and converted to a corresponding TTL level pulse by the Index Sensor Interface.

Each index sensor has an Index Sensor Interface section whose output strobes the position count into the Index Reference Latch in the respective Encoder Tracker.

Time Signal Generator

The Time Signal Generator block receives 1 Hz and 10K Hz pulses from the TPRO Time Code Receiver card. It derives 50% duty cycle 200 Hz, 1K Hz, and 1 Hz clocks from these signals. The 200 Hz and 1 KHz clocks are synchronized to the 1 Hz signal. The 200 Hz clock is sent to the Encoder Trackers to latch the counts at a regular interval. It also goes to the VME interface interrupter to inform the TCC of the new position data in the Encoder Trackers and to provide a general purpose heartbeat for the TCS. The 1 KHz and 1 Hz clocks are differentially driven and distributed in a bus configuration via the Serial Opto-Isolator box (see drawing 4421-0142) to several locations in the WIYN observatory.

VME Bus Interface

The Encoder Interface card is built on a prototype board. As delivered by its manufacturer, these cards contain a user application wire-wrap section, and part of a VME Bus Interface which is the printed circuit section of the board. The printed circuit area provides a partial interrupter, some decoding, handshaking, buffering and a simple interface between the prototyping area of the board and the VME bus. The remainder of the interface is part of the wire-wrap portion of the board which consists of these logic functions:

- the remainder of the VME interrupter
- the remainder of the address decoding
- an Index Status Register
- an Interrupt Vector Register
- a Wait State Generator

Detailed Circuit Description

The schematic diagram of the Encoder Interface Module is SSEC drawing 4421-0030 in the *WIYN Drawings* binder (see *Appendix A).* This Detailed Circuit Description discusses the logic of each block shown in the functional block diagrams in Figure 4-2 on page 4-2.

Schematic Conventions

The Encoder Interface Module is built on Xycom's XVME-085 prototype board. Most of the VME bus interface is in a printed circuit section of the board called NIKL which is documented by Xycom. The remainder of the board is a wire-wrap protyping section where the remaining encoder logic resides. Components on the NIKL are referenced by designators silk screened on the circuit board; components on the prototype area are referenced by adhesive labels on the wire side of the board. Component designators may conflict in these two areas. All references to schematic circuit symbols in this manual refer to components in the prototype section of the board unless stated otherwise. References to schematic circuit symbols of a multiple section device use the symbol ID followed by a hyphen and the letter designator, e.g. section A of a 26LS33 line receiver IC located at U6 is called U6-A. The circuit symbol alone refers to single function ICs.

Logic Conventions

Logic signal names are indicated by all uppercase letters and numbers, e.g. SINT. A logic signal name ending with a trailing slash represents an active low signal, e.g. LINT/.

Some conventions for describing the state of a logic signal are true or false, high or low, one or zero, and active or inactive. In this discussion, all logic states are described as high and low. This convention best describes the physical condition of a logic signal and is better suited for troubleshooting.

Frequently, a logic signal is *asserted*, which means that a signal is in its active state.

Some of the Encoder Interface Module logic is contained in EPLDs which are described via equivalent schematic diagrams and/or text files in the *WIYN Drawings* binder (see *Appendix A*).

Position Generator

Heidenhain ROD800 encoders drive Heidenhain EXE650B interpolators which output incremental position change pulses to the Position Generator. The encoders output a quadrature analog voltage proportional to the light level passing through the encoder plate. This voltage changes from minimum to maximum and back to minimum in 1/100 of a degree of rotation. The interpolators increase encoder resolution by a factor of 25 by processing the light intensity range input from the encoder. Thus, each input pulse to the Position Generator represents 1/2500 degree of rotation.

The Position Generator consists of five identical sections, one for each encoder. Each section contains:

- two Line Receivers
- a Quadrature Decoder
- an Encoder Tracker

Line Receivers

Refer to sheet 1 of the schematics. The encoders connect to JP2 via the SES Connector Panel. Encoder signals enter the SES connector panel via MS connectors J6, J7, J13, J23 and J25. A cable harness connects to the encoder signal pins on the MS connectors which terminates in plug P9. P9 plugs into J9 on the VME crate which connects to JP2 on the Encoder Interface Board. For each encoder, two 26LS33 differential line receivers convert the differential quadrature inputs to quadrature TTL outputs. Table 4-1 on the next page shows the complete path between the MS connectors and the respective line receiver on the Encoder Interface.

Quadrature Decoder

The line receiver outputs drive LS7084 quadrature clock converters which output incremental pulses and direction signals. The converters output a pulse on each edge of the quadrature signals which quadruples the pulse frequency and resolution. Thus, 10,000 pulses are generated for each degree of encoder shaft rotation. The LS7084s are biased for a maximum output pulse frequency of approximately 5 MHz. The pulses and direction signals drive the Encoder Tracker.

SES Front Panel Connector (4421-0100)	Encoder Signal Name	VME Crate Backpanel Connector P9/S9 Pin No.	Encoder Interface JP2 Pin No.	Line Receiver
J6-A	AZ1 + Sig 1	P9-01	1	U13A-2
J6-B	AZ1 - Sig 1	P9-14	2	U13A-1
J6-D	AZ1 + Sig 2	P9-02	3	U13B-6
J6-E	AZ1 - Sig 2	P9-15	4	U13B-7
J7-A	AZ2 + Sig 1	P9-03	5	U13C-10
J7-B	AZ2 - Sig 1	P9-16	6	U13C 9
J7-D	AZ2 + Sig 2	P9-04	7	U13D-14
J7-E	AZ2 - Sig 2	P9-17	8	U13D-15
J13-A	EL + Sig 1	P9-05	9	U14A-2
J13-B	EL - Sig 1	P9-18	10	U14A-1
J13-D	EL + Sig 2	P9-06	11	U14A-6
J13-E	EL - Sig 2	P9-19	12	U14A-7
J23-A	MOS +Sig 1	P9-22	17	U15A-2
J23-B	MOS -Sig 1	P9-09	18	U15A-1
J23-D	MOS +Sig 2	P9-10	19	U15B-6
J23-E	MOS -Sig 2	P9-23	20	U15B-7
J25-A	WIYN +Sig 1	P9-20	13	U14C-10
J25-B	WIYN -Sig 1	P9-07	14	U14C-9
J25-D	WIYN +Sig 2	P9-08	15	U14D-14
J25-E	WIYN -Sig 2	P9-21	16	U14D-15

Table 4-1. Encoder Signal Routing

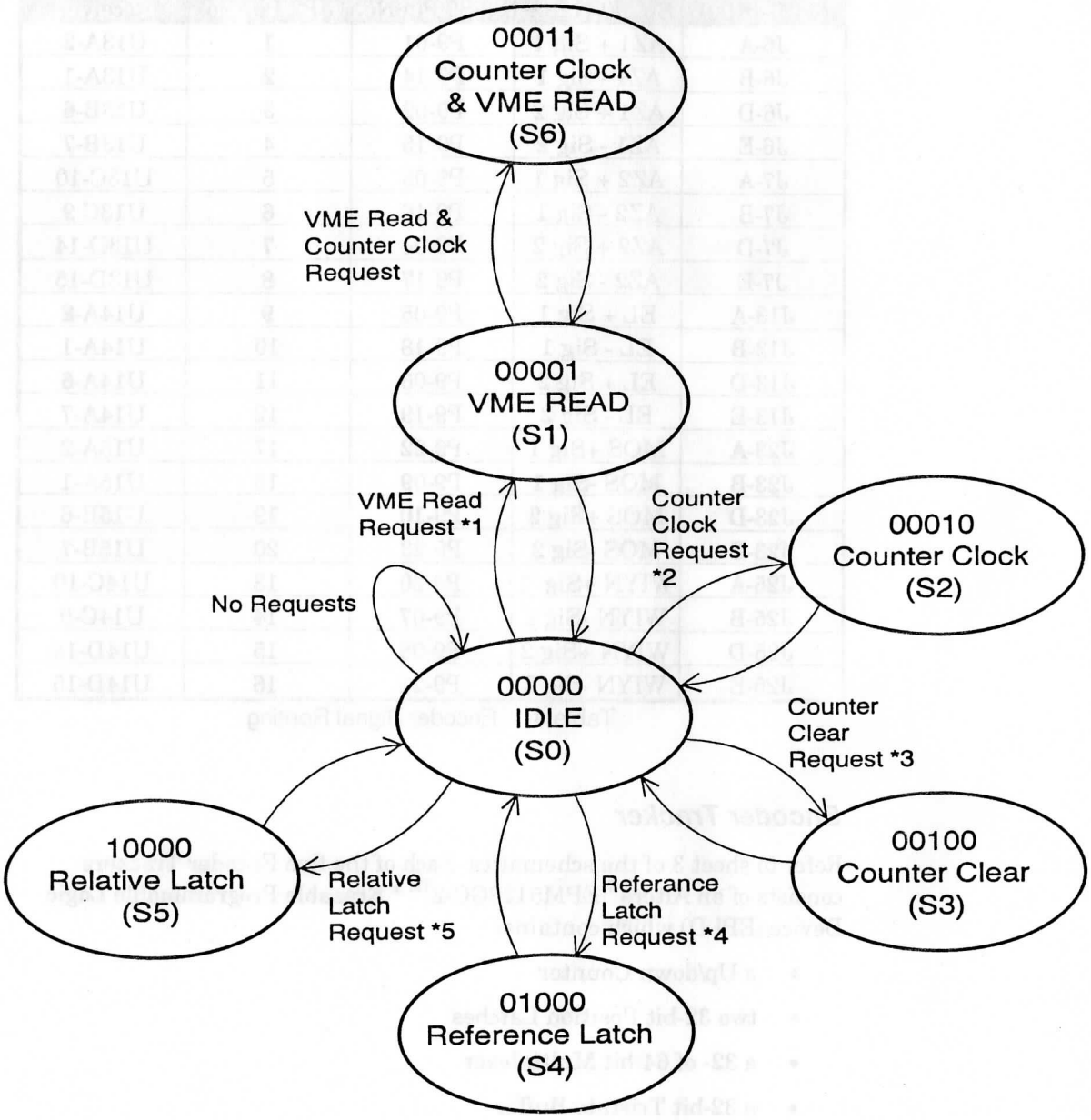
Encoder Tracker

Refer to sheet 3 of the schematics. Each of the five Encoder Trackers consists of an Altera® EPM5128GC-2™ * Erasable Programmable Logic Device (EPLD) which contains:

- a Up/down Counter
- two 32-bit Position Latches
- a 32- of 64-bit Multiplexer
- a 32-bit Tristate Buffer
- an Arbiter

The Encoder Trackers receive encoder position requests from the VME interface, index reference count latching signals from the Index Sensor Interface and, every five milliseconds, a present position latching signal from the Time Signal Generator.

* Altera® is a registered trademark of Altera Corporation
EPM5128GC-2™ is a trademark of Altera Corporation



* In addition to the stated condition, all requests of higher priority must be false for the transition to occur. The priority is noted after the asterisk; 1 is the highest priority

Figure 4-3. Encoder Tracker Arbiter State Diagram

Up/down Counter

Drawing 4421-0107 is a hierarchical set of drawings for the internal logic of the Encoder Tracker. Refer to sheet 1, the top sheet, in the hierarchical drawings. The LS7084 clock and direction outputs (Quadrature Decoder - U8 through U12 on sheet 1 of drawing 4421-0030) drive the 32-bit Up/down Counter's clock and up/down inputs, respectively. The counter can be cleared by a memory mapped decode from the VME interface.

Position Latches

The counter's 32 output bits drive the Present Position and Index Reference Latches. The Present Position Latch is strobed every 5 ms by a 200 Hz clock output of the Time Signal Generator. The Index Reference Latch is strobed when a magnet located on the perimeter of the rotating device passes a stationary index sensor located near the device's perimeter. The latch output enables are driven by memory mapped VME select strobes which also enable the outputs of the tristate buffer onto the external bus.

Multiplexer

A 32- of 64-bit Multiplexer selects the outputs of the Present Position Latch or the output of the Index Reference Latch to drive the 32-bit Tristate Buffer. ABS/5MS drives the Multiplexer's select input. When ABS/5MS is high, the Index Reference Latch is selected; when ABS/5MS is low, the Present Position Latch is selected.

Tristate Buffer

The Tristate Buffer connects the Multiplexer's output to the external VME bus when it is enabled by the OE_ strobe from the Arbiter

Arbiter

The arbiter orchestrates latching signals and requests for latched data. This prevents undefined data resulting from such actions as strobing a latch while the counter's outputs are changing. The Arbiter is described via the Encoder Tracker Arbiter State Diagram shown in Figure 4-3.

Index Sensor Interface

Refer to sheet 2 of the schematics. The magnetic displacement sensors connect to JP3 via the SES Connector Panel. Sensor signals enter the SES connector panel via MS connectors J5, J12, J22 and J24. A cable harness connects to the sensor signal pins on the MS connectors and terminates in plug P10. P10 plugs into J10 on the back of the VME crate; J10 connects to JP3 on the Encoder Interface Board. Table 4-2 on the next page provides sensor signal routing information.

SES Front Panel Connector (4421-0100)	Encoder Signal Name	VME Crate Backpanel Connector P10/S10	Encoder Interface JP2 Pin No.	AMP03 Differential Amplifier
J5-L	AZ Index Out+	P10-01	1	U18-3
J5-M	AZ Index Out-	P10-14	2	U18-2
J12-L	EL Index Out+	P10-03	5	U19-3
J12-M	EL Index Out-	P10-16	6	U19-2
J22-L	MOS Index Out+	P10-07	13	U21-3
J22-M	MOS Index Out-	P10-20	14	U21-2
J24-L	WIYN Index Out+	P10-05	9	U20-3
J24-M	WIYN Index Out-	P10-18	10	U20-2

Table 4-2. Index Sensor Signal Routing

Refer to sheet 2 of the schematics. The Index Sensor Interface consists of four identical channels, one for each sensor input. Therefore, only the Azimuth Index Sensor Interface is described. Each sensor interface consists of:

- Input Filter and AMP03 Differential Amplifier
- Amplifier Output Filter
- Limiter
- Comparator

Input Filter and AMP03 Differential Amplifier

The differential analog input is applied to the AMP03 differential amplifier U18 via a low pass filter consisting of C1 and C2. U18 provides unity gain for the differential analog input.

Amplifier Output Filter and Limiter

U18 drives comparator U16A via a low pass filter and limiter. The filter consisting of R20 and C4 reduces high frequency noise at the input to the comparator.

The limiter, consisting of R20, D1 and D2 limits the negative and positive analog signal peaks to 0 volts and + 5.6 volts, respectively.

Comparator

Comparator U16A has a 2-volt threshold voltage derived from a voltage divider which is driven by a stable REF02 voltage reference. The REF02 reference, located at U17, provides a precision 2.5 VDC input to the voltage divider consisting of R37 and R38. The encoder count is latched into the Index Reference Latch when the positive-going index sensor input to the comparator passes through the 2-volt threshold. A small amount of comparator hysteresis, provided by R22, ensures fast output switching.

The comparator output also sets a bit in the index status latch in the VME interface, indicating a new index reference count is available.

Time Signal Generator

Refer to sheet 4 of drawing 4421-0030. The TTL time reference signals connect to JP1 via a short ribbon cable from the TPRO Time Code Receiver card immediately above the EIM. They drive inputs of the Altera EPM5128GC-2 labeled encoder glue in Figure 4-2. All time signal generator logic is contained in the encoder glue EPLD along with several other functions.

The two inputs from the TPRO time code receiver card are 10 KHz and 1 Hz rates. Both signals have 2 µs wide pulse durations. The Time Signal Generator outputs 50% duty cycle 200 Hz, 1 KHz, and 1 Hz clocks.

The 200 Hz clock is sent to the interrupter which is also part of the glue EPLD, the Encoder Trackers to latch the latest position data, and back to the TPRO Time Code Receiver card. The 1 KHz and 1 Hz go to 26LS31 differential drivers U7AA and U7BB, respectively, which output the signals via JC4. From JC4, the signals drive time signal ports throughout the observatory building via the Serial Opto-isolator (see drawing 4421-0142).

Refer to sheet 1 of drawing 4421-0105 which is the top drawing of a hierarchical set of drawings for the internal logic of the encoder glue EPLD. The Time Signal Generator, labeled *clk-gen* is shown in greater detail on sheet 2 of drawing 4421-0105.

VME Bus Interface

The VME Bus Interface consists of the NIKL interface logic and custom interface logic located in the encoder glue EPLD.

The NIKL is part of a VME Bus Interface and provides a simple interface to the prototyping area of the board. The remainder of the VME interface connects to the simple interface and includes interrupter logic, finer decoding, wait state generation, and index status and interrupt vector registers.

The NIKL is modified to:

- operate as a 32-bit slave
- defeat the "sysfail_" acknowledge
- keep the "PASS" LED illuminated whenever there is power

These modifications are described in the *Encoder Interface Module Prototype BD Modification* drawing 4421-0074. The unmodified NIKL is described in the *Xycom XVME-085 Prototyping Module Manual* which also describes the switch and jumper options. The correct switch and jumper settings for use as an EIM are described in the *Encoder Interface Module Configuration* drawing 4421-0075.

Refer to sheet 4 of drawing 4421-0030. The connector and bus at the top of the sheet labeled NIKL-IF is the simple interface between the NIKL and the prototype area on the board. The NIKL-IF connector consists of a row of wire wrap sockets installed around the perimeter of the NIKL. NIKL signals are available at these sockets.

The encoder glue EPLD contains the prototype-specific interface logic which complements the NIKL-IF logic to form the complete VME Bus Interface. The encoder glue EPLD contains these interface logic functions:

- the remainder of a VME Interrupter
- the remainder of an Address Decoder
- an Index Status Register
- an Interrupt Vector Register
- a Wait State Generator

Refer to sheet 1 of drawing 4421-0105. The memory mapped addresses of these functions can be found in drawing 4421-0034, the *DCC / TCC Environment Specification*.

VME Interrupter

Refer to interrupter text design file drawing, 4421-0105. The interrupter receives the 200 Hz signal from the Time Signal Generator, *clk-gen*, and generates a VME interrupt each clock. The interrupter has a one bit enable register allowing the computer to disable interrupts. BRESET (Bus Reset) clears any pending interrupts when the VME bus is reset.

Address Decoder

Refer to decoder text design file drawing, 4421-0105. The decoder uses the chip select and buffered active low address lines from the NIKL to select the Encoder Tracker, Index Status Register and Interrupt Vector Register hardware. The Encoder Tracker hardware includes the Index Reference Latch, Present Position Latch, and counter reset. The counter resets are executed with an interlocked double write.

The Encoder Interface Module;s responds to a switch selected 1K address block between $FF0000_H$ and $FFFC00_H$ inclusive. Switch sections 6-1 of octal switch SW1 define bits A15 through A10, respectively of the 24-bit base address. A16 - A23 are hard-wired and are all high (binary ones). If necessary, refer to the TCC/DCC Environment Specification (drawing 4421-0034) to determine the assigned base address. The NIKL uses buffered address lines A6 through A9 to decode the 1K base address range into three chip selects labeled CS0_ through CS3_. Table 4-3 defines CS1_ through CS3_ in terms of A6 through A9.

VME Address Bits				
A9	A8	A7	A6	Chip Select
0	0	1	0	CS1_
0	0	1	1	CS2_
0	1	0	0	CS3_
Remaining Permutations of A9 - A6				undefined

Table 4-3. VME Base Address Coding

The Address Decoder portion of the encoder glue logic combines these chip selects with buffered address lines BA5 through BA2, WRSTB_ (WRite STroBe) and WRITL_ (WRITe Latched) to complete the address decode process. Table 4-4 on the next page defines the addresses of the Encoder Interface Module hardware.

Function	Chip Select	Base Address +	Comments
Vector Register	CS1_	80H - BFH	Read/Write
Status Register	CS2_	C0H - FFH	Read Only
Interrupt Enable	CS2_	D8H - DBH	Write Only
Counter Reset Enable	CS2_	DCH - DFH	Write Only
Counter 0 Reset	CS2_	C0H - C3H	Write Only
Counter 1 Reset	CS2_	C4H - C7H	Write Only
Counter 2 Reset	CS2_	C8H - CBH	Write Only
Counter 3 Reset	CS2_	CCH - CFH	Write Only
Counter 4 Reset	CS2_	D0H - D3H	Write Only
Encoder Counter 0	CS3_	100H-103H	Read Present Position
Encoder Counter 0	CS3_	104H-107H	Read Index Position
Encoder Counter 1	CS3_	108H-10BH	Read Present Position
Encoder Counter 1	CS3_	10CH-10FH	Read Index Position
Encoder Counter 2	CS3_	110H-113H	Read Present Position
Encoder Counter 2	CS3_	114H-117H	Read Index Position
Encoder Counter 3	CS3_	118H-11BH	Read Present Position
Encoder Counter 3	CS3_	11CH-11FH	Read Index Position
Encoder Counter 4	CS3_	120H-123H	Read Present Position
Encoder Counter 4	CS3_	124H-127H	Read Index Position

Table 4-4. Encoder Interface Module Memory Map

Index Status Register

Refer to sheet 4 of drawing 4421-0105.2. The Index Status Register is an 8-bit register. It is organized as four 2-bit registers, one pair of bits for each index sensor. During a 32-bit VME bus transfer, the status byte drives the lower eight bits; the upper 24 bits are undefined. The LSB in a pair is set by the output of the respective Index Sensor Interface when passing an index sensor position. This bit is reset when the computer reads the Index Reference Latch in the Encoder Tracker. The MSB of each register pair is the direction bit. It latches the direction of travel at the time the index position was passed. This bit does not reset. If the LSB is not set, the MSB is not valid.

The azimuth axis has two encoders but only one index sensor. Each encoder has its own Position Generator section and Index Reference Latch. Both Azimuth Index Reference Latches are latched when the azimuth index sensor is passed. The azimuth encoders have only one status pair. Reading either latch resets the LSB of the azimuth bit pair.

Interrupt Vector Register

Refer to sheet 3 of drawing 4421-0105.2. The TCC/DCC writes to the 8-bit Interrupt Vector Register during initialization, and reads the register during interrupt acknowledge cycles and normal read cycles.

Wait State Generator

Refer to sheet 1 of drawing 4421-0105.3. When the computer requests data from one of the Encoder Tracker latches, there are arbiter delays, multiplexer propagation delays, tristate buffer delays, and delays in the NIKL buffers before the data gets to the VME bus. The Wait State Generator installs one wait state for a VME bus read of any of the Encoder Tracker latches to ensure that the read data is valid before the computer's read cycle completes.

Chapter 5
Table of Contents

Optics support structure Control Subsystem (OCS) 5-1

Overview 5-2

Functional Description 5-3

Support Subsystems Background 5-3
Thermocoupler 5-3
Secondary Mirror Control Hardware 5-3
Tertiary Mirror Control Hardware 5-5
Counterbalance Mechanism 5-5
Flat Field Lamp Assemblies 5-5
Secondary and Tertiary Mirror Air and Vacuum Control 5-6
Primary Mirror Covers 5-6
STD Bus Boards 5-7
Custom Interfaces 5-9
Thermocoupler Interface 5-9
Secondary Mirror Stepper Motor Interface 5-9
Secondary Mirror Vacuum Support Load Cell Interface 5-11
Secondary Mirror LVDT Interface 5-13
Tertiary Mirror Fold Mechanism Interface 5-15
Tertiary Mirror Vacuum Support Load Cell Interface 5-15
Tertiary Mirror Rotator Interface 5-17
Counterbalance Interface 5-19
Flat Field Lamp Interface 5-21
Vacuum/Air Bag Solenoid Interface 5-23
Mirror Cover Interface 5-25

Detailed Circuit Description 5-27

Thermocoupler Interface 5-24
Secondary Mirror Stepper Motor Interface 5-29
Stepper Motors 5-29
Stepper Motor Controllers 5-29
Controller Input Power Control 5-29
Sensor Switches 5-29
Secondary Mirror Vacuum Support Load Cell Interface 5-29
Load Cells 5-29

Load Cell Preamplifiers 5-29
Secondary Mirror LVDT Interface 5-31
Linear Voltage Differential Transformers LVDTs) 5-31
Power Supply 5-31
Power Supply Control Relay 5-31
Tertiary Mirror Fold Mechanism Interface 5-32
Flip Actuator 5-32
Motor Direction Control 5-32
Motor Power Supply 5-32
Control Logic 5-32
Status Switches 5-33
Tertiary Mirror Vacuum Support Load Cell Interface 5-34
Tertiary Mirror Rotator Interface 5-35
Rotator Motor 5-35
Motor Speed Control Logic 5-35
Speed/Direction Control 5-37
OCS Logic Board (partial) 5-38
Power Control Relay 5-39
Latch Pin Solenoid 5-39
Latch Pin Solenoid Control 5-39
Latch Pin Status 5-39
Counterbalance Interface 5-40
120 VAC Counterbalance Drive Motor 5-40
Motor Direction Control 5-40
Limit Switch Selector Relays 5-40
Forward and Reverse Limit Switches 5-41
Position Sensor 5-41
Brake Air Solenoid Valve 5-41
Brake Solenoid Control 5-41
Flat Field Lamp Interface 5-42
Programmable Power Supplies 1 and 2 5-42
200 and 100 Watt Lamp Assemblies 5-42
Digital-to-Analog Board 5-42
Parallel Interface Board (partial) 5-42
Vacuum/Air Bag Solenoid Interface 5-43
Vacuum and Air Solenoids 5-43
Power Relays 5-43
Control Relays and the Parallel Interface Board 5-43
Power Supply 5-43
Mirror Cover Interface 5-44
Cover Drive Motor 5-44
Motor Direction Control 5-44
Motor Power Supply 5-46
Status Switches 5-46
Circuit Board Configuration 5-46

Figures

Figure 5-1. OCS Functional Block Diagram 5-4
Figure 5-2. Secondary Mirror Stepper Motor Interface Block Diagram. 5-8
Figure 5-3. Secondary Mirror Vacuum Support Load Cell Interface Block Diagram. 5-10
Figure 5-4. Secondary Mirror LVDT Interface Block Diagram. 5-12
Figure 5-5. Tertiary Mirror Fold Mechanism Interface Block Diagram. 5-14
Figure 5-6. Tertiary Mirror Rotator Interface Block Diagram 5-16
Figure 5-7. Counterbalance Interface Block Diagram. 5-18
Figure 5-8. Flat Field Lamp Interface Block Diagram 5-20
Figure 5-9. Vacuum/Air Bag Solenoid Interface Block Diagram 5-22
Figure 5-10. Mirror Cover Interface Block Diagram 5-24
Figure 5-11. OCS Logic Board Conceptual Logic Diagram 5-47

Tables

Table 5-1. OCS STD Bus Boards 5-7
Table 5-2. Stepper Motor Responses 5-29
Table 5-3. Rotator Control Signal Truth Table 5-39
Table 5-4. Mirror Cover Opening Logic Truth Table. 5-45
Table 5-5. Mirror Cover Closing Logic Truth Table 5-45

Optics support structure Control Subsystem (OCS)

The Optics support structure Control Subsystem (OCS) consists of a three-drawer enclosure attached to the telescope. The drawers contain relays, power supplies, circuit boards and a 13-slot STD card cage containing seven STD bus boards. One of these boards is a CPU board which controls the remainder of the OCS in response to commands from the Telescope Control/Device Control Computer (TCC/DCC).

The OCS is a mix of commercial and custom hardware which controls several telescope optics support subsystems. The commercial hardware is documented by its manufacturer and no attempt is made here to duplicate or expand on that documentation. This chapter documents the custom hardware and consists of these sections:

- Overview
- Functional Description
- Detailed Circuit Description
- Circuit Board Configuration

The Overview introduces the various telescope optics support subsystems which make up the OCS. The Functional Description describes the telescope optics support subsystems in terms of control requirements. It also describes the functions of the STD bus boards and the 11 custom interfaces between those boards and the telescope optics support subsystems. The Detailed Circuit Description describes the custom interfaces in detail; the Circuit Board Configuration section provides detailed configuration information for the STD bus boards.

Overview

The OCS is connected to the Telescope Control/Device Control Computer (TCC/DCC) via a serial data link and performs actions only when commanded to do so by the TCC/DCC. Subsystem Status is routed to the Engineering Data System (EDS).

The OCS performs functions which control:

- Telescope temperature acquisition
- Secondary Mirror focusing
- Tertiary Mirror rotating
- Tertiary Mirror folding
- Telescope Counterbalance positioning
- Flat Field Lamp intensity
- Secondary and Tertiary Mirror Air Bags control
- Primary Mirror Cover positioning

The CPU board provides overall control of these telescope functions in response to commands from the TCC/DCC. The remaining OCS enclosure hardware acts as an interface between the CPU board and the subsystems listed above. The output section of this interface controls various motors, air and vacuum solenoids and intensity calibration lamps; the input section of this interface provides device position, limit switch status, telemetry and telescope temperature inputs to the CPU board.

Functional Description

Figure 5-1 on the next page is a functional block diagram of the OCS. Refer to it throughout this description. The Functional Description is organized into these sections:

- Support Subsystems Background
- STD Bus Boards
- Custom Interfaces

Support Subsystems Background

The telescope hardware controlled by the OCS includes the:

- Thermocoupler
- Secondary Mirror Control Hardware
- Tertiary Mirror Control Hardware
- Counterbalance Mechanism
- Flat Field Lamp Assemblies
- Secondary and Tertiary Mirror Air and Vacuum Control
- Mirror Cover Hardware

Thermocoupler

The Thermocoupler, a microprocessor based controller located in a small enclosure mounted on the top of the OCS cabinet, monitors sixteen thermocouple temperature sensors mounted at various locations on the telescope. An RS-485 interface links the Thermocoupler to the OCS CPU board via a STD Bus serial communications adapter board. The CPU board issues commands to the Thermocoupler, telling it which sensors to monitor. The Thermocoupler converts requested sensor voltages to digital Celsius values and outputs them upon request to the CPU board.

Secondary Mirror Control Hardware

The Secondary Mirror is mounted in a cell (see page 5-6) and suspended from the Secondary Support Truss facing down toward the Primary Mirror. The cell and mirror assembly is connected to the truss via three linear actuators which attach to the back of the cell in a triangular pattern. Telescope focusing is accomplished by positioning this mirror via the linear actuators.

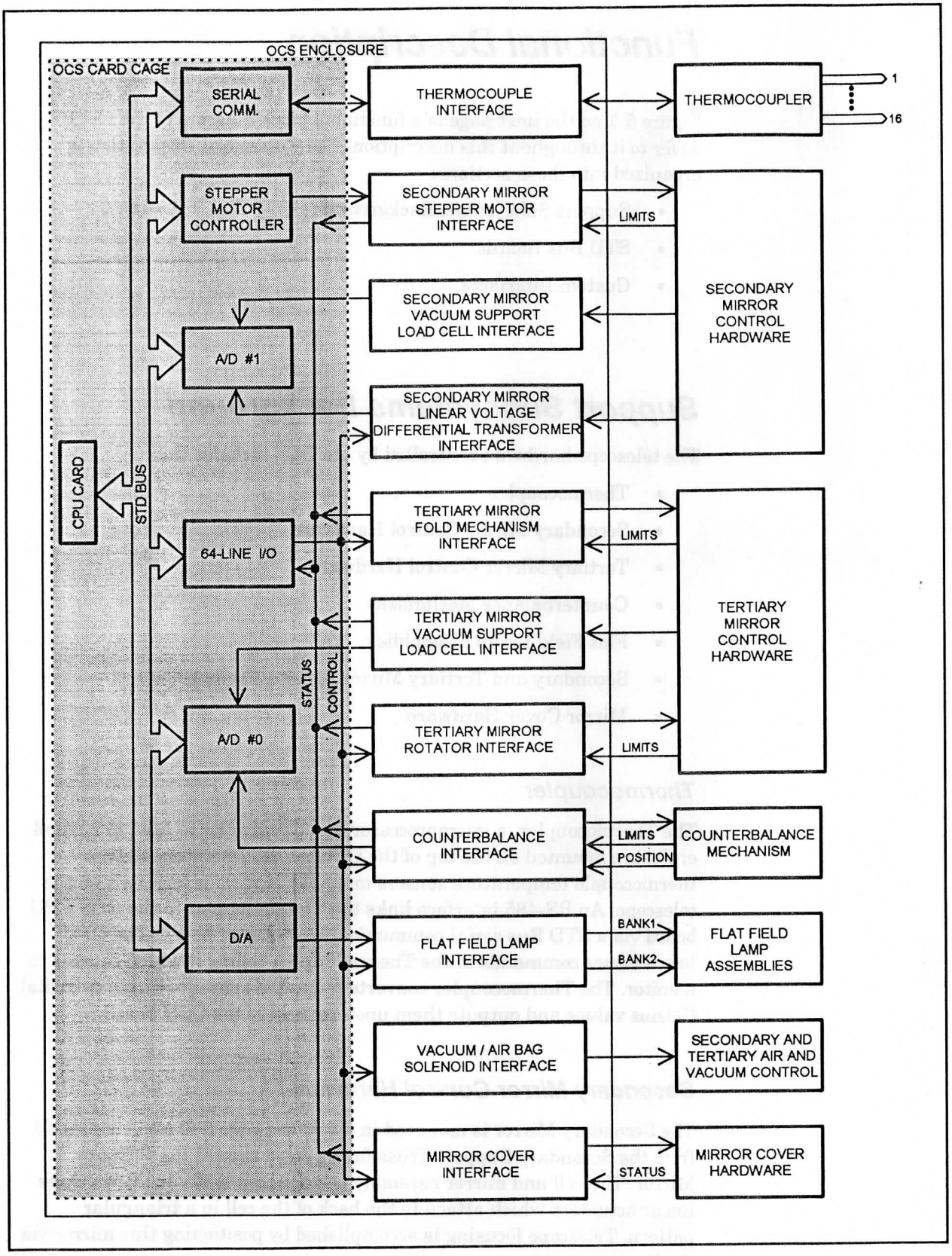


Figure 5-1. OCS Functional Block Diagram

Tertiary Mirror Control Hardware

The Tertiary Mirror, located between the Primary and Secondary Mirrors, is oriented at 45° with respect to the telescope's Z_0 axis. Refer to the Secondary and Tertiary Mirror Air and Vacuum Control description on page 5-6 for mirror mounting information.

The Tertiary Mirror directs the light beam to the Nasmyth (WIYN and MOS NIRs) and bent Cassegrain instrument ports. The OCS rotates the Tertiary Mirror about the telescope's Z_0 axis to direct the beam to the MOS or WIYN NIR port. The Cassegrain port is behind the opening in the center of the primary mirror. The Tertiary Mirror must be folded up out of the beam's path to allow it to pass undeflected to the Cassegrain port. A latch pin mechanism ensures the Tertiary mirror is properly aligned at each port position. Position sensor switches indicate location.

Three load cells mounted between the mirror and its cell sense the difference between the force exerted by the applied vacuum or air and the mirror's weight. The CPU reads the load cell outputs to balance these forces by enabling air or vacuum solenoid valves.

Counterbalance Mechanism

Two powered counterweights provide the fine balance function of the Optical Support Structure about the elevation axis. When the telescope is properly balanced, the Elevation Servo needs only to overcome friction and inertia during telescope elevation changes, regardless of the direction of that change. If the telescope is unbalanced, the Elevation Servo must also overcome the forces of gravity on the unbalanced mass of the telescope. This can result in substantial servo drive currents during tracking.

The OCS controls motors which position the two counterweights. The counterweights operate independently but provide the same function of balancing the telescope about the elevation axis.

Flat Field Lamp Assemblies

A 200-watt and a 100-watt lamp assembly are mounted on the Optical Support Structure such that they can project a flat field illumination on a screen mounted inside the dome. This screen can be observed by the telescope for calibration purposes.

Secondary and Tertiary Mirror Air and Vacuum Control

The Secondary and Tertiary mirrors, because of their size, shape and mass, can flex under their own weight. The flexing causes distortion in the observed images. The mirror flex can be eliminated if a uniform pressure is applied to the underside of the mirror producing an upward force equal to the mirror's weight.

The mirrors are mounted in air-tight enclosures called cells. The perimeter of the mirror is sealed to the perimeter of the cell, forming an air-tight enclosure behind the mirror. For a downward-pointing mirror, such as the Secondary Mirror, a partial vacuum is created in the chamber allowing atmospheric pressure to provide a uniform upward pressure on the mirror. For an upward-pointing mirror, air pressure is applied to the chamber, creating an upward force on the underside of the mirror. If a mirror such as the Tertiary Mirror is sometimes upward-pointing and at other times downward-pointing, air pressure must be applied when it is pointing up and vacuum must be applied when it is pointing down. While the Secondary Mirror is technically a downward-pointing mirror whenever the telescope elevation is above zero degrees, air or vacuum can be ported to the Secondary Mirror as well as the Tertiary Mirror.

Primary Mirror Covers

The Mirror Covers are in front of the Primary Mirror and protect it from dust and falling objects. Two accordion style covers are required. The Mirror Cover Interface section of the OCS controls the cover positioning motors in response to inputs from the CPU board.

STD Bus Boards

The commercial STD bus boards associated with the CPU board expand the I/O capability of the CPU board. Collectively, they equip the CPU with these functions:

- four configurable RS-232/422/485 serial I/O ports (only one serial I/O port is used and it is configured as an RS-422 type)
- three Stepper Motor Control channels (controls Secondary Mirror positioning)
- sixteen 12-bit Analog-to-Digital (A/D) channels with differential inputs (11 channels are used)
- four 12-bit Digital-to-Analog (D/A) channels (two are used)
- 64 parallel I/O lines are configurable as inputs or outputs in blocks of eight lines (22 of 32 input lines are used and 30 of 32 output lines are used)

The boards are located in the 13-slot STD card cage in the top drawer of the OCS enclosure. The card cage has vertical slots numbered 1 through 13, with slot 1 at the left. Table 5-1 below describes the boards located in the card cage.

Slot	Manufacturer	Model	Description
1	Pro-Log	7342-3	Stepper Motor Controller
2			
3	WinSystems, Inc.	LPM-SBC40A	Single Board Computer
4			
5	WinSystems, Inc.	LPM-COM4	Serial Communications
6			
7	WinSystems, Inc.	LPM-A/D12M	Analog-to-Digital (A/D)
8			
9	WinSystems, Inc.	LPM-7614	Parallel Interface Board
10	WinSystems, Inc.	LPM-A/D12M	Analog-to-Digital (A/D)
11			
12	WinSystems, Inc.	LPM-D/A-4-DC	Digital-to-Analog (D/A)
13			

Table 5-1. OCS STD Bus Boards

Each telescope support subsystem requires one or more custom interfaces in addition to one or more functions provided by the STD bus boards.

Hereafter, the Pro-Log 7342-3 is referred to as the Stepper Motor Controller, the LPM-SBC40A is referred to as the CPU board, the LPM-COM4 is referred to as the COM-4 board, the LPM-A/D12M in slot 7 is referred to as the A/D 0 board, the LPM-7614 is referred to as the Parallel Interface board, the LPM-A/D12M in slot 10 is referred to as the A/D 1 board and the LPM-D/A-4-DC is referred to as the D/A board.

The Stepper Motor Interface is currently being redesigned. No functional block diagram was available at the time of this printing.

Figure 5-2. Secondary Mirror Stepper Motor Interface Block Diagram

Custom Interfaces

Custom interfaces adapt the seven OCS subsystems to one or more of the STD Bus boards described in Table 5-1 on page 5-7. Figure 5-1 on page 5-4 shows the custom interfaces as unshaded blocks in the OCS ENCLOSURE outline.

The custom interfaces are:

- Thermocoupler Interface
- Secondary Mirror Stepper Motor Interface
- Secondary Mirror Vacuum Support Load Cell Interface
- Secondary Mirror LVDT Interface
- Tertiary Mirror Fold Mechanism Interface
- Tertiary Mirror Vacuum Support Load Cell Interface
- Tertiary Mirror Rotator Interface
- Counterbalance Interface
- Flat Field Lamp Interface
- Vacuum/Air Bag Solenoid Interface
- Mirror Cover Interface

Thermocoupler Interface

The Thermocoupler is a microprocessor-based temperature monitor which senses temperature at 16 locations on the telescope. This monitor is connected to the COM-4 board via the Thermocoupler Interface. The interface consists of a commercial, low-power, 5-volt DC power supply which provides all the Thermocoupler's power requirements. The remainder of the interface consists of a straight-through RS-485 serial communications connection between the Thermocoupler and the COM-4 board.

Secondary Mirror Stepper Motor Interface

Figure 5-2 is the block diagram of the Secondary Mirror Stepper Motor Interface. The stepper motors shown in Figure 5-2 drive the three linear actuators used to position the secondary mirror. Each motor receives drive power from a respective Stepper Motor Driver module. The three drivers receive Step and Direction control inputs from the Stepper Motor Controller. Motor drive power is supplied to the drivers by the Motor Power Control block whose output is enabled by a control output from the Parallel Interface board. Two limit switches for each actuator provide the CPU board with position status via the Parallel Interface board.

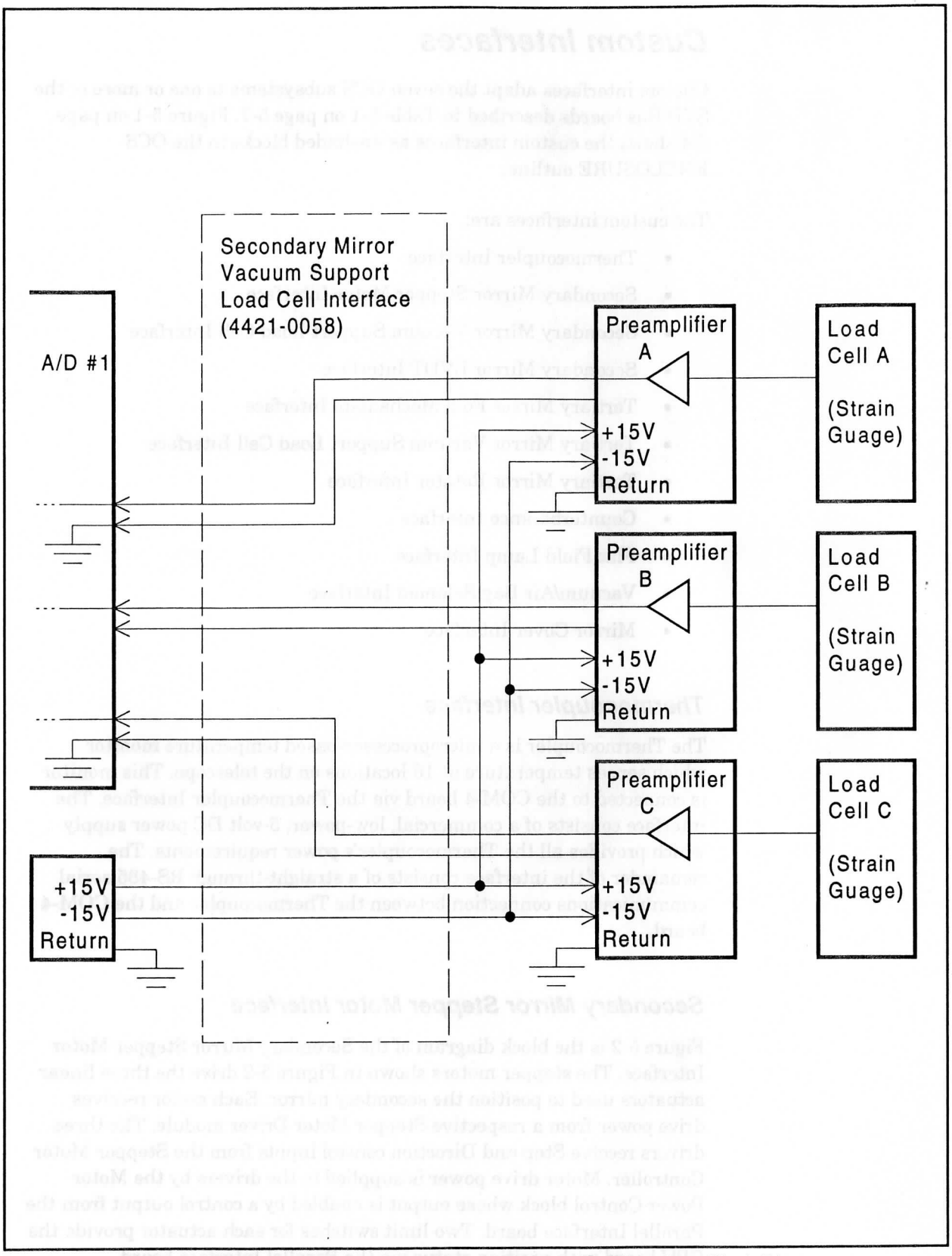


Figure 5-3. Secondary Mirror Vacuum Support Load Cell Interface Block Diagram

Secondary Mirror Vacuum Support Load Cell Interface

Vacuum or air pressure is applied between the Secondary Mirror and its support cell. Three load cells arranged in a triangular pattern are connected between the mirror and its cell. The load cells sense the imbalance between the applied vacuum and the force of gravity on the face of the mirror. The CPU board monitors the cell outputs to determine changes in the applied vacuum. The applied vacuum goes from zero to maximum as the telescope's elevation goes from 0° to 90°.

Figure 5-3 is the Functional Block Diagram of the Secondary Vacuum Support Load Cell Interface which consists of cabling and three preamplifier boards.

The three load cell outputs are amplified by three preamplifier boards which are located in an enclosure mounted a few inches from the Secondary Mirror on its support truss. These preamplifiers receive DC power from the STD Bus board cage's backplane.

Each preamplifier's analog output is converted to digital by A/D 1.

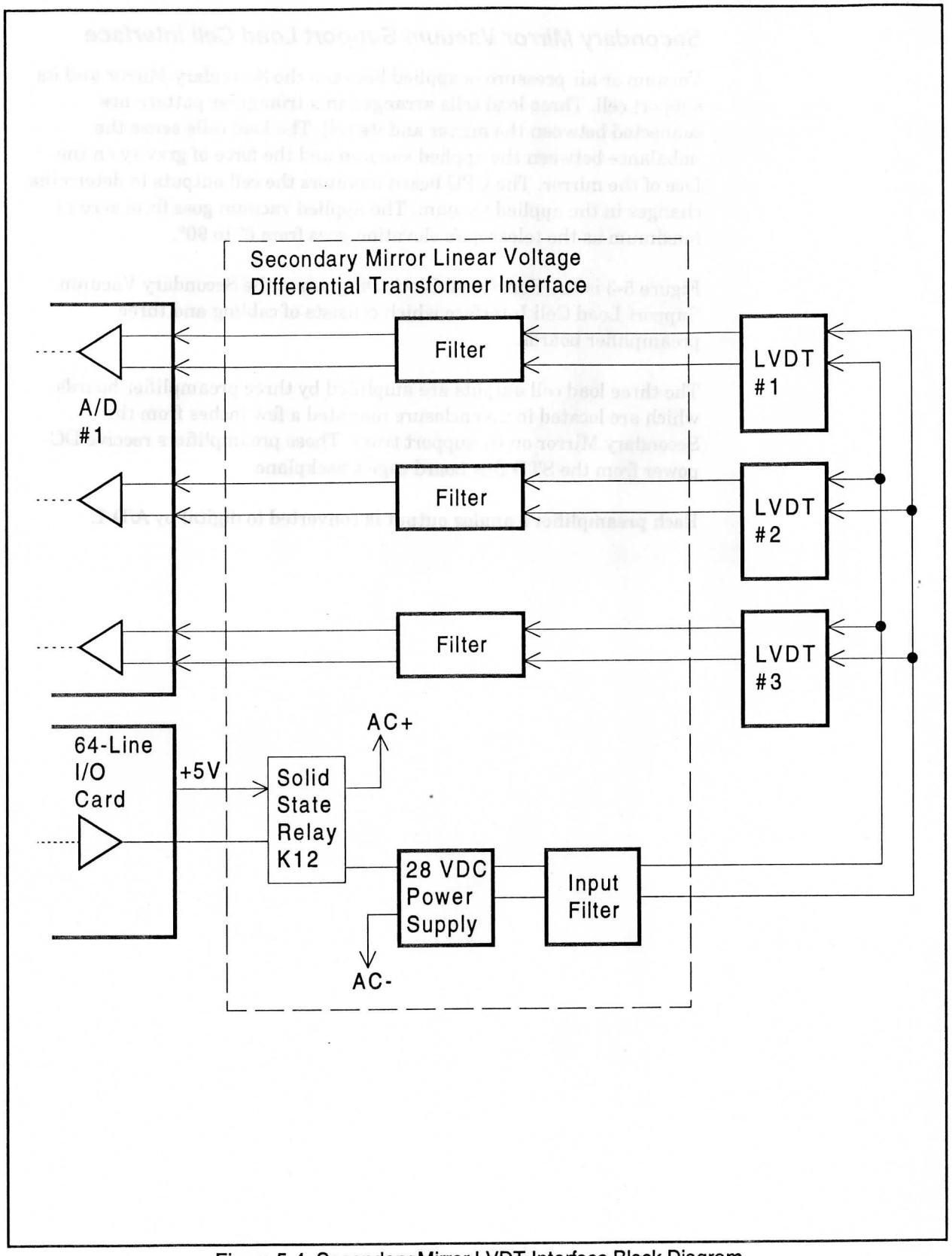


Figure 5-4. Secondary Mirror LVDT Interface Block Diagram

Secondary Mirror LVDT Interface

Secondary Mirror position is sensed by three Linear Voltage Differential Transformers (LVDT). These devices consist of a movable-core transformer driven by an oscillator. The transformer has two output windings which have induced voltages proportional to the position of the core. The windings drive a demodulator which produces a DC output voltage proportional to the difference between the two winding outputs. The LVDT outputs are converted to digital by A/D 1.

Figure 5-4 is the Secondary Mirror LVDT Interface Block Diagram. It shows that the interface consists of a DC power supply and low-pass filters. The power supply provides power for the LVDT oscillators; the filters prevent the high frequency oscillator frequencies from reaching the A/D inputs.

The power supply is powered by 115 VAC and controlled by an input from the Parallel Interface board.

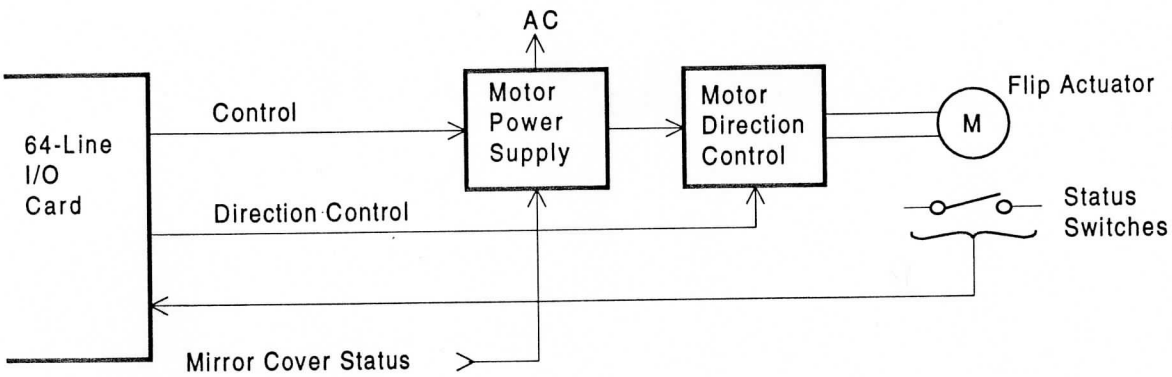


Figure 5-5. Tertiary Mirror Fold Mechanism Interface Block Diagram

Tertiary Mirror Fold Mechanism Interface

The telescope's three observation ports are the WIYN NIR, MOS NIR and Cassegrain. The Tertiary Mirror position determines port usage. The Cassegrain port is used by folding the Tertiary Mirror back out of the light beam; the NIR ports are available when the Tertiary Mirror is folded into the light beam. When the mirror is folded in, it can be rotated to the WIYN or MOS NIR port positions (see the Tertiary Mirror Rotator Interface description).

Figure 5-5 is the block diagram of the Tertiary Mirror Fold Mechanism Interface. It consists of:

- Motor Power Supply
- Motor Direction Control
- Status Switches

The Tertiary Mirror is folded in and out by a DC motor called the Flip Actuator. It is powered by the Motor Power Supply via the Motor Direction Control block which can reverse the direction of current flow through the motor.

The Tertiary Mirror fold mechanism extends through the Primary Mirror Covers. When the covers are in place, the Mirror Cover position status inhibits the Motor Power Supply. Thus, the Primary Mirror Covers must be retracted to allow folding.

Limit switches provide Tertiary Mirror position to the CPU board via the Parallel Interface board.

Tertiary Mirror Vacuum Support Load Cell Interface

The Tertiary Mirror Vacuum Support Load Cell Interface is identical functionally and electrically to the Secondary Mirror Vacuum Support Load Cell Interface described on page 5-11. However, the preamplifier outputs drive input channels on the A/D 0 board instead of the A/D 1 board.

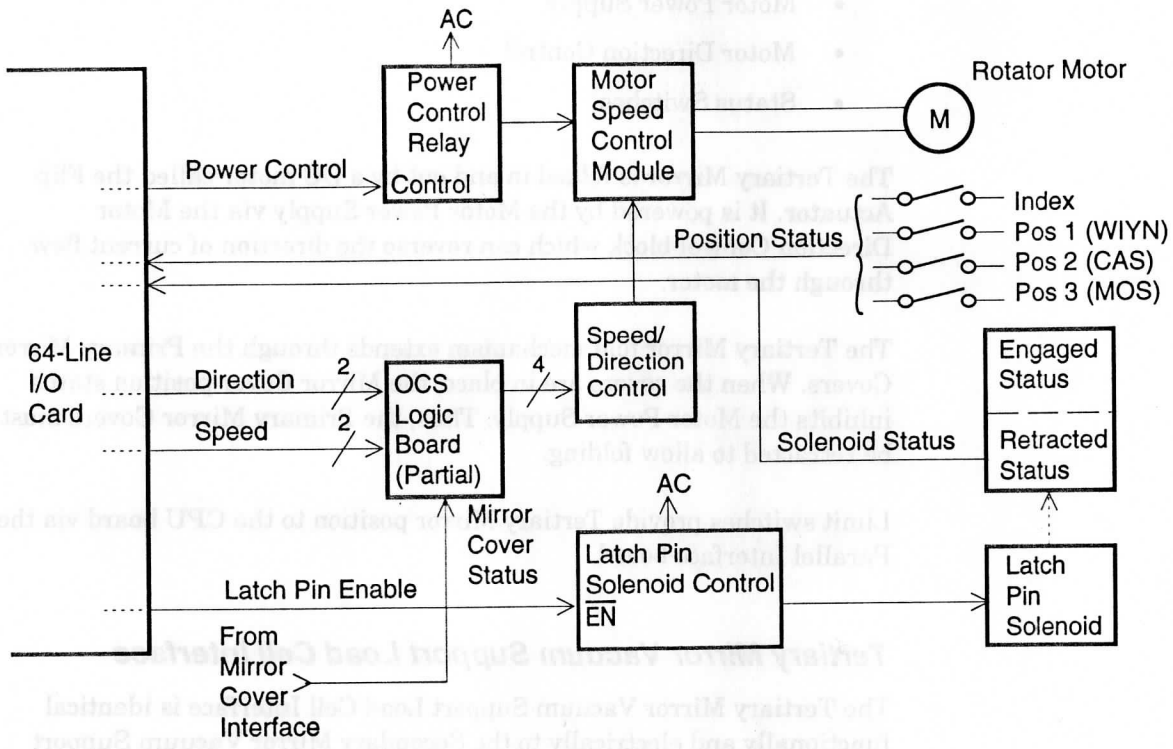


Figure 5-6. Tertiary Mirror Rotator Interface Block Diagram

Tertiary Mirror Rotator Interface

The Tertiary Mirror Rotator Interface controls the rotation of the Tertiary Mirror about the telescope's Z_0 axis. A DC motor drives the mirror to one of these positions:

- WIYN NIR (WIYN)
- Cassegrain (CAS)
- MOS NIR (MOS)

Refer to Figure 5-6, the Tertiary Mirror Rotator Interface Functional Block Diagram. The motor is powered by a regenerative motor speed controller which is powered by 115 VAC via a power control relay. The relay is controlled via an input from the Parallel Interface board.

The regenerative motor speed controller provides positive motor speed control under all conditions within the limits of the motor and controller (true four-quadrant control). Thus, the controller allows the motor to rapidly decelerate the mirror as it approaches the commanded position by returning power to the AC supply.

The Speed/Direction Control block provides a high and low analog speed for both the forward and reverse directions. It receives speed and direction selection inputs from the OCS Logic Board.

The OCS Logic Board gates speed and direction selection inputs from the Parallel Interface board with Primary Mirror Cover status. The Primary Mirror Covers must be retracted because the Tertiary Rotator mechanism extends below the surface of the covers and would strike them if it was rotated with the covers closed (see the Mirror Cover Interface description).

A spring-loaded, pneumatically-retracted Index Pin ensures precise mirror positioning at each port position (WIYN, CAS or MOS). Before the mirror can be moved to a new position, the Index pin must be retracted by applying air pressure to the pin mechanism via an air solenoid valve. The 115 VAC operated valve receives power via the Latch Pin Solenoid Control block. Power to the valve is controlled by an enable signal from the Parallel Interface board. No hardware in the Tertiary Mirror Rotator Interface prevents power application to the rotator motor when the latch pin is engaged. This function is accomplished in software since the Latch Pin's status is available to the CPU board via the Parallel Interface board.

Four normally-closed switches provide position information to the CPU board via the Parallel Interface board. The INDEX switch opens at each port position (WIYN, CAS and MOS). The POS 1, POS 2 and POS 3 switches open only at the WIYN, CAS or MOS ports, respectively. Thus, at each port position, two switches are open, the INDEX switch and the respective port switch.

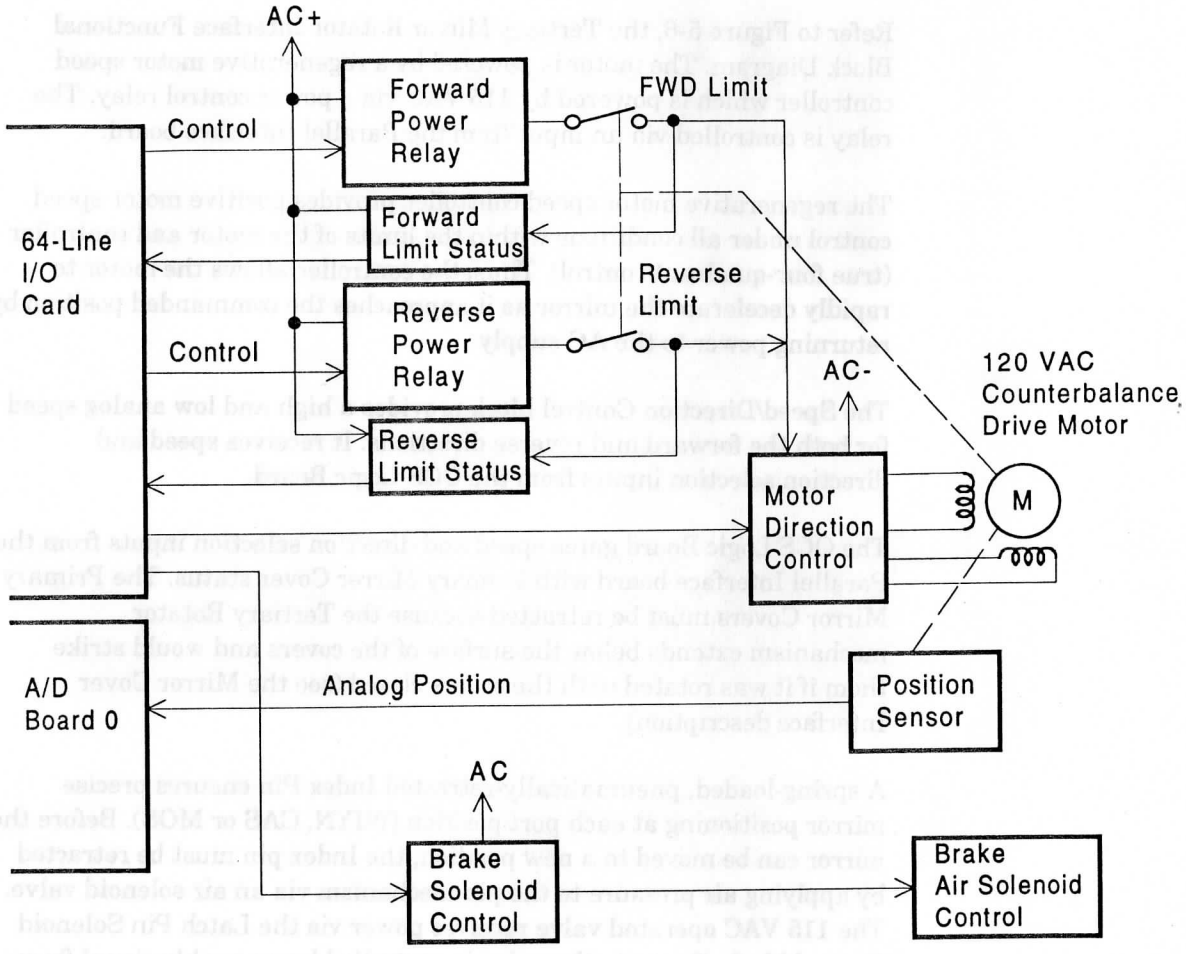


Figure 5-7. Counterbalance Interface Block Diagram

A typical sequence of events for moving the mirror after the Mirror Covers are retracted is:

1. Retract the Index Pin.
2. Select HIGH speed and FORWARD or REVERSE direction.
3. Select SLOW speed as the mirror approaches the desired position.
4. Stop the mirror at the desired position.
5. Engage the Index Pin. As the chamfered Index Pin engages, the mirror is precisely aligned to the desired port.

Do not release the Latch Pin while the mirror is moving because the pin can be damaged or destroyed if it drops into the engaged position while the mirror is moving.

Counterbalance Interface

Figure 5-7 is a functional block diagram of the Counterbalance Interface. Two counterbalance mechanisms operate independently but provide the same function of balancing the telescope about the elevation axis. Figure 5-7 shows the interface for one counterbalance; the interface for the other counterbalance is identical.

The counterbalance is positioned by an AC induction motor. The Motor Direction Control performs field winding switching to reverse motor direction. Switching, and therefore motor direction, is controlled by the Direction control input from the Parallel Interface board.

Power is supplied to the Motor Direction Control via the Forward or Reverse Power Relay and normally-closed (NC) Forward or Reverse Limit Switch, respectively. Each relay via its associated limit switch provides AC power to the Motor Direction Control. The relays have no effect on motor direction. That function is controlled by the Motor Direction Control as described above. The purpose of the relays and limit switches is to automatically disconnect power from the motor by opening the associated limit switch if the counterbalance runs into an end stop.

Counterbalance position is sensed by an analog sensor which provides an input to the A/D 0 board. A/D 0 converts the position input to digital which is periodically read by the CPU board.

The Counterbalance mechanism is equipped with a brake which holds the counterbalance in position when motor power is removed. The brake is spring loaded and uses air pressure to retract it. Brake retraction air pressure is supplied to the brake via an air solenoid valve. Power to the valve is controlled by an output from the Parallel Interface board.

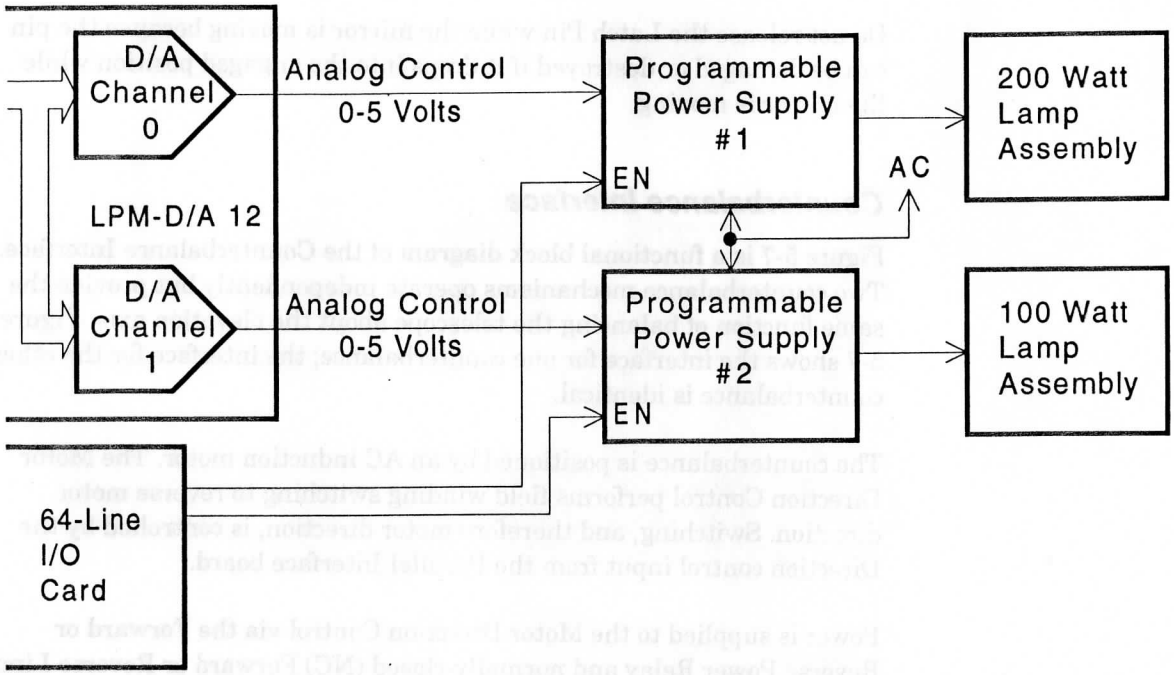


Figure 5-8. Flat Field Lamp Interface Block Diagram

Flat Field Lamp Interface

Figure 5-8 is a functional block diagram of the Flat Field Lamp Interface. The Flat Field Lamp Interface powers a 200 watt and a 100 watt Flat Field Lamp Assembly. Each assembly requires 48 VDC to develop rated intensity. Each assembly is driven by a Programmable Power Supply which is controlled by a 0 - 5 VDC analog input. The power supplies are enabled by control outputs from the Parallel Interface board. Channels 0 and 1 on the D/A board provide the Analog Control inputs to the Programmable Power Supplies.

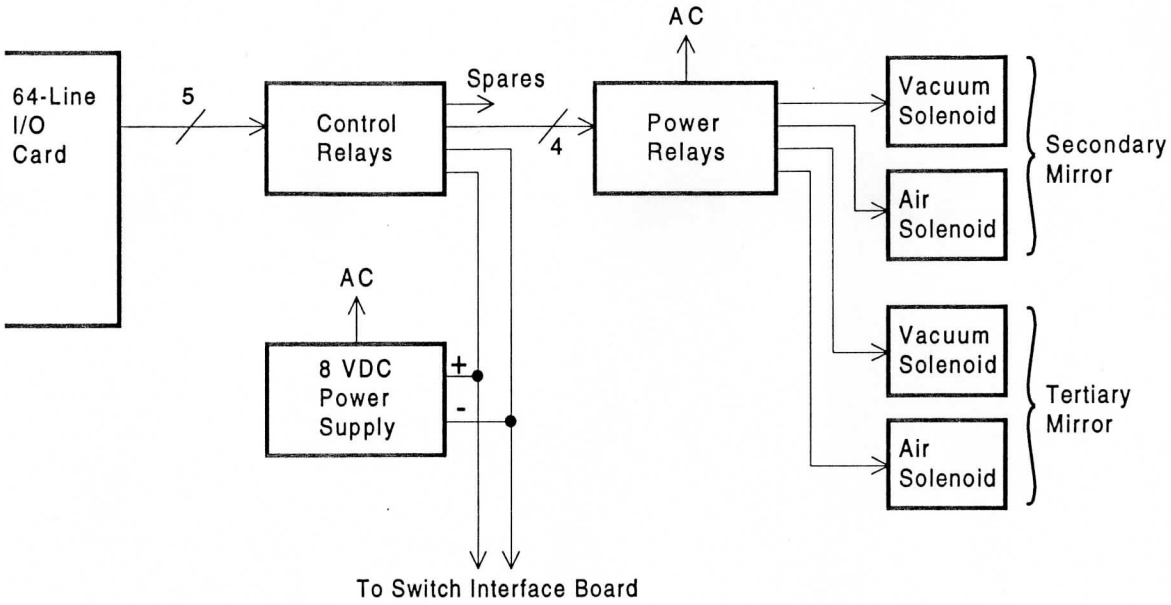


Figure 5-9. Vacuum/Air Bag Solenoid Interface Block Diagram

Vacuum/Air Bag Solenoid Interface

The Secondary and Tertiary Mirrors use air pressure or vacuum to support the weight of the respective mirror. Air pressure or vacuum can be ported to either mirror cell via solenoid valves which require 115 VAC power to open.

Refer to Figure 5-9, the Vacuum/Air Bag Solenoid Interface Block Diagram. The Power Relays block applies AC power to each solenoid valve via individual solid-state power relays. These relays are enabled by control signals from the Control Relays block.

The Control Relays provide high isolation between control inputs from the Parallel Interface board and the Power Relays block which provides the Parallel Interface board with transient voltage protection.

The Control Relays block requires a DC voltage to develop its output signals. The 8 VDC Power Supply provides DC power for the Control Relays and Switch Interface Board (SIB - not shown) which interfaces all OCS sensor switches to the I/O board.

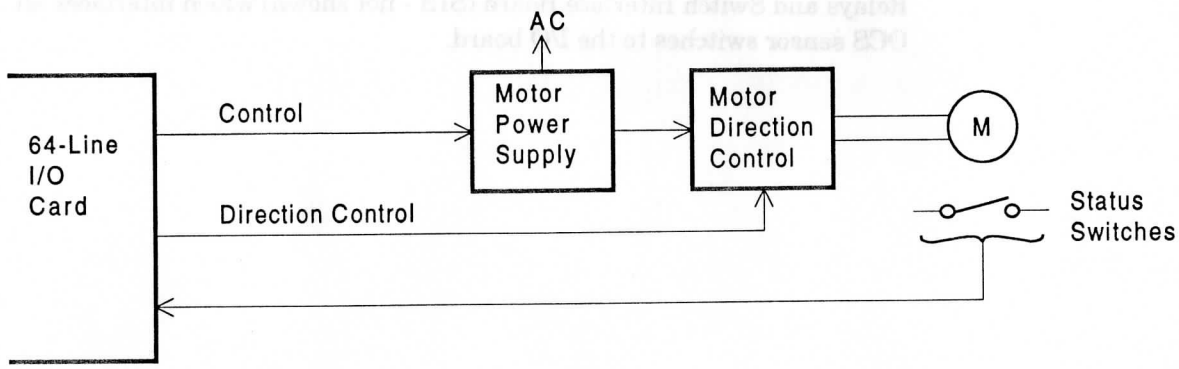


Figure 5-10. Mirror Cover Interface Block Diagram

Mirror Cover Interface

The Primary Mirror is protected by two accordion-style mirror cover halves called the Right Mirror Cover and Left Mirror Cover. In the closed position, the two covers meet above the center of the Primary Mirror.

The Tertiary Mirror Rotator mechanism extends above the mirror cover. Two thin metal bars extend between the mirror cover halves to support the upper portion of the rotator. When the mirror covers close, the rubber sealing gaskets on the edges of the mirror covers squeeze around the metal bars. The Tertiary Mirror must be in one of the NIR positions to allow the mirror covers to close.

The covers are positioned by identical controllers which are interfaced to the CPU board via the Parallel Interface board. Figure 5-10 is a functional block diagram of the left or right Mirror Cover Interface.

The Left Mirror Cover is positioned by a DC motor via the Motor Direction Control block which can reverse the direction of current flow through the motor in response to the Direction Control input from the Parallel Interface board. Motor power is provided by the Motor Power Supply which is enabled by a control signal from the Parallel Interface board.

Mirror Cover position status for each cover half is provided by two sensor switches (a total of four switches for the two cover halves). One switch opens when the respective cover is fully open; the other switch opens when the respective cover is fully closed.

Detailed Circuit Description

This description discusses the circuits of each block shown in the interface functional block diagrams (Figures 5-2 through 5-10).

Much of the OCS custom interface logic circuitry is mounted on the OCS Logic Board, a wirewrap board located in the upper drawer of the OCS enclosure. The logic on this board consists of two Programmable Array Logic (PAL) ICs and an octal line driver IC. Drawing 4421-XXXX in the *WIYN Drawings* binder (see *Appendix A*) is the schematic for the OCS Logic Board; Figure 5-11 on page 5-47 is an equivalent logic form of the PAL equations. All OCS sensor switches are interfaced to the OCS logic via two Switch Interface Boards (SIBs) which are located beside the OCS Logic Board.

Discrete resistors, capacitors and transistors are referenced by R, C and A designators, respectively. Decimal points (.) in resistor and capacitor values are replaced by K and u, respectively, to prevent misinterpretation of a component's value due to overlooking a decimal point. For example, a 4990 ohm resistor is shown as 4K99 (4.99K ohms); a 0.1μ capacitor is shown as u1.

Signal names are in uppercase letters and numbers, e.g., NPM. Names with an overscore or trailing or back slash represent an active low signal, e.g., $\overline{\text{WNE}}$, WNE/ or WNE\. All logic states are described as high and low. An *asserted* logic signal is a signal in its active state.

All OCS power is derived from 115 VAC UPS power (see drawing 4421-0070) which enters the OCS enclosure on J23 (lower drawer, front panel, lower-right connector). J23 connects to a six-screw terminal strip in each drawer (see drawings 4421-0093 through 4421-0095).

These OCS interfaces are described in this Detailed Circuit Description:

- Thermocoupler Interface
- Secondary Mirror Stepper Motor Interface
- Secondary Mirror Vacuum Support Load Cell Interface
- Secondary Mirror LVDT Interface
- Tertiary Mirror Fold Mechanism Interface
- Tertiary Mirror Vacuum Support Load Cell Interface
- Tertiary Mirror Rotator Interface
- Counterbalance Interface
- Flat Field Lamp Interface
- Vacuum/Air Bag Solenoid Interface
- Mirror Cover Interface

Thermocoupler Interface

The Thermocoupler Interface is shown on drawing 4421-0065. It consists of the Acopian 5EB250 power supply mounted in the top drawer of the OCS enclosure. The power supply's AC input is wired into terminal strip TS1.

The remainder of the interface consists of cabling between the Thermocoupler and the COM-4 board. Power and communications are routed to the Thermocoupler via a single multi-conductor cable connected to J6.

Secondary Mirror Stepper Motor Interface

The Secondary Mirror Stepper Motor Interface is shown on drawing 4421-0059. It consists of:

- three 6-volt Stepper Motors
- three Centent CN0162 Stepper Motor Controllers
- Controller Input Power Control
- Sensor Switches

Stepper Motors

Each linear actuator is powered by a 6-volt Stepper Motor which is powered by a Stepper Motor Controller. The motor shaft moves 1.8° per step input (200 steps per revolution).

Stepper Motor Controllers

The Stepper Motor Controller provides +5 VDC logic power, Step and Direction inputs to the motor controllers which are in standby when they are not positioning their respective motor. In this state, they draw very little power. The controllers enter the active state if the Step input goes high. Table 5-2 describes the motor response to the Step and Dir inputs.

Step	Dir	Motor Response
0	0	Standby
0	1	Standby
1	0	CCW 1.8°
1	1	CW 1.8°

Table 5-2. Stepper Motor Responses

Controller Input Power Control

The controllers receive 48-volt motor excitation power from an Acopian B15G700 power supply mounted in the top drawer of the OCS enclosure. Solid-state relay K5, which is enabled by the J4 pin 9 output of the Parallel Interface board, controls AC power to the 48 VDC supply. K5 is located in the Relay Enclosure in the bottom drawer of the OCS enclosure.

Sensor Switches

Each linear actuator has a travel range of approximately 0.5 inch and is equipped with a normally closed microswitch sensor at each end of travel. The six sensor switches are interfaced to the Parallel Interface board via Switch Interface Board 2 (drawing 4421-0087, sheet 2 of 2) which is located in the top OCS drawer.

Secondary Mirror Vacuum Support Load Cell Interface

The Secondary Mirror Vacuum Support Load Cell Interface is shown on drawing 4421-0058. It consists of:

- Load Cells
- three Load Cell Preamplifiers

Load Cells

Three commercial strain-gauge type load cells are located in a triangular pattern between the Secondary Mirror and its mounting cell. The Load Cells have a linear millivolts/lb transfer function.

Load Cell Preamplifiers

The Load Cell Preamplifiers are modified Analog Devices AC1224 preamplifiers. Each preamplifier provides a precision reference output to its respective Load Cell. The preamplifier scales the input from a few millivolts/lb to 18 volts/lb.

Drawing 4421-0117 shows the modified Load Cell Preamplifier board. The modifications consist of adding an output buffer and modifying the board's gain factor.

The output buffer consists of:

- AD711JN operational amplifier
- two 47K ohm resistors
- 0.47 MFD capacitor

The buffer isolates the board's output from the capacitance resulting from the long cable runs between the preamplifier and the OCS enclosure.

The external gain of the Analog Devices 1B32 component is determined by the ratio of R7 to the combination of R6 and R1. R6 was changed from 100 ohms to 80.6 ohms to increase the gain enough so that R1 can be adjusted to produce a -5 to +5 VDC (10 volt range) with a -90 to +90 lb (180 lb range) force on the Load Cell.

The A/D 1 board converts the -5 to +5 VDC input to a count range of 0 - 4095 which represents -90 lbs to +90 lbs. Thus, each count represents 0.044 lbs and a count of 2047 represents zero lbs. Software running on the CPU board maintains the count between 1695 and 1805 (decimal). This is a software commanded range which equates to -13 lbs $\pm$2.42 lbs. Since there are three Load Cells, the mirror has 39 lbs ($\pm$7.26 lbs) outward force on the back of the mirror which is calibrated at these forces.

Secondary Mirror LVDT Interface

The Secondary Mirror LVDT Interface schematic diagram is 4421-0056. It consists of:

- three Linear Voltage Differential Transformers (LVDTs)
- Power Supply
- Power Supply Control Relay

Linear Voltage Differential Transformers (LVDTs)

The Secondary Mirror is positioned by three linear actuators. The mirror's total range of travel is approximately 0.5 inch. Each actuator has an associated LVDT which senses linear displacement.

The LVDT consists of an oscillator, movable core transformer and demodulator. The oscillator generates an AC voltage and applies it to the primary coil of the transformer. Voltage is induced into each transformer secondary coil as a function of the degree of coupling. When the movable core is fully retracted, the lower coil has maximum coupling and the upper coil has minimum, resulting in maximum negative output from the demodulator. When the movable core is centered, the equal and opposite outputs result in zero output from the demodulator. When the movable core is fully extended, the top coil has maximum output and the bottom coil has minimum output, resulting in maximum positive output.

When powered by a 28 VDC power supply, the LVDTs generate a -5 to +5 VDC range corresponding to a 0 - 0.5 inch travel. The outputs are applied to A/D 1 via low pass filters.

LVDT oscillators generate AC noise which must be prevented from reaching their outputs and power supply inputs. Each LVDT's input and output is filtered by a respective input and output low-pass filter located in a filter enclosure near the LVDTs. Each output filter has a 16 Hz roll-off while presenting a desirable inductive load to the LVDT. Each input filter prevents oscillator noise from reaching the power supply.

Power Supply

An Acopian 28EB30 28 VDC power supply powers the LVDTs. It is located in the top drawer of the OCS enclosure and receives its AC input power via relay K12 which is located in the Relay Enclosure in the bottom drawer of the OCS enclosure.

Power Supply Control Relay

The J4-11 output of the Parallel Interface board (LVDTPWR\) enables solid-state relay K12, the LVDTs' 28 VDC power supply control relay.

Tertiary Mirror Fold Mechanism Interface

The Tertiary Mirror Fold Mechanism Interface schematic diagram is drawing 4421- 0061. This interface consists of:

- Flip Actuator (motor)
- Motor Direction Control
- Motor Power Supply
- Control Logic
- Status Switches

Flip Actuator

The Flip Actuator is a 24-volt DC, 6-amp, permanent-magnet motor. Changing direction on this type of motor requires polarity reversal of the DC input.

Motor Direction Control

Solid-state relays K32 through K35 determine the direction of the DC current flow from the Lambda LMS-7040 power supply through the Flip Actuator. The relays are controlled by signals IN\ and OUT\ from the OCS Logic Board. K33 and K35 are enabled if OUT\ is low; K32 and K34 are enabled if IN\ is low. When IN\ is low, the polarity markings for the Flip Actuator are as shown on drawing 4421-0061; when OUT\ is low, the polarity markings are the opposite of those shown on the drawing. K32 - K35 are located in the middle drawer of the OCS enclosure.

Motor Power Supply

The Motor Power Supply is a Lambda model LMS 7040 24-volt supply located in the lower drawer of the OCS enclosure. It is referenced as PS8 on drawing 4421-0095, the OCS Lower Drawer Subassembly drawing. PS8 receives AC power via solid state relay K7 which is located in the Relay Enclosure in the bottom drawer of the OCS enclosure. K7 is enabled when the FLIPMOTPWR\ control signal from the Parallel Interface board goes low.

Control Logic

The Control Logic generates control signal IN\ and OUT\ for relays through K35. This logic is part of the OCS Logic which is shown (conceptually) in Figure 5-11 on page 5-47 and schematically in drawing 4421-XXXX.

Because part of the Tertiary Mirror mechanism extends above the two primary mirror covers, these covers must be retracted before the Tertiary Mirror is folded in or out. Each mirror cover closes a microswitch when it is fully open. These switches are interfaced to the OCS Logic Board by Switch Interface Board 2 (see sheet 1 of drawing 4421-0057). When the left mirror cover switch opens, MCLFTOPENED goes high; when the right mirror cover switch opens, MCRHTOPENED goes high.

Refer to Figure 5-11 on page 5-47 and drawing 4421-XXXX in the *WIYN Drawings* binder (see *Appendix A*). MCLFTOPENED and MCRHTOPENED are ANDed together by PAL 1 on the OCS Logic Board to form FOLD_O.K. This signal is gated with FLIPMOTOUT\ (fold out signal) and FLIPMOTIN\ (fold in signal), the motor direction control inputs from the Parallel Interface board. OUT\ is formed by ANDing FOLD_O.K. with inverted FLIPMOTOUT\ to form OUT which is inverted to form OUT\; FOLD_O.K. is ANDed with inverted FLIPMOTIN\ to form IN\ which is inverted to form IN\. Thus, IN\ or OUT\ can only be asserted if the Primary Mirror Covers are fully open and FLIPMOTOUT\ or FLIPMOTIN\ is asserted, respectively.

Status Switches

Refer to drawing 4421-0061. Two status switch inputs are interfaced by Switch Interface Board (SIB) 1 to form status signals FOLDIN\ and FOLDOUT\. The normally open FOLDIN, TORQUE #1 and TORQUE #2 switches are series connected. These switches must close before the SIB asserts FOLDIN\. The FOLDIN switch closes when the Tertiary Mirror Fold mechanism reaches its folded-in position. TORQUE 1 and 2 are closed when the Flip Actuator applies a certain amount of torque to the fold mechanism after the motor reaches the end stop and enters a stall condition. The fold-in position of the Tertiary Mirror is critical for NIR port usage. Forcing the Flip Actuator to build up a certain amount of torque after it reaches its end stop ensures that the Tertiary Mirror returns to the plane each time it is folded in.

The fold-out position of the Tertiary Mirror is not critical. It simply must fold out of the light beam. Thus, a single sensor switch detects the fold-out position. The FOLDOUT switch closes when the mirror reaches its folded-out position and causes the SIB to assert FOLDOUT\ low.

FOLDIN\ and FOLDOUT\ are interfaced to the CPU board via the Parallel Interface board. In addition, FOLDIN\ is output to the OCS Logic Board for use by the Mirror Cover Logic (see the Mirror Cover Interface description on page 5-44).

Tertiary Mirror Vacuum Support Load Cell Interface

The Tertiary Mirror Vacuum Support Load Cell Interface schematic is drawing 4421-0064. This circuit is identical to the Secondary Mirror Vacuum Support Load Cell Interface description on page 5-30.

Tertiary Mirror Rotator Interface

Schematic drawing 4421-0060 shows the Tertiary Mirror Rotator Interface. Figure 5-6 on page 5-16, the functional block diagram of the Tertiary Mirror Rotator Interface, shows these parts:

- Rotator Motor
- Motor Speed Control Module
- Speed/Direction Control
- OCS Logic Board (partial)
- Power Control Relay
- Latch Pin Solenoid
- Latch Pin Solenoid Control
- Latch Pin Status

Rotator Motor

The Tertiary Mirror Rotator Motor is a 90-volt permanent magnet DC motor. Its speed and direction are controlled by the Motor Speed Control Module.

Motor Speed Control Module

The Motor Speed Control Module is a Minarik model RG-310UA Regenerative DC Motor Speed Controller. It is located in the lower drawer of the OCS enclosure. It is designed to control motor loads of 1/20 through 1/8 hp. It can provide armature currents up to 1.5 amps. The controller must be adjusted to the motor for optimum motor performance.

The controller is a true four-quadrant regenerative controller. A motor operates in Quadrant 1 when it starts in the forward direction. Quadrant 2 regeneratively decelerates a forward running motor to a lower speed. That is, it applies a reverse torque to the motor to slow it down. Under this condition, the motor generates more power than it uses and the additional power is returned to the AC power grid (UPS). A motor operates in Quadrant 3 when it starts in the reverse direction. Quadrant 4 is similar to Quadrant 2 except the motor is running in reverse while it is being torqued in the forward direction to slow it down.

WARNING

The Minarik controller is not isolated from earth ground. Circuit potentials are at 115 VAC above ground. Contact with any element of the primary circuit can cause injury or death. All connections to the controller, including the Motor Control Circuit, are also at above-ground potential. Always use nonmetallic tools to adjust the controller while it is connected to line power. When checking fuse FU501, disconnect AC power at the input of the OCS enclosure by disconnecting plug P23 (lower drawer, front panel) to prevent the possibility of applying power via K6.

The controller adjustments are:

- MAX SPD (Maximum Speed)
- MIN SPD (Minimum Speed)
- FWD TQ (Forward Torque)
- REV TQ (Reverse Torque)
- FWD ACC (Forward Acceleration)
- REV ACC (Reverse Acceleration)
- IR COMP (armature IR Compensation)
- DB (Dead Band)

The MAX SPD is factory set to achieve rated speed at full load. Set this control fully clockwise since the Motor Control Circuit determines actual maximum speed.

The MIN SPD is a unidirectional feature and is not used in the WIYN application.

The FWD TQ setting determines the maximum torque for accelerating and driving the motor in the forward direction and decelerating a motor operating in the reverse direction. This control is factory set at 120% of full load for a 1/8 hp motor (about 1.5 amps). It should be set at 120% of the nameplate rating. Since the Rotator Motor's nameplate rating is 0.68 amps, this control should be set to deliver 0.82 amps when the motor is stalled in the forward direction.

The REV TQ performs the same functions for a motor running in reverse as FWD TQ does for a motor running in FWD. Therefore, FWD TQ should be set for 0.82 amps maximum when the motor is stalled in reverse direction.

The FWD ACC determines the forward acceleration rate and reverse deceleration rate. This control is factory set to maximum (fully counterclockwise). Unless Tertiary Mirror Rotator components are adversely affected by excessive acceleration or decelerations, set this control fully counterclockwise. The maximum acceleration rate is affected by the FWD TQ adjustment. If it is too low, the controller may not deliver enough applied torque to accelerate the load rapidly enough for this control to function. If this occurs, and FWD ACC is fully counterclockwise, increase FWD TQ to 130% of nameplate current.

The REV ACC is set the same as the FWD ACC control.

The IR COMP adjustment uses armature counter EMF to determine motor speed. This method of speed detection requires subtraction of armature voltage caused by the armature current flowing through the armature resistance (IR drop). Since the armature resistance is motor specific, this characteristic is approximated by IR COMP. For the Tertiary Mirror Rotator motor, set IR COMP to the 3 o'clock position. If the motor oscillates at this setting, turn the control counterclockwise until the oscillations cease. If the motor does not appear to maintain constant speed, turn the control clockwise until the motor maintains constant speed or begins to oscillate. If it begins to oscillate, turn the control counterclockwise until oscillation ceases.

The DB adjustment regulates the time between reversals of the output voltage polarity. This control is initially set to the 3 o'clock position for 60 Hz AC power. Clockwise rotation of the control shortens the dead band; counterclockwise lengthens the dead band. The correct setting depends largely on the motor. If the dead band is too long, the controller doesn't respond crisply to regeneration demands. If the dead band is too narrow, the controller produces regeneration responses to very slight changes in speed. The onset of this mode is detected by an audible hum in the motor while it is stopped. Extremely narrow dead bands result in pronounced vibration in the motor. The DB adjustment is normally set at a point slightly counterclockwise from the point where hum is first detected when the motor speed is set to zero.

Speed/Direction Control

The Minarik controller receives motor speed and direction inputs from the Motor Control Circuit (Speed/Direction Control block in Figure 5-6) shown on drawing 4421-0060. This circuit consists of a printed wiring board located near the Minarik controller in the lower drawer of the OCS enclosure. Its schematic diagram is drawing 4421-0066. The Minarik controller determines desired motor speed from an analog input to its S2 input terminal. The polarity of the S2-input determines the direction of motor rotation. A positive voltage at S2 with respect to terminal RB1 causes forward rotation; a negative voltage at S2 with respect to RB1 causes reverse rotation.

The Motor Control Circuit generates four fixed DC voltages, high and low speed forward voltages and high and low reverse speed voltages. Each voltage is available to the controller via a solid state opto-isolated relay. Each relay is enabled via a control input from the OCS Logic Board. Since only one relay is enabled at a time, the relays function as an electronically controlled 4-position switch.

OCS Logic Board (partial)

The OCS Logic is shown conceptually in Figure 5-11 on page 5-47 and schematically in drawing 4421-XXXX in the *WIYN Drawings* binder (see *Appendix A*). Outputs FWDFAST\, FWDSLOW\, REVFAST\ and REVSLOW\ control the Motor Control. PAL 1 generates these signals which are shown in the upper-right corner of the drawing.

The four output control signals are formed from three inputs from the Parallel Interface board and three status signals. The control inputs are:

- ROTMOTFWD\ (Rotate Motor Forward)
- ROTMOTREV\ (Rotate Motor Reverse)
- ROTMOTSLOW\ (Rotate Motor Slow)

The status signals are:

- MCLFTOPENED (Mirror Cover LeFT OPENED)
- MCRHTOPENED (Mirror Cover RigHT OPENED)
- IPRETRACTED\ (rotator Index latch Pin RETRACTED)

MCLFTOPENED and MCRHTOPENED are ANDed with inverted IPRETRACTED\ to form a gating signal called ROT_OK (ROTate OK). ROT_OK is high if the Primary Mirror Covers are retracted and the Tertiary Mirror's rotator latch pin is retracted.
Four NAND gates form the output signals from the three inputs from the Parallel Interface board and ROT_OK. Table 5-3 is the output truth table.

ROT_ OK	ROT MOT FWD\	ROT MOT REV\	ROT MOT SLOW\	REV FAST\	REV SLOW\	FWD FAST\	FWD SLOW\
0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	1	1
1	1	0	1	0	1	1	1
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1

Table 5-3. Rotator Control Signal Truth Table

Power Control Relay

Refer to drawing 4421-0060. Power Control Relay K6 controls the application of AC power to the Minarik controller. K6 is enabled when ROTMOTPWR\, an output of the Parallel Interface board, is low. K6 is located in the Relay Enclosure in the lower drawer of the OCS enclosure.

Latch Pin Solenoid

The Rotator Latch Pin is retracted by air pressure which is controlled by a 115 VAC solenoid valve. The valve receives 115 VAC power via K13 which is located in the Relay Enclosure in the lower drawer of the OCS enclosure.

Latch Pin Solenoid Control

The solenoid valve is controlled by solid state relay K13 which is enabled when PINRETRACT\ is low. PINRETRACT\ is an output of the Parallel Interface board.

Latch Pin Status

The Latch Pin includes an optional sensor package containing two sensors. One sensor opens when the Latch Pin is fully engaged; the other sensor opens when the Latch Pin is fully retracted.

Counterbalance Interface

The Counterbalance Interface is shown on drawing 4421-0052 (3 sheets). Sheets 1 and 2 describe the drive and brake controls for Counterbalance 1 and 2, respectively. Sheet 3 describes position sensing for both counterbalances.

Since the circuitry for both counterbalances is identical, only Counterbalance 1 is described. All relays used both counterbalance interfaces are located in the Relay Enclosure in the bottom drawer of the OCS enclosure. Figure 5-7 shows the functional sections of a counterbalance interface which includes:

- 120 VAC Counterbalance Drive Motor
- Motor Direction Control
- Limit Switch Selector Relays
- Forward and Reverse Limit Switches
- Position Sensor
- Brake Air Solenoid Valve
- Brake Solenoid Control

120 VAC Counterbalance Drive Motor

The counterbalance is positioned by a 120 VAC capacitor-run induction motor. Direction reversal is accomplished by reversing the phase of the AC power applied to the field winding (red and black leads) containing the run capacitor.

Motor Direction Control

Relay K26, located in the Relay Enclosure in the lower drawer of the OCS enclosure, controls the direction of the Counterbalance Drive Motor by effectively reversing the AC power phase to the field winding connected to the red and black leads. K26 receives 120 VAC coil voltage via solid state relay K8 which is controlled by REV1\, a control output of the Parallel Interface board. When K26 is de-energized, the motor runs forward when power is applied; when K26 is energized, the motor runs in reverse when power is applied.

Limit Switch Selector Relays

Solid State relay K1 selects the Forward Limit Switch as the active limit switch; solid state relay K2 selects the Reverse Limit Switch as the active limit switch. K1 or K2 applies 120 VAC to the BLK/RED motor lead via the Forward Limit switch or Reverse Limit Switch, respectively. K1 is enabled when FWDPWR1\ is asserted; K2 is enabled when REVPWR1\ is asserted.

Forward and Reverse Limit Switches

The Forward and Reverse Limit Switches are labeled Fwd Limit and Back Limit, respectively. Motor current flows through the contacts of K1 and Fwd Limit when K1 is enabled, or the contacts of K2 and Back Limit when K2 is enabled. If the motor is running forward, it trips the Fwd Limit switch when it reaches the forward end of travel. Likewise, it trips the Back Limit switch if the motor is in reverse and reaches the reverse end of travel.

When a limit switch opens, all power is removed from the motor and 115 VAC appears across its open contacts and the control inputs of relay K15 or K14, energizing the respective relay. If the Fwd Limit switch opens, K15 is energized; if the Back Limit switch opens, K14 is energized. K14 and K15 provide limit switch status to the Parallel Interface board.

Limit switch selection (controlled by K1 and K2) is independent of motor direction which is determined by the state of Motor Direction Control relay K26. K1, K2 and K26 (via K8) are controlled by the CPU board via the Parallel Interface board (signals FWDPWR1, REVPWR1 and REV1, respectively). Therefore, CPU software must prevent undesirable signal combinations such as asserting FWDPWR1 and REV1 simultaneously which would select the Reverse Limit Switch and run the motor forward. Under this condition, the motor would trip the Forward Limit Switch without disconnecting power from the motor.

Position Sensor

The Position Sensor is shown on sheet 3 of drawing 4421-0052. It consists of a linear 5K ohm potentiometer which is positioned by the counterbalance drive motor. The sensor receives +5 VDC from the REF-02 precision reference located on the OCS Logic Board. The REF-02 is powered by PS3, an Acopian model B15-50 power supply located in the top drawer of the OCS enclosure (see drawing 4421-0093).

Brake Air Solenoid Valve

The Counterbalance Brakes (one for each counterbalance) are engaged by spring pressure and disengaged by air pressure. Air pressure is supplied to the brakes via separate 115 VAC solenoid valves which are controlled by the Brake Solenoid Control.

Brake Solenoid Control

The Brake Solenoid Control consists of solid state relays K9 and K11. K9 controls AC power to the Brake Air Solenoid Valve for Counterbalance 1; K11 controls AC power to the Brake Air Solenoid Valve for Counterbalance 2. These relays are enabled by the CB1BRAKE\ and CB2BRAKE\ outputs of the Parallel Interface board, respectively.

Flat Field Lamp Interface

The schematic diagram for the Flat Field Lamp Interface is 4421-0054. The functional block diagram for this interface shows these blocks:

- Programmable Power Supplies 1 and 2
- 200 and 100 Watt Lamp Assemblies
- Digital-to-Analog Board
- Parallel Interface Board (partial)

Programmable Power Supplies 1 and 2

Each lamp assembly is driven by a Lambda model LMS-7060 programmable DC power supply located in the lower drawer of the OCS enclosure. Each supply receives 115 VAC input power via a relay.

The supplies have a voltage gain factor of 12. TCC/DCC software limits the maximum inputs to these supplies to +4 volts DC, which limits the outputs to 48 VDC.

PS9 receives AC power via solid state relay K23; PS10 receives AC power via solid state relay K24. These relays energize when pin 4 goes low. However, they require a greater current sink than the active low control outputs from the Parallel Interface board can deliver directly. Enhancement mode FETs labeled A1 and A2 are connected between ground and the pin 4 input of K12 and K24, respectively. They perform relay switching while reducing control input loading. The FETs require logic high inputs to turn on and energize their respective relays. The FETs, and relays K23 and K24 are located in the Relay Enclosure in the bottom drawer of the OCS enclosure.

200 and 100 Watt Lamp Assemblies

Each Flat Field Lamp Assembly consists of four 12-volt series-connected lamps. The 200 and 100 watt assemblies use 50 and 25 watt lamps, respectively.

Digital-to-Analog Board

Each power supply requires a 0 - 4 volt input to produce a 0 - 48 VDC output. Each input is developed by a channel on the D/A board.

Parallel Interface Board (partial)

Two outputs from the Parallel Interface board control AC power to the programmable power supplies. When FF1PWR is high, K23 is enabled; when FF2PWR is high, K24 is enabled.

Vacuum/Air Bag Solenoid Interface

The schematic diagram for the Vacuum/Air Bag Solenoid Interface is drawing 4421-0055. This interface consists of:

- Vacuum and Air Solenoids
- Power Relays
- Control Relays and the Parallel Interface Board
- Power Supply

Vacuum and Air Solenoids

Refer to the Secondary and Tertiary Mirror Air and Vacuum Control description on page 5-6.

The Secondary and Tertiary Mirror cells can be pressurized or evacuated via 115 VAC air or vacuum solenoids, respectively. The four valves (air and vacuum for each mirror) are identical.

Power Relays

Each air and vacuum solenoid valve receives AC power via a solid state opto-isolated power relay located near its respective solenoid valve.

Control Relays and the Parallel Interface Board

Opto-isolated control relays K18 - K21 control the solenoid power relays; K22 is a spare. These relays are located in the Relay Enclosure in the bottom drawer of the OCS enclosure. When enabled by inputs from the Parallel Interface board, the relays provide a low impedance path between pins 8 and 6, connecting the 8 VDC power supply to the inputs of the respective power relay via a 100 ohm resistor. The 100 ohm resistors limit the current inputs to the power relays to a safe value. The relays and resistors are located in the Relay Enclosure in the lower drawer of the OCS enclosure.

SECVACON\ (SECondary VACuum ON), SECAIRON\ (SECondary AIR ON), TERVACON\ (TERtiary VACuum ON) and TERAIRON\ (TERtiary AIR ON) enable control relays K18 - K21, respectively.

Power Supply

The power relays require 3 - 6 VDC to operate. An 8 VDC Power Supply located in the top drawer of the OCS enclosure (PS1 in drawing 4421-0093) provides drive for these relays via control relays K18 - K21. This power supply also provides power for the input side of both Switch Interface Boards.

Mirror Cover Interface

Drawing 4421-0057 is the schematic diagram of the Mirror Cover Interface. Each mirror cover half is controlled by a separate interface which consists of these blocks in Figure 5-10:

- Cover Drive Motor
- Motor Direction Control
- Motor Power Supply
- Status Switches

The Left Mirror Cover Interface is described here; the Right Mirror Cover Interface is similar.

All relays associated with the Mirror Cover Interface are located in the middle drawer of the OCS enclosure (see drawing 4421-0094).

The Mirror Covers have several names which are used interchangeably. The *Left Mirror Cover* is also called *Mirror Cover 1* and the *WIYN side Mirror Cover*; the *Right Mirror Cover* is also called *Mirror Cover 2* and the *MOS side Mirror Cover*.

Cover Drive Motor

Each mirror cover is positioned by a 28-volt, permanent-magnet, DC motor. Motor direction reversing is accomplished by reversing the direction of current flow through the motor. The polarities shown on the schematic are the polarities during opening.

Motor Direction Control

Solid-state relays K28 through K31 determine the direction of the DC current flow from the Lambda LMS-9040 power supply through the Cover Drive Motor. The relays are controlled by signals OPNLFT\ and CLSLFT\ from the OCS Logic Board. K28 and K30 are enabled if OPNLFT\ is low; K29 and K31 are enabled if CLSLFT\ is low. When OPNLFT\ is low, the polarity markings for the Mirror Cover Motor are as shown on drawing 4421-0057; when CLSLFT\ is low, the polarity markings for the Mirror Cover Motor are the opposite of those shown on drawing 4421-0057.

The OCS Logic Board is shown conceptually in Figure 5-11 on page 5-47 and schematically in drawing 4421-XXXX in the *WIYN Drawings* binder (see *Appendix A*). CLSLFT\ OPNLFT\, CLSRT\ and OPNRT\ are direction control inputs from the OCS Logic Board. They are driven by the 74FCT240 line driver which is driven by combinatorial logic in PAL 2. The cover opening logic for each cover consists of an AND gate which ANDs an active low command input from the Parallel Interface board and an inverted status input from SIB 2. For example, the command input to open the left cover is MCLFTOPN\ (Mirror Cover LeFT OPeN). This command is inverted and ANDed with inverted MC1OPENED which causes OPNLFT\ to be asserted until the cover fully opens and actuates the MC1OPENED switch, causing the MC1OPENED status signal to go high. When the status signal goes high, the command input is blocked, OPNLFT\ goes high and the motor stops. The mirror closing logic includes the term MOVE_OK which blocks the command if the Tertiary Mirror is not at the WIYN or MOS NIR position. Tables 5-4 and 5-5 are truth tables for the opening and closing functions

MCLFTOPENED *	MCLFTOPN\ *	OPENLFT\ *
0	0	0
0	1	1
1	0	1
1	1	1
* Replace *LFT* with *RHT* for the Right Mirror Cover		

Table 5-4. Mirror Cover Opening Logic Truth Table

MOVE_OK	MCLFTCLOSED *	MCLFTCLS\ *	CLSLFT\ *
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1
0	X	X	1
* X = don't care. Replace *LFT* with *RHT* for the Right Mirror Cover			

Table 5-5. Mirror Cover Closing Logic Truth Table

The signals that form MOVE_OK are status inputs from the Tertiary Mirror Rotator Interface (4421-0060). They are POS_1, POS_3, IPENGAGED\ and INDEX. For MOVE_OK to be asserted, all signals except IPENGAGED\ must be high.

Motor Power Supply

Two Lambda model LMS-9040 DC power supplies power the two Cover Drive Motors. Both power supplies receive AC input power via solid state relay K25. The power supplies and K25 are located in the middle drawer of the OCS enclosure (see drawing 4421-0094 for component location).

Status Switches

Four normally closed limit switches provide position status for the two covers. Each cover opens its respective OPENED status switch when it is fully opened; each cover opens its respective CLOSED limit switch when it is fully closed. The limit switches for the left mirror cover are MC1OPENED and MC1CLOSED; the limit switches for the right mirror cover are MC2OPENED and MC2CLOSED.

The status switches are interfaced to the Parallel Interface board and OCS Logic Board by Switch Interface Board 2 (SIB2).

Circuit Board Configuration

The seven STD Bus boards listed in Table 5-1 on page 5-7 must be properly configured before installation in the OCS Card Cage. Refer to the OCS Environment Specification (document number 4421-0035) for complete board configuration information.

Figure 5-11. OCS Logic Board Conceptual Logic Diagram

Scanner's note:

There are no pages in section 6 of this document.

Chapter 7
Table of Contents

Time Code Receiver 7-1

Introduction 7-1
Electrical Interfaces 7-3
  TPRO-VME Module 7-3
  IRIG-B Time Code Input 7-3
  Time Code Output 7-3
  Timing Signal Outputs 7-4
  Connector Pin Assignments 7-4
TPRO-VME Setup 7-6
  Software Addresses 7-6
  External Time Stamping 7-7
  FIFO Buffer Configuration Mode 7-7
  Rate Output Selection 7-7
TPRO-VME Installation 7-8
Electrical Specifications 7-9

Tables

  Table 7-1. User I/O Connector (J1) 7-4
  Table 7-2. Coaxial Time Code Output Connector (J5) 7-5
  Table 7-3. Coaxial Time Code Input Connector (J6) 7-5
  Table 7-4. Electrical Specifications 7-9

Electrical Interfaces

The TPRO-VME module contains these interfaces:

- TPRO-VME Module
- IRIG-B Time Code Input
- Time Code Output
- Timing Signal Outputs
- Connector Pin Assignments

TPRO-VME Module

The TPRO-VME module is a standard VME bus compatible card. It plugs directly into the Heurikon crate located in the middle equipment rack on the northeast side of the observatory's second level which houses other VME bus compatible, WIYN-related control electronics.

IRIG-B Time Code Input

The amplitude modulated IRIG-B input is used as a synchronization reference for the TCR. The input circuits accept amplitudes from 0.5 to 8.0 volts peak-to-peak. The acceptable ratios of large peaks to small peaks is from 2:1 to 4:1. The input impedance is 10k ohms and the input signal can be connected via coax to the BNC connector labeled J2 or the 20-pin connector labeled J1.

J1 pin assignments for the IRIG-B Time Code Input are:

J1 Pin	Signal
2	Time Code In+
4	Time Code In-

Time Code Output

The IRIG-B Time Code is output on BNC connector J3.

Timing Signal Outputs

The 1 Hz and 10 KHz timing signals required for system distribution are used by the WIYN Encoder Interface to generate the 200 Hz timing signal used to latch the various encoder information and drive the TPRO-VME External Event input.

J1 pin assignments for the Timing Signal Outputs are:

J1 Pin	Signal
10	1 Hz
12	10 KHz

Connector Pin Assignments

The TPRO-VME card contains four connectors labeled J1, J5, J6 and P1.

J1 is a front panel user I/O connector on the TPRO-VME module. A 20-pin ribbon cable connects it to the Encoder Interface Module. Pin definitions for J1 are shown in Table 7-1 below.

J1 Pin	Signal Name
1	N/C
2	Time Code In+
3	N/C
4	Time Code In -
5	N/C
6	N/C
7	N/c
8	IRIG-B Out
9	N/c
10	Sel Rate Out 1 (1 Hz)
11	N/C
12	Sel Rate Out 2 (10 Khz)
13	N/C
14	External Event In
15	N/C
16	N/C
17	N/C
18	N/C
19	N/C
20	1 MHz Disciplined

Table 7-1. User I/O Connector (J1)

Connector J5 is the coaxial Time Code output connector. It is described in Table 7-2.

Pin	Signal Name
Center	Time Code Out
Shield	Ground

Table 7-2. Coaxial Time Code Output Connector (J5)

Connector J6 is the Time Code input. It is described in Table 7-3.

Pin	Signal Name
Center	Time Code In +
Shield	Ground

Table 7-3. Coaxial Time Code Input Connector (J6)

Refer to ANSI/IEEE Standard 1014-1987 VME Specifications for the standard pin-out for VME connector P1.

TPRO-VME Setup

The TPRO-VME module requires jumpers for:

- setting up software addresses
- enabling external time stamping on the rising edge of the the 5 ms clock
- setting the FIFO buffer configuration mode
- selecting the rate output s (1 Hz and 10 KHz)

Several other jumpers on the module are not associated with these functions. All TPRO-VME jumpers not specifically described below should remain at their factory settings.

Each function is described in detail below. This configuration procedure is valid for TPRO-VME modules Revision D and greater with the PAL device code 930110E or 940309A in location U4. Verify that the revision level of your module is D or greater.

Software Addresses

The TPRO-VME module is mapped into the VME short address space (16-bit addresses). In VME terminology this requires the module to be configured as an *A16 slave* using configuration header P16.

Refer to the TPRO-VME manual addendum: p16. doc for P16 configuration header pin-out and associated information.

To configure the module as an A16 slave:

- connect P16-3 to P16-5
- connect P16-4 to P16-6

The base address is the upper byte of the 16-bit address. It is configured by the P4 terminal strip. P4-9 is a logic 0 level (ground) used for connecting address bits that are zeros. Address bits that are ones are not connected.

For a WIYN base address of 0700 Hex:

- daisy-chain these pins to B4-9
  P4-8 (Address 15) to P4-9 - Logic 0
  P4-7 (Address 14) to P4-8 - Logic 0
  P4-6 (Address 13) to P4-7 - Logic 0
  P4-5 (Address 12) to P4-6 - Logic 0
  P4-4 (Address 11) to P4-5 - Logic 0

- and leave these pins unconnected:
  P4-3 (Address 10) - Logic 1
  P4-2 (Adders 09) - Logic 1
  P4-1 (Adders 08) - Logic 1

External Time Stamping

The 5 ms system clock (external event) input enters the module on the front panel connector J1. The signal latches onboard time into a FIFO for subsequent VME reading. This capability can be enabled or disabled via jumpers W6, W7 and W8. To enable the external event input, connect W6 to W7.

FIFO Buffer Configuration Mode

P14 configures the FIFO Buffer Configuration Mode. In this mode, the FIFO is configured to be cleared and refilled on every external event by connecting P14-2 to P14-3. Thus, if any time stamp fragments remain in the FIFO after a host unload cycle, they are cleared prior to the next FIFO load cycle.

Rate Output Selection

The TPRO module is configured to provide 1 Hz and 10 KHz TTL-level pulse rates at its front panel connector J1. P13 is the output rate configuration header. To enable these rates, connect P13-1 (1 Hz) to P13-10 (Rate 1) and connect P13-7 (10 KHz) to P13-11 (Rate 1).

TPRO-VME Installation

The TPRO-VME module is not a standalone subsystem. The Encoder Interface Module and the TPRO-VME module depend on each other for timing. Both modules are housed in the Heurikon VME crate located in the middle equipment rack on Level 2.

Use the steps below to install the TPRO-VME module perform.

1. Locate the Heurikon VME crate in Rack 2.
2. Insert a properly configured TPRO-VME module into slot 3 (Slot 0 is the lowest slot in the crate).
3. Connect a 20-pin ribbon cable between the Encoder Interface module and the J1 connector on the TPRO-VME module.
4. Connect the incoming IRIG-B input to the J6 BNC connector if it is available.
5. Connect the coaxial output cable to the J3 BNC connector if you want the IRIG-B output.

Electrical Specifications

Refer to Table 7-4 for TPRO-VME electrical specifications.

Electrical Characteristic	Specifications
DC Power	+5 VDC (5%) @ 3. 5A (Max) +12 VDC (5%) @ 150 mA (Max) -12 VDC (5%) @ 100 mA (Max)
Input Code Modulation	Amplitude Modulated Rate: between 2:1 - 4:1
Input Code Amplitude	500 mV - 8 V peak to peak
Input Code Frequency Error	100 ppm Maximum
Input Code Impedance	10K Ohms
Input Common Mode Rejection	200V
Jam Resynchronization Threshold	200 uSec

Table 7-4. Electrical Specifications

Scanner's note:

There are no pages in section 8 of this document.

Appendix A
Referenced Drawings

This appendix summarizes the official WIYN Telescope Control System drawings referenced in Chapters 1 through 8 of the *WIYN Telescope Control System Maintenance Manual*. These drawings are located in the *WIYN Telescope Control System Drawings* binder which was updated 10/05/94.

Chapter 1 Drawings

Drawing Number	Title

None

Chapter 2 Drawings

Drawing Number	Title
4421-0018	DC Drive Power Control Subsystem Schematic
4421-0019	Servo Amplifier Subassembly Schematic
4421-0020	Current Monitor Schematic
4421-0022	Current Monitor Printed Wiring Board Layout/Assembly
4421-0024	DC Drive Power Relay Subassembly
4421-0026	Servo Amplifier Subassembly
4421-0029	DC Drive Power Rack Detail
4421-0033	Battery Charger Schematic
4421-0034	DCC/TCC Environment Specification
4421-0036	Xenotronix 8125 Battery Charger Schematic
4421-0040	DC Drive Power/Connector Panel Subassembly
4421-0045	DC Drive Power Wire Wrap Subassembly
4421-0047	DC Drive Power Test Load Subassembly
4421-0062	Servo Electronics Subsystem Power Distribution Schematic
4421-0063	Servo Electronics Subsystem Logic Board Schematic
4421-0076	Copley 220 Servo Amplifier Gain/Compensation Configuration
4421-0079	Emergency Stop Switch Wiring Diagram

4421-0080	SES Sensor Switch Interface Schematic
4421-0088	DCC Analog I/O List
4421-0098	SES Sensor Switch Interface PWB Subassembly
4421-0100	Servo Electronics Subsystem Connector Panel Subassembly
4421-0101	Servo Electronics Subsystem Wirewrap Board Layout
4421-0109	SES Connector Panel and Shelf Subassembly
4421-0135	SES Fuse and Relay Subassembly
4421-0141	DCDPS/Battery Charger Monitor PWB Subassembly
4421-0143	DCDPS/Battery Charger Monitor Schematic

Chapter 3 Drawings

Drawing Number	Title
4421-0062	Servo Electronics Subsystem Power Distribution Schematic
4421-0063	Servo Electronics Subsystem Logic Board Schematic
4421-0092	Maintenance Handpaddle Schematic
4421-0096	Dome Control Logic Document (Text Design File)

Chapter 4 Drawings

Drawing Number	Title
4421-0030	Encoder Interface Module Schematic
4421-0034	DCC/TCC Environment Specification
4421-0074	Encoder Interface Module Prototype Board Modifications
4421-0075	Encoder Interface Module Configuration
4421-0100	Servo Electronics Subsystem Connector Panel Subassembly
4421-0105	Encoder Glue Part Specification
4421-0107	Encoder Tracker Part Specification
4421-0142	Serial Opto-isolator PWB Schematic

Chapter 5 Drawings

Drawing Number	Title
4421-0035	OCS Environment Specification
4421-0052	Counterbalance Electrical Interface
4421-0054	Flat Field Lamp Electrical Interface Diagram
4421-0055	Vacuum-Airbag Solenoid Interface Diagram
4421-0056	Secondary LVDT Interface Diagram
4421-0057	Mirror Cover Interface Diagram
4421-0058	Secondary Vacuum Support Load Cell Interface Diagram
4421-0059	Secondary Stepper Motors Interface Diagram
4421-0060	Tertiary Rotator Interface Diagram
4421-0061	Tertiary Fold Mechanism Interface Diagram
4421-0064	Tertiary Vacuum Support Load Cell Interface Diagram
4421-0065	Thermocoupler Interface Diagram
4421-0066	Tertiary Motor Control Circuit Schematic
4421-0070	OCS Primary Power Diagram
4421-0087	OCS Switch Interface Board Schematic
4421-0093	OCS Upper Drawer Subassembly
4421-0094	OCS Center Drawer Subassembly
4421-0095	OCS Lower Drawer Subassembly
4421-0117	Load Cell Preamplifier Schematic

Chapter 6 Drawings

Drawing Number	Title
None	

Chapter 7 Drawings

Drawing Number	Title
4421-0034	DCC/TCC Environment Specification

Chapter 8 Drawings

Drawing Number	Title
None	

Appendix B
Battery Charger Modifications

Refer to sheet 1 of schematics 4421-0033 and 4421-0034 in *Appendix A*. Four modified XENOTRONICS 12-volt battery chargers keep the batteries fully charged when 120 VAC power is available. The battery chargers are temperature compensated and deliver higher charge voltage during low temperatures. Diagram 4421-0033 is a schematic of the modified chargers.

If a battery charger is replaced, verify that the following modification steps are performed or perform these steps prior to installation.

1. Disassemble the heat sink assembly. Apply silicone heat sink compound between the heat sink and angle stock and between all semiconductors and their mounting surfaces. Reassemble the heat sink assembly. Do not replace the bridge rectifier BR1 at this time.

2. Change R1, the 110 ohm current limit resistor to 150 ohms 1%. This sets the new current limit to 16 amps.

3. Remove D1 and connect the former D1 cathode pad to the positive output at the cathode of D2.

4. Locate the small circuit board and remove pin 1 from its mating connector.

5. Replace resistor R3 with a 60.4 K ohm 1% metal film resistor.

6. Replace resistor R4 with a 232 K ohm 1% metal film resistor.

7. Replace resistor R5 with a 20.5 K ohm 1% metal film resistor.

8. Replace diode D3 with a 10 K 1% metal film resistor in parallel with a YSI 44006 thermistor.

9. Replace resistor R6 with a 180 K ohm 5% composition resistor.

10. Remove LEDs D4 and D5.

11. Remove pins 13 and 15 from the connector on the small circuit board.

12. Connect a 56 K ohm 5% composition resistor between pins 13 and 15 on the connector on the small circuit board using the mounting holes and pads made available in step 11.

13. Connect an 8.2 K ohm 5% composition resistor between pins 2 and 4 of IC A1 on the foil side of the small circuit board .

14. Remove bridge rectifier BR1 (MB252). Drill and tap a 10-32 mounting hole through the angle stock and heat sink so that the replacement MB352 bridge rectifier can be mounted to the wide part of the angle stock attached directly to the heat sink. Apply silicone heat sink compound to the MB352 bridge and heat sink mounting surface. Mount the MB352 bridge rectifier to the heat sink with a 10-32 stainless steel screw and internal tooth lock washer. Tighten the mounting screw to 30 inch-pounds.

15. Replace the positive and negative wires to BR1 with AWG 12 wire soldered directly to the BR1 terminals. Remove the terminals from the two AC wires and solder the wires directly to the BR1 terminals.

Appendix C
Safety and Interlocks

Introduction

The Control System provides numerous hardware interlocks for the protection of both personnel and equipment. This section lists these interlocks, together with the operator's indication that the interlock is active, the devices disabled by each, and the recovery method from each interlock state.

The following conventions are used in the interlock descriptions.

- When a dome device is marked with an asterisk (*), the device is disabled only when the Dome Maintenance Keyswitch is in the ***COMPUTER*** position.
- The diamond (◊) indicates that the step is a software procedure or command.
- Any of the *Indications* listed indicate the interlock is active. If more than one Indication item is needed to uniquely identify the interlock status, these items are connected by the word *AND*.
- Figure C-1 is a sample MDCS screen. Refer to this figure when references are made to MDCS Page.

Interlocks

This Appendix describes these interlocks:

- Drive Control Keyswitch "OFF"
- Emergency Stop
- TCC/DCC Emergency Stop
- TCC/DCC Watchdog Timer Inactive
- Main Drive Lockout Switch "LOCKOUT"
- Azimuth Angle Hard Limits

mdcs page Wed Jan 18 14:27:43 1995 msg count 0

MDCS: off

Azimuth		Elevation		MOS NIR		WIYN NIR		Dome	
Amp cmd	off	Amp cmd	off	Amp cmd	off	Amp cmd	off	Brake	off
Brake cmd	off	Brake cmd	off	Brake cmd	off	Brake cmd	off	Clamp Unlock	off
Brake	off	Brake	off	Brake	off	Brake	off	Clamp Lock	off
CCW hard	off	Up hard	off	CCW hard	off	CCW hard	off	Clamp	off
CCW soft	off	Up soft	off	Center	CW	Center	CW	Inverter 1	OK
Center	CW	Down Hard	off	CW hard	off	CW hard	off	Inverter 2	OK
CW soft	off	Down soft	off	Indexed	off	Indexed	off	Inverter 1 LL	off
CW hard	off	Latch	free	Index dir	CCW	Index dir	CCW	Inverter 2 LL	off
Overspeed	off	Overspeed	off	Latch	free	Latch	free	Computer	off
Indexed	off	Indexed	off	Encoder	0	Encoder	0	Maintenance	off
Index dir	CCW	Index dir	down	Index	0	Index	0	Speed 1	0
Encoder mode	0	Tilt 20	off	Motor dmd	0	Motor dmd	0	Speed 2	0
Enc 1	0	Tilt 30	off					Speed 3	0
Enc 2	0	Tilt 85	off					Speed	0
Enc ave	0	Elevation zone	0						
Enc diff	0	Encoder	0					AIO status	0x00000000
Index 1	0	Index	0					DIO status	0x00000000
Index 2	0	Motor ratio	0.000					DIO port A	0x00000000
Motor ratio	0.000	Motor 1 dmd	0					DIO port B	0x00000000
Motor 1 dmd	0	Motor 1 mon	0.000					DIO port C	0x00000000
Motor 1 mon	0.000	Motor 2 dmd	0					DIO port D	0x00000000
Motor 2 dmd	0	Motor 2 mon	0.000					EIO status	0x00000000
Motor 2 mon	0.000								

Main power cmd	off	Interlocks	normal
Main power	off	Keylock on	off
Main relay	OK	Keylock start	off
NIR power cmd	off	Lift platform	down
NIR power	off	Lockout	off
NIR relay	OK	Tape switch	off
Estop switch	off	Watchdog	tock
Estop latch	off	Restart	off
Stop cmd	off	Audio	on
Stop cmd latch	off		
Battery	OK	Charger	OK

Figure C-1. Sample MDCS Page

TCC/DCC Watchdog Timer Inactive

Indication:

- MDCS Page - ***Watchdog*** no ***tick/tock***

Disables:

- Main Drive DC Power
- NIR Drive DC Power
- Main Drive Brakes
- NIR Brakes
- Dome Motor Brakes*
- Dome Clamp*
- Dome Inverters*
- Dome Inverter Power Relay*

Recovery Procedure:

1. Turn Drive Control Keyswitch ***OFF***.
2. ◊ Initialize TCS.
3. Turn Drive Control Keyswitch ***ON***.
4. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
5. ◊ Perform normal drive start-up.

Note 1. Momentary activation of this interlock removes power from all brakes and drives. After the interlock condition is cleared or overridden, power is not restored until the Drive Control Keyswitch is momentarily turned to the ***START*** position.

Main Drive Lockout Switch in "LOCKOUT"

Indication:

- MDCS Page - ***Lockout*** ***on***

Disables:

- Main Drive DC Power
- Main Drive Servo Amplifiers
- Main Drive Brakes

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. ◊ Turn off NIR Drive Power, disable NIR Drives, and engage NIR Brakes.
3. Turn Drive Control Keyswitch ***ON***.
4. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.

Emergency Stop

Indication:

- Emergency Stop Switch (ES) pressed
- MDCS Page - ***Estop switch on***

Disables:

- Main Drive DC Power
- NIR Drive DC Power
- Main Drive Brake
- NIR Brakes
- Dome Motor Brakes
- Dome Clamp
- Dome Inverters
- Dome Inverter Power Relay
- ES Auxiliary Relays
- ES Opto-isolators

Recovery Procedure:

1. Turn Drive Control Keyswitch ***OFF***.
2. Reset Emergency Stop Switch.
3. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
4. ◊ Turn off NIR Drive Power, disable NIR Drives, and engage NIR Brakes.
5. Turn Drive Control Keyswitch ***ON***.
6. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
7. ◊ Perform normal drive start-up.

Note 1. Momentary activation of this interlock removes power from all brakes and drives. After the interlock condition is cleared or overridden, power is not restored until the Drive Control Keyswitch is momentarily turned to the ***START*** position.

TCC/DCC Emergency Stop

Indication:

- MDCS Page - ***Estop latch on***

Disables:

- Main Drive DC Power
- NIR Drive DC Power
- Main Drive Brakes
- NIR Brakes
- Dome Motor Brakes
- Dome Clamp
- Dome Inverters
- Dome Inverter Power Relay
- ES Auxiliary Relays
- ES Optoisolators

Recovery Procedure:

1. Turn Drive Control Keyswitch ***OFF***.
2. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
3. ◊ Turn off NIR Drive Power, disable NIR Drives, and engage NIR Brakes.
4. ◊ Reset TCS Stop Command.
5. Turn Drive Control Keyswitch ***ON***.
6. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
7. ◊ Perform normal drive start-up.

Note 1. Momentary activation of this interlock removes power from all brakes and drives. After the interlock condition is cleared or overridden, power is not restored until the Drive Control Keyswitch is momentarily turned to the ***START*** position.

Note 3. Azimuth Overspeed, Elevation Overspeed, TCS Emergency Stop, and Tape Switch interlocks are activated by a momentary interlock condition and remain in effect until reset as indicated.

- Elevation Angle Hard Limits
- Elevation Latch Pin Engaged
- Lift Platform Raised
- Azimuth Overspeed
- Elevation Overspeed
- Fork Tape Switch (Momentary)
- MOS NIR Rotation Limit
- WIYN NIR Rotation Limit
- Dome Keyswitch "LOCK"

Interlock Recovery Notes

One or more of the following notes may apply to the recovery process for some interlocks.

Note 1. Momentary activation of this interlock removes power from all brakes and drives. After the interlock condition is cleared or overridden, power is not restored until the Drive Control Keyswitch is momentarily turned to the ***START*** position.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

Note 3. Azimuth Overspeed, Elevation Overspeed, TCS Emergency Stop, and Tape Switch interlocks are activated by a momentary interlock condition and remain in effect until reset as indicated.

Applicable notes are reprinted at the bottom of each interlock description page.

Drive Control Keyswitch "OFF"

Indication:

- Drive Control Keyswitch position
- MDCS Page - ***Keylock on*** ***off***

Disables:

- Main Drive DC Power
- NIR Drive DC Power
- Main Drive Brakes
- NIR Brakes
- Dome Motor Brakes*
- Dome Clamp*
- Dome Inverters*
- Dome Inverter Power Relay*

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. ◊ Turn off NIR Drive Power, disable NIR Drives, and engage NIR Brakes.
3. Turn Drive Control Keyswitch ***ON***.
4. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
5. ◊ Perform normal drive start-up.

Note 1. Momentary activation of this interlock removes power from all brakes and drives. After the interlock condition is cleared or overridden, power is not restored until the Drive Control Keyswitch is momentarily turned to the ***START*** position.

Azimuth Angle Hard Limits

Indication:

- MDCS Page (Azimuth column) - ***CW hard*** ***on***
- MDCS Page (Azimuth column) - ***CCW hard*** ***on***

Disables:

- Main Drive DC Power
- Main Drive Servo Amplifiers
- Main Drive Brakes

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. ◊ Turn off NIR Drive Power, disable NIR Drives, and engage NIR Brakes.
3. Ensure that an operator is in a position to observe both Azimuth and Elevation motion, and to activate an Emergency Stop switch, if necessary.
4. Turn Interlock Override switch to ***OVERRIDE*** and hold.
5. ◊ Perform normal Azimuth Drive start-up. Do not enable Elevation or NIR drives.
6. ◊ Back Azimuth Drive away from limit.
7. Release Interlock Override switch.
8. ◊ Perform normal Elevation and NIR Drive start-up procedures, if desired.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

Elevation Angle Hard Limits

Indication:

- MDCS Page (Elevation column) - ***Up hard*** ***on***
- MDCS Page (Elevation column) - ***Down hard*** ***on***

Disables:

- Main Drive DC Power
- Main Drive Servo Amplifiers
- Main Drive Brakes

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. ◊ Turn off NIR Drive Power, disable NIR Drives, and engage NIR Brakes.
3. Ensure that an operator is in a position to observe both Azimuth and Elevation motion, and to activate an Emergency Stop switch, if necessary.
4. Turn Interlock Override switch to ***OVERRIDE*** and hold.
5. ◊ Perform normal Elevation Drive start-up. Do not enable Azimuth or NIR drives.
6. ◊ Back Elevation Drive away from limit.
7. Release Interlock Override switch.
8. ◊ Perform normal Azimuth and NIR Drive start-up procedures, if desired.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

Azimuth Overspeed

Indication:

- MDCS Page (Azimuth column) - ***Overspeed*** ***on***

Disables:

- Main Drive DC Power
- Main Drive Servo Amplifiers
- Main Drive Brakes

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
3. ◊ Perform normal Main Drive start-up.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

Note 3. Azimuth Overspeed, Elevation Overspeed, TCS Emergency Stop, and Tape Switch interlocks are activated by a momentary interlock condition and remain in effect until reset as indicated.

Elevation Overspeed

Indication:

- MDCS Page (Elevation column) - ***Overspeed*** ***on***

Disables:

- Main Drive DC Power
- Main Drive Servo Amplifiers
- Main Drive Brakes

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
3. ◊ Perform normal Main Drive start-up.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

Note 3. Azimuth Overspeed, Elevation Overspeed, TCS Emergency Stop, and Tape Switch interlocks are activated by a momentary interlock condition and remain in effect until reset as indicated.

Elevation Latch Pin Engaged

Indication:

- MDCS Page - ***Latch engaged***

Disables:

- Elevation Servo Amplifiers

Recovery Procedure:

1. ◊ Disable Elevation Drive and engage Elevation Brakes.
2. Disengage Elevation Latch Pin
3. ◊ Perform normal Elevation Drive start-up.

Lift Platform Raised

Indication:

- MDCS Page - ***Lift Platform up***

Disables:

- Main Drive DC Power
- Main Drive Servo Amplifiers
- Main Drive Brakes

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. Lower Lift Platform
3. ◊ Perform normal Main Drive start-up.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

Note 3. Azimuth Overspeed, Elevation Overspeed, TCS Emergency Stop, and Tape Switch interlocks are activated by a momentary interlock condition and remain in effect until reset as indicated.

Fork Tape Switch (Momentary)

Indication:

- MDCS Page - ***Tape switch on***

Disables:

- Main Drive DC Power
- Main Drive Servo Amplifiers
- Main Drive Brakes

Recovery Procedure:

1. ◊ Turn off Main Drive Power, disable Main Drives, and engage Main Drive Brakes.
2. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
3. ◊ Perform normal Main Drive start-up.

MOS NIR Rotation Limit

Indication:

- MDCS Page (MOS NIR column) - ***CW hard*** ***on***
- MDCS Page (MOS NIR column) - ***CCW hard*** ***on***

Disables:

- NIR DC Power
- NIR Servo Amplifiers

Recovery Procedure:

1. ◊ Turn off NIR Power, disable NIR Drives, and engage NIR Drive Brakes.
2. ◊ Turn off Main Drive Power, disable Main Drives, and Main Drive Brakes.
3. Ensure that an operator is in a position to observe motion of both NIRs, and to activate an Emergency Stop switch, if necessary.
4. Turn Interlock Override switch to ***OVERRIDE*** and hold.
5. ◊ Perform normal MOS Drive start-up. Do not enable Main Drives or WIYN NIR drive.
6. ◊ Back MOS NIR Drive away from limit.
7. Release Interlock Override switch.
8. ◊ Perform normal Main Drive and WIYN NIR Drive start-up procedures, if desired.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

WIYN NIR Rotation Limit

Indication:

- MDCS Page (WIYN NIR column) - ***CW hard*** ***on***
- MDCS Page (WIYN NIR column) - ***CCW hard*** ***on***

Disables:

- NIR DC Power
- NIR Servo Amplifiers

Recovery Procedure:

1. ◊ Turn off NIR Power, disable NIR Drives, and engage NIR Drive Brakes.
2. ◊ Turn off Main Drive Power, disable Main Drives, and Main Drive Brakes.
3. Ensure that an operator is in a position to observe motion of both NIR's, and to activate an Emergency Stop switch, if necessary.
4. Turn Interlock Override switch to ***OVERRIDE*** and hold.
5. ◊ Perform normal WIYN Drive start-up. Do not enable Main Drives or MOS NIR drive.
6. ◊ Back WIYN NIR Drive away from limit.
7. Release Interlock Override switch.
8. ◊ Perform normal Main Drive and MOS NIR Drive start-up procedures, if desired.

Note 2. Interlock Override resets and/or overrides Main Drive and NIR hard limits, Azimuth and Elevation Overspeed interlocks, and TCS Emergency Stop. Other interlocks cannot be overridden. Software always inhibits rotation toward an active hard limit switch.

Dome Keyswitch "LOCK"

Indication:

- MDCS Page (Dome column) - ***Computer*** ***off***
- *AND*
- MDCS Page (Dome column) - ***Maintenance*** ***off***

Disables:

- Dome Motor Brakes
- Dome Clamp
- Dome Inverters
- Dome Inverter Power Relay

Recovery to COMPUTER Mode:

1. Turn Dome Control Keyswitch to the "COMPUTER" position.
2. Turn Drive Control Keyswitch ***ON***.
3. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
4. ◊ Perform normal dome Start-up.

Recovery to MAINTENANCE Mode:

1. Turn Dome Control Keyswitch to the ***MAINTENANCE*** position.
2. Turn Drive Control Keyswitch ***ON***.
3. Momentarily turn Drive Control Keyswitch to ***START***, then back to ***ON***.
4. Operate Dome using Dome Maintenance Hand Paddle.

Appendix D
WIYN Purchased Equipment Manual List

Manufacturer	Item	Model Number	Application
Carter	Tachometer, Overspeed,	CTA60DA	
Centent Co.	Microstep Drive	CN0162	OCS Secondary Steppers
CmC	Thermocoupler	CNTRL1/TCP1	
Heurikon	V3D Schematics		
Heurikon	Enclosure	HSE/10	
Heurikon	Enclosure	HSE/12	
Heurikon	68030 SBC	HK68/V3D	
ICS	Serial I/F Card	RS422AT-P	
Interface	Load Cell	1010-500	Secondary/Tertiary
KSI Div/Odetics	Time Generator	TPRO-VME	
LambdaOCS	Power Supply	LMS-7040	Tertiary Fold Motor
Lambda	Power Supply	LMS-7060	OCS Flat Field Lamp
Lambda	Power Supply	LMS-9040	OCS Mirror Cover Motor
MacroLink, Inc	AsyncComMultiplexer	221001	
Matrix Corp	A/D-D/A Converter	MD-DAADIO	
Matrix Corp.	I/O Board	MD-DIO	
Minarik	Motor Controller	RG310UA	OCS Tertiary Rotator
PFT, Inc.	Enclosure	MDR192223 PRR	OCS
QSI Corp.	Data-Entry Terminal	QTERM II	Telescope Handpaddle
Realistic	Audio Amplifier	MPA-25	Audio System
Toshiba	Transistor Inverter	TOSVERT-130 G2	Dome Drive
Trans-Tek	Gage Transducer	0352-0000	Secondary LVDT
WinSystems, Inc	Quad Serial I/O Card	LPM-SI04	
WinSystems, Inc	V40 S/BComputer	LPM-SBC40A	
WinSystems, Inc	A/D Converter	LPM/MCM-A/D12	
XYCOM	Prototype Module	XVME-085	
XYCOM	Extender Board	XVME-090	
Young	Programmable Translator	26700	Weather Station
Young	Radiation Shield	41002/41004	Weather Station
Young	Wind Monitor	05103	Weather Station

Table D-1. WIYN Purchased Equipment Manual List

Index

A

A/D 0 Board (OCS) 5-7, 5-15, 5-19
A/D 1 Board (OCS) 5-7, 5-11, 5-13, 5-15, 5-30→5-31
Actuator
  Tertiary Mirror Flip 5-15, 5-32→5-33
Adjustment
  Azimuth Overspeed Threshold 2-29
  Tertiary Mirror Rotator Controller 5-36→5-37
Air Solenoid
  Counterbalance Brake Release 5-19, 5-40→5-41
  Secondary Mirror Air Bag 5-5, 5-22→5-23, 5-43
  Tertiary Mirror Air Bag 5-43
  Tertiary Mirror Rotator Latch Pin 5-17, 5-39
Amplifier
  Azimuth Servo 2-9, 2-18, 2-34
  Elevation Servo 2-4, 2-9, 2-18, 2-34, 2-39
  Main Drive Servo 2-7, 2-11→2-12, 2-19, 2-31, 2-33, 2-37
  MOS NIR 2-18
  NIR Servo 2-7, 2-11→2-12, 2-18→2-19, 2-28, 2-33, 2-37
  Servo 2-1, 2-3→2-4, 2-7→2-8, 2-11, 2-18→2-20, 2-22, 2-24, 2-27, 2-35, 2-37, 2-39
  WIYN NIR 2-18
Analog I/O Board 2-3, 2-23→2-24
AOS logic signal 2-31, 2-34→2-35
AREL logic signal 2-33, 2-37, 2-40
Assembly
  100 Watt Flat Field Lamp 5-5, 5-21, 5-42
  200 Watt Flat Field Lamp 5-5, 5-21, 5-42
  Secondary Mirror and Cell 5-3
AZ CW Soft Limit switch 2-32
AZ TACH OUT+ 2-29
AZ TACH OUT- 2-29
AZBC logic signal 2-38
AZBCREL/ logic signal 2-38, 2-42
AZE/ logic signal 2-39
AZEC logic signal 2-39
Azimuth Brake 2-34
  Control Logic 2-38
  Control Relay 2-34, 2-38
  Pressure Switch 2-10
Azimuth Encoders 2-41
Azimuth Overspeed
  Latch 2-31
  LED 2-31
  Processor 2-28, 2-36
  Tachometer 2-29
  Threshold Adjustment 2-29
  Threshold Reference Generator 2-29
  Threshold Reference Voltage 2-29
Azimuth Servo Amplifier 2-9, 2-18, 2-34
Azimuth Tachometer 2-28

B

Back Limit (Counterbalance Limit Switch) 5-41
Batteries 2-14
Battery Chargers 2-7, 2-14
Block diagrams
  Counterbalance Interface 5-18
  Flat Field Lamp Interface 5-20
  Main Drive and NIR Servos 2-6
  Main Drive and NIR Simplified 2-2
  Mirror Cover Interface 5-24
  OCS Functional 5-4
  Secondary Mirror LVDT Interface 5-12
  Secondary Mirror Stepper Motor Interface 5-8
  Secondary Mirror Vacuum Support Load Cell Interface 5-10
  Servo Electronics Subsystem 2-8
  Tertiary Mirror Fold Mechanism Interface 5-14
  Tertiary Mirror Rotator Interface 5-16
  Vacuum/Air Bag Solenoid Interface 5-22
Board
  A/D 0 (OCS) 5-7, 5-15, 5-19
  A/D 1 (OCS) 5-7, 5-11, 5-13, 5-15, 5-30→5-31
  Analog I/O 2-23
  COM-4 (OCS) 5-3, 5-7, 5-9, 5-28
  CPU (OCS) 5-1→5-3, 5-5→5-7, 5-9, 5-11, 5-15, 5-17, 5-19, 5-25, 5-30, 5-33
  Current Monitor Printed Wiring 2-13, 2-22
  D/A (OCS) 5-7, 5-21, 5-42
  DC Drive Power Wire Wrap 2-13→2-14
  Fuse and Relay 2-25, 2-27, 2-38, 2-40, 2-42
  Load Cell Preamplifier 5-11, 5-30
  OCS Logic 5-17, 5-27, 5-32→5-33, 5-38, 5-44→5-46
  Parallel Interface (OCS) 5-7, 5-9, 5-13, 5-15, 5-17, 5-19, 5-21, 5-23, 5-25, 5-29, 5-31→5-33, 5-38→5-43, 5-46
  Sensor Switch Interface 2-13, 2-32
  SES Logic 2-25, 2-27, 2-32, 2-35, 2-37
  Switch Interface Board 5-23, 5-27, 5-29, 5-33, 5-43
Brake
  Air Solenoid Valve (Counterbalance) 5-41
  Azimuth 2-34
  Control Logic 2-10→2-12, 2-32, 2-37→2-38, 2-42
  Counterbalance 5-19
  Drivers 2-9, 2-11→2-12, 2-42→2-44
  Drivers Relays 2-42

Pressure Switches 2-10
release signals 2-42
Solenoid Control (Counterbalance) 5-41

C

Cassegrain Port 5-15
CB1BRAKE Logic Signal 5-41
CB2BRAKE Logic Signal 5-41
CCHL logic signal 2-34
Charger, Battery 2-7, 2-14, 2-17
Circuit Board Configuration (OCS) 5-46→5-48
CLOSED Mirror Cover Limit Switch 5-46
CLSLFT\ Logic Signal 5-44→5-45
CLSRT\ Logic Signal 5-45
Command,
Emergency Stop 2-11, 2-33, 2-40
Configuration
OCS STD Bus Circuit Boards 5-46→5-48
Control
Tertiary Mirror Rotator Latch Pin Solenoid 5-17, 5-35, 5-39
Control Logic 2-14, 2-19
Brake 2-10→2-12, 2-32, 2-37→2-38, 2-42
Dome 2-5, 2-11, 2-25, 2-39
Power 2-10→2-11, 2-32, 2-37
SES 2-9→2-11, 2-25, 2-27, 2-32
Control Logic block 2-3→2-4
Controller
Stepper Motor 5-9, 5-29
Counterbalance
Brakes 5-41
Drive Motors 5-40
Interface 5-9, 5-19, 5-40→5-41
Interface Block Diagram 5-18
Mechanism 5-19
Cover
Drive Motors 5-44, 5-46
Primary Mirror 5-15, 5-17, 5-33, 5-38
CPU Board (OCS) 5-1→5-3, 5-6→5-7, 5-9, 5-11, 5-15, 5-17, 5-19, 5-25, 5-30, 5-33, 5-41
Current Monitor 2-13, 2-22→2-24
CWHL logic signal 2-34

D

D/A Board (OCS) 5-7, 5-21, 5-42
DC Drive Power Control 2-43
DC Drive Power Subsystem 2-3, 2-5, 2-7, 2-11, 2-14→2-21, 2-23, 2-28, 2-33, 2-37→2-39, 2-41
DC Drive Power Test Load 2-22, 2-24→2-26
Dead Band (DB) Adjustment (Tertiary Mirror Rotator) 5-37
Detailed Circuit Description
Main Drive and NIR Servos 2-13
OCS 5-27
DHL logic signal 2-34
Digital-to-Analog Board (OCS) 5-7, 5-21, 5-42
Dome
Clamp Pressure switch 2-10
Control Logic 2-5, 2-11, 2-25, 2-39
Control MAINT and COMP switch 2-10
Inverter Fault switches 2-10
Inverters 2-5
Maintenance Handpaddle switches 2-10
Motor Low Velocity switches 2-10
Servo Subsystem 2-5
Drive Control Keyswitch 2-12, 2-40→2-41
Drive Power Monitors 2-10→2-11, 2-32, 2-37
Drivers, Brake 2-9, 2-11→2-12, 2-42→2-44
Drivers, Power Relay 2-20

E

ELBCREL/ logic signal 2-42
ELE/ logic signal 2-20, 2-39
ELEC logic signal 2-39
Elevation
Brake Control Logic 2-38
Brake Pressure Switch 2-10
Encoder 2-41
hard and soft limit switches 2-10
Latch Pin 2-4, 2-39
Latch Pin switch 2-10, 2-39
Latch Pin Telemetry 2-39
Overspeed Processor 2-28
Overspeed Threshold Reference Voltages 2-30
Servo 5-5
Servo Amplifier 2-4, 2-9, 2-18, 2-34, 2-39
Tachometer 2-28, 2-30
Threshold Reference 2-29
Tilt Switches 2-10, 2-28→2-30
ELP logic signal 2-39
Emergency Stop
Command 2-11, 2-33, 2-40
Command Latch 2-33, 2-39
Logic 2-10→2-12, 2-19, 2-27, 2-32→2-33, 2-37, 2-40
Relays 2-9, 2-12, 2-25, 2-40→2-41
Switch Interface 2-9, 2-25, 2-27, 2-33
Switch Interface Wiring 2-26
Switch telemetry 2-33
Switches 2-9, 2-12, 2-27→2-28, 2-33, 2-40
Enclosure
LVDT Filter 5-31
OCS 5-1→5-2, 5-7, 5-29, 5-31→5-32, 5-35→5-37, 5-39→5-44, 5-46

Relay (OCS) 5-29, 5-31→5-32, 5-39→5-40, 5-42→5-43
Secondary Mirror Load Cell Preamplifier 5-11
Thermocoupler 5-3
Encoder Interface 2-3
EOS logic signal 2-34, 2-36
ESW logic signal 2-27→2-28
ESW/ logic signal 2-27→2-28

F

FF1PWR Logic Signal 5-42
FF2PWR Logic Signal 5-42
Flat Field Lamp
Assemblies 5-5, 5-21, 5-42
Interface 5-20→5-21, 5-42
Flip Actuator 5-32→5-33
FLIPMOTIN\ Logic Signal 5-33
FLIPMOTOUT\ Logic Signal 5-33
FLIPMOTPWR\ Logic Signal 5-32
FOLD_OK Logic Signal 5-33
FOLDIN Sensor Switch 5-33
FOLDIN\ Logic Signal 5-33
FOLDOUT Sensor Switch 5-33
FOLDOUT\ Logic Signal 5-33
Functional Block Diagram
Main Drive and NIR Servos 2-6
OCS 5-4
Servo Electronics Subsystem 2-8
Functional Description
Main Drive and NIR Servos 2-5
OCS 5-3
Fuse and Relay Board 2-25, 2-27, 2-38, 2-40, 2-42
FWD ACC Adjustment (Tertiary Mirror Rotator) 5-37
Fwd Limit (Counterbalance Limit Switch) 5-41
FWD TQ Adjustment (Tertiary Mirror Rotator) 5-36
FWDFAST\ Logic Signal 5-38→5-39
FWDPWR1\ Logic Signal 5-40
FWDSLOW\ Logic Signal 5-38→5-39

G

Generator
Overspeed Threshold Reference 2-28→2-29
Power-on Reset 2-39

I

ILOR logic signal 2-34→2-36, 2-39→2-40
IN\ Logic Signal 5-32→5-33
INDEX
Logic Signal 5-45
Switch (Tertiary Mirror Rotator) 5-17
Index Pin, Tertiary Mirror Rotator 5-17, 5-19
Index Sensor 2-3
Inhibit
Main Drive 2-34, 2-38
NIR 2-34, 2-36
Inrush
Limiter 2-37
Relays 2-19
Interface
Counterbalance 5-19, 5-40→5-41
Emergency Stop Switch 2-9, 2-11, 2-27, 2-33, 2-40
Encoder 2-3
Flat Field Lamp 5-21, 5-42
Mirror Cover 5-6, 5-25, 5-44→5-45
Secondary Mirror Fold Mechanism 5-32→5-33
Secondary Mirror LVDT 5-13, 5-31
Secondary Mirror Stepper Motor 5-9, 5-29
Secondary Mirror Vacuum Support Load Cell 5-11, 5-30
Sensor Switch 2-9→2-11, 2-25, 2-29→2-30, 2-32, 2-34→2-35, 2-39
SES Sensor Switch 2-25
Tachometer 2-9, 2-11
Tertiary Mirror Fold Mechanism 5-15
Tertiary Mirror Rotator 5-17, 5-35→5-39
Tertiary Mirror Vacuum Support Load Cell 5-15, 5-34
Thermocoupler 5-9, 5-28
Vacuum/Air Bag Solenoid 5-23, 5-25, 5-43
Interlock
Logic 2-10→2-12, 2-31→2-32, 2-34, 2-38→2-39
Logic, NIR 2-36
Override Switch 2-9, 2-34→2-35, 2-39
telemetry, NIR 2-36
IPENGAGED\ Logic Signal 5-45
IPRETRACTED\ Logic Signal 5-38
IR COMP Adjustment (Tertiary Mirror Rotator) 5-37

K

Keyswitch
Drive Control 2-12, 2-40→2-41

L

Latch Pin
  Elevation 2-4, 2-39
  Tertiary Mirror Rotator 5-17, 5-19, 5-39
Lift Platform switch 2-10→2-11, 2-35→2-36
Lift Platform telemetry 2-35
Linear Voltage Differential Transformer
  See LVDT
Load Cells 5-5, 5-11, 5-30
  Interface, Secondary Mirror Vacuum Support 5-11, 5-30
  Interface, Tertiary Mirror Vacuum Support 5-15, 5-34
  Preamplifiers 5-30
Logic
  Azimuth and Elevation Brake Control 2-38
  Board, OCS 5-17, 5-27, 5-32→5-33, 5-38, 5-44→5-46
  Board, SES 2-25, 2-27, 2-35
  Brake Control 2-10→2-12, 2-38, 2-42
  Dome Control 2-5, 2-25
  Emergency Stop 2-10→2-12, 2-19, 2-27→2-28, 2-33, 2-37, 2-40
  Interlock 2-10→2-12, 2-31, 2-34, 2-38→2-39
  Main Drive Interlock 2-34
  NIR Interlock 2-36
  Power Control 2-10→2-11, 2-32, 2-37→2-38
  Power Relays and Control 2-14, 2-18→2-20
  Reset 2-10→2-11, 2-33, 2-39
  Servo Amplifier Enable 2-10→2-11, 2-39
  SES Control 2-9→2-10, 2-27, 2-32
  Watchdog Timer 2-10→2-11, 2-37
Logic Signals
  AC RTN 2-18→2-19, 2-41
  AOS 2-31, 2-34→2-35
  AREL 2-33, 2-37, 2-40
  AZ TACH OUT+ 2-29
  AZ TACH OUT- 2-29
  AZBC 2-38
  AZBCREL/ 2-38, 2-42
  AZE/ 2-20, 2-39
  AZEC 2-39
  BREL 2-40
  CB1BRAKE\ 5-41
  CB2BRAKE\ 5-41
  CCHL 2-34
  CLSLFT\ 5-44→5-45
  CLSRT\ 5-45
  CWHL 2-34
  DHL 2-34
  ELBCREL/ 2-42
  ELE/ 2-20
  ELEC 2-39
  ELP 2-39
  ELP/ 2-39
  EOS 2-34, 2-36
  ESW 2-27→2-28
  ESW/ 2-27→2-28
  FF1PWR 5-42
  FF2PWR 5-42
  FLIPMOTIN\ 5-33
  FLIPMOTOUT\ 5-33
  FLIPMOTPWR\ 5-32
  FOLD_OK 5-33
  FOLDIN\ 5-33
  FOLDOUT\ 5-33
  FWDFAST\ 5-38→5-39
  FWDPWR1\ 5-40
  FWDSLOW\ 5-39
  ILOR 2-34→2-36, 2-39→2-40
  IN\ 5-32→5-33
  INDEX 5-45
  IPENGAGED\ 5-45
  IPRETRACTED\ 5-38
  LP 2-34→2-35
  LVDTPWR\ 5-31
  MBCREL/ 2-42
  MC1CLOSED 5-46
  MC1OPENED 5-45→5-46
  MC2CLOSED 5-46
  MC2OPENED 5-46
  MCCL 2-36
  MCLFTCLOSED 5-45
  MCLFTCLS\ 5-45
  MCLFTOPENED 5-33, 5-38, 5-45
  MCLFTOPN\ 5-45
  MCRHTOPENED 5-33, 5-38
  MCWL 2-36
  MDINH/ 2-34, 2-36, 2-38→2-39, 2-41
  MDLO 2-34→2-35
  MDP 2-37
  MOVE_OK 5-45
  MP 2-37
  MPC 2-38
  MPC1 2-20→2-21, 2-38
  MPC2 2-20, 2-38
  MR/ 2-31, 2-34→2-35, 2-39→2-40
  MRF 2-20
  NINH/ 2-34, 2-36, 2-41
  NP 2-37
  NPC 2-38
  OPNLFT\ 5-44→5-45
  OPNRT\ 5-45
  OUT\ 5-32→5-33
  PINRETRACT\ 5-39
  REV1\ 5-40
  REVFAST\ 5-38
  REVSLOW\ 5-38
  ROT_OK 5-38

ROTMOTFWD\ 5-38
ROTMOTPWR\ 5-39
ROTMOTREV\ 5-38
ROTMOTSLOW\ 5-38
START/ 2-39→2-40
TERAIRON\ 5-43
TERVACON\ 5-43
TES/ 2-33
TS 2-34→2-35
UHL 2-34
WBCREL/ 2-42
WCCL 2-36
WCWL 2-36
Low Voltage Sensor 2-21
LP logic signal 2-34→2-35
LVDT 5-13, 5-31
Interface, Secondary Mirror 5-13, 5-31
LVDTPWR\ Logic Signal 5-31

M

Main Drive 2-34
(MD) Inrush Limiter 2-19
Inhibit 2-34
Interlock Logic 2-34
Lockout Switch 2-10, 2-35→2–36
Power→Also see DC Drive Power Subsystem 2-23, 2-27, 2-37
Power Control 2-37
Power Relay Control 2-18
Power Relays 2-18→2-20, 2-34, 2-41
Relay Driver 2-20
Relay Failure Symptoms 2-21
Relay Monitor 2-18, 2-20→2-21
Servo Amplifiers 2-7, 2-11→2-12, 2-18→2-20, 2-28, 2-31, 2-33→2-35, 2-37
Servo Motors 2-22
Servos 2-1, 2-5, 2-9, 2-35, 2-38, 2-40, 2-42
Main Drive and NIR
Relay Monitors 2-20
Servo Amplifiers 2-19, 2-28
Servo Outputs 2-23
Servos Functional Block Diagram 2-6
Servos Simplified Block Diagram 2-2
MAX SPD Adjustment (Tertiary Mirror Rotator) 5-36
MBCREL/ logic signal 2-42
MC1CLOSED Logic Signal 5-46
MC1OPENED Logic Signal 5-45→5-46
MC2CLOSED Logic Signal 5-46
MC2OPENED Logic Signal 5-46
MCCL logic signal 2-36
MCLFTCLOSED Logic Signal 5-45
MCLFTCLS\ Logic Signal 5-45
MCLFTOPENED Logic Signal 5-33, 5-38, 5-45
MCLFTOPN\ Logic Signal 5-45
MCRHTOPENED Logic Signal 5-33, 5-38
MCWL logic signal 2-36
MD Inrush Limiter 2-19
MDINH/ logic signal 2-34, 2-36, 2-38→2-39, 2-41
MDLO logic signal 2-34→2-35
MDP logic signal 2-37
MIN SPD Adjustment (Tertiary Mirror Rotator) 5-36
Mirror
Cover Interface 5-6, 5-25, 5-44→5-45
Covers, Primary 5-6, 5-15, 5-17, 5-33, 5-38, 5-44
Fold Mechanism Interface, Tertiary 5-15, 5-32→5-33
LVDT Interface, Secondary 5-13, 5-31
Positioning System, Secondary 5-3
Positioning System, Tertiary 5-5
Primary 5-25
Rotator Interface, Tertiary 5-17, 5-35→5-39
Rotator Latch Pin, Tertiary 5-38
Rotator Mechanism, Tertiary 5-25
Rotator, Tertiary 5-37
Secondary 5-11
Stepper Motor Interface, Secondary 5-9, 5-29
Tertiary 5-5, 5-33, 5-45
Vacuum Support Load Cell Interface, Secondary 5-11, 5-30
Vacuum Support Load Cell Interface, Tertiary 5-15, 5-34
Mirror Cover Interface Block Diagram 5-24
Monitors
Current 2-7, 2-22→2-24
Drive Power 2-10→2-11, 2-37
MD (Main Drive) Relay 2-18, 2-20→2-21
NIR Relay 2-20
MOS Encoder 2-41
MOS NIR 2-23, 2-39, 2-42, 5-5, 5-15, 5-17, 5-25, 5-33, 5-45
MOS NIR Servo Amplifier 2-18
Motor Speed Control Module (Tertiary Mirror Rotator) 5-35
MOVE_OK Logic Signal 5-45
MP logic signal 2-37
MPC logic signal 2-38
MPC1 logic signal 2-20→2-21, 2-38
MPC2 logic signal 2-20, 2-38
MR/ logic signal 2-31, 2-34→2-35, 2-39→2-40
MRF logic signal 2-20
Multi-Object Spectrograph
See MOS NIR

N

Nasmyth Instrument Rotator
See NIR
NINH/ logic signal 2-34, 2-36, 2-41
NIR
Brake Control 2-38
Brake Pressure Switches 2-10
Brakes 2-34
Center Switch 2-10
Drives 2-34
Inhibit 2-34, 2-36
Inrush Limiter 2-37
Interlock Logic 2-34, 2-36
Interlock Telemetry 2-36
Latch Pin Switch 2-10
Limit Switches 2-10
MOS 5-5, 5-15, 5-17, 5-25, 5-33, 5-45
Power Control 2-37→2–38
Power Relay Control 2-18
Power Relay Drivers 2-20
Power Relays 2-18→2-19, 2-41
Relay Monitor 2-20
Servo Amplifiers 2-7, 2-11→2-12, 2-18→2-19, 2-28, 2-33, 2-37
Servo Drives 2-22
Servo Outputs 2-23
Servos 2-1, 2-5, 2-9, 2-13, 2-36, 2-38, 2-42
WIYN 5-15, 5-17, 5-25, 5-33, 5-45
NP logic signal 2-37
NPC logic signal 2-38

O

Observation Control Computer 2-33
OCS 5-5
Card Cage 5-7, 5-46
Enclosure 5-7, 5-27→5–32, 5–35→5–37, 5–39→5–46
Interfaces 5-27
Logic Board 5-17, 5-27, 5-32→5-33, 5-38, 5-44→5-46
Power 5-28
STD Bus Boards 5-7
Subsystem 5-2→5-3, 5-5→5-6
OPENED Status Switch (Mirror Cover status) 5-46
OPNLFT\ Logic Signal 5-44→5-45
OPNRT\ Logic Signal 5-45
Optical Encoder 2-3
Optics support structure Control Subsystem
See OCS
OUT\ Logic Signal 5-32→5-33
Overspeed
Latch 2-28, 2-31
Latch Telemetry 2-31
Threshold Reference Generator 2-28→2-29
Threshold Reference Voltages 2-29→2-30

P

PINRETRACT\ Logic Signal 5-39
Position Sensor, Counterbalance 5-41
Power
Control 2-12
Control Logic 2-11, 2-32, 2-37→2–38
Relay Drivers 2-19→2-20
Relays 2-7, 2-14, 2-18
Relays and Control Logic 2-7, 2-14, 2-18→2-20
Power and Brake Control 2-37→2-38
Power-on Reset Generator 2-39
Preamplifiers
Secondary Mirror Vacuum Support Load Cell 5-30
Primary Mirror Covers 5-6, 5-15, 5-17, 5-25, 5-33, 5-38, 5-44→5-45
Pro-Log 7342-3 Stepper Motor Controller Board
See Stepper Motor Controller

R

Relay Enclosure (OCS) 5-29, 5-31→5–32, 5–39→5–40, 5–42→5–43
REV ACC Adjustment (Tertiary Mirror Rotator) 5-37
REV TQ Adjustment (Tertiary Mirror Rotator) 5-36
REV1\ Logic Signal 5-40
REVFAST\ Logic Signal 5-38
REVSLOW\ Logic Signal 5-38
Right Mirror Cover (Primary Mirror) 5-44
ROT_OK Logic Signal 5-38
Rotator Latch Pin (Tertiary Mirror) 5-39
ROTMOTFWD\ Logic Signal 5-38
ROTMOTPWR\ Logic Signal 5-39
ROTMOTREV\ Logic Signal 5-38
ROTMOTSLOW\ Logic Signal 5-38

S

Safety Warning 2-13
Secondary Mirror
LVDT Interface 5-13, 5-31
LVDT Interface Block Diagram 5-12→5-13
Mounting 5-5→5-6

Positioning System 5-3
Stepper Motor Interface 5-9
Stepper Motor Interface Block Diagram 5-8
Vacuum Support Load Cell Interface 5-10→5-11, 5-30
Sensor Switch Interface 2-9→2-11, 2-25, 2-29→2-30, 2-32, 2-34→2-36, 2-39
See also SES Sensor Switch Interface
Sensor, Index 2-3
Servo Amplifier 2-3→2-4
Azimuth 2-9, 2-18, 2-34
Elevation 2-9, 2-18, 2-34, 2-39
Enable Logic 2-10→2-11, 2-32, 2-39
Main Drive 2-7, 2-11→2-12, 2-18, 2-20, 2-28, 2-31, 2-33, 2-35
Main Drive and NIR 2-7, 2-11→2-12, 2-19, 2-28, 2-33, 2-37
MOS NIR 2-18
NIR 2-7, 2-11→2-12, 2-18→2-19, 2-28, 2-33, 2-37
Subassembly 2-22→2-24, 2-37
Subsystem 2-1, 2-5, 2-11, 2-14, 2-22
WIYN NIR 2-18
Servo Electronics Subsystem 2-4→2-5, 2-8, 2-14, 2-25, 2-41
Detailed Circuit Description 2-25
Functional Block Diagram 2-8
Functional Description 2-9→2-13
Logic Board 2-25
See also SES
See also SES Logic Board
Servos
Main Drive 2-2, 2-5→2-6, 2-9, 2-13, 2-35
Main Drive and NIR 2-1, 2-5, 2-40
NIR 2-1, 2-5, 2-9, 2-13
SES 2-19, 2-25, 2-28, 2-37
See also Servo Electronics Subsystem Logic Board 2-27
See Board, Fuse and Relay
Control Logic 2-9→2-11, 2-25, 2-27, 2-32
Fuse and Relay Assembly 2-25
See Fuse and Relay Board
Logic Board 2-25, 2-27, 2-32, 2-35, 2-37
See also Sensor Switch Interface 2-25
Sensor Switch Interface 2-25
SIBs (OCS) 5-23, 5-27, 5-29, 5-33, 5-43
Solenoid
Secondary Mirror Air Bag 5-22
Tertiary Mirror Air Bag 5-5, 5-22→5-23
Start Relay 2-33, 2-41→2-42
START/ logic signal 2-39→2-40
Status Switches
Counterbalance Limits 5-41
Primary Mirror Cover Position 5-25, 5-38, 5-45→5-46
Secondary Mirror Position 5-9
Tertiary Mirror Fold 5-15
Tertiary Mirror Fold Limit 5-33
Tertiary Mirror Fold Mechanism 5-15
Tertiary Mirror Latch Pin 5-17
Tertiary Mirror Rotator 5-45
Tertiary Mirror Rotator Latch Pin 5-39
STD Bus Boards (OCS) 5-7→5-8
Stepper Motor Controller 5-7, 5-29
Subsystem
DC Drive Power 2-1, 2-3→2-5, 2-7, 2-11, 2-14→2-21, 2-23, 2-28, 2-33, 2-37→2-39, 2-41
Dome Servo 2-5
Optics support structure Control (OCS) 5-1
Servo Amplifier 2-1, 2-5, 2-7→2-8, 2-11, 2-14, 2-22→2-24
Servo Electronics 2-4→2-5, 2-8→2-14, 2-25
Switch Interface Boards (OCS) 5-23, 5-27, 5-29, 5-33, 5-43
Switch(es)
Azimuth Limit 2-10
Brake Pressure 2-10
Dome Clamp Pressure 2-10
Dome Control MAINT and COMP 2-10
Dome Inverter Fault 2-10
Dome Maintenance Handpaddle 2-10
Dome Motor Low Velocity Limit 2-10
Drive Control Key- 2-12, 2-40→2-41
Elevation Latch Pin 2-10
Elevation Latch Pin Sensor 2-39
Elevation Limit 2-10
Elevation Tilt 2-10, 2-28→2-30
Emergency Stop 2-9, 2-12, 2-27→2-28, 2-33, 2-40
Interlock Override 2-9→2-10, 2-34→2-35, 2-39→2-40
Lift Platform 2-10→2-11, 2-35
Main Drive Lockout 2-10, 2-35→2-36
NIR Center 2-10
NIR Latch Pin 2-10
NIR Limit 2-10
On and Start 2-10
Servo Amplifier mode selection (S1) 2-23
Tape 2-10→2-11, 2-35→2-36
System
Engineering Data (EDS) 5-2

T

Tachometer
Azimuth Overspeed 2-28→2-29
Elevation Overspeed 2-28, 2-30
Interface 2-9, 2-11, 2-25, 2-28, 2-34
Tape switch 2-10→2-11, 2-34→2-36

TCC/DCC 2-3→2-5, 2-7, 2-10→2-11, 2-18, 2-20→2-21, 2-23→2-24, 2-27, 2-31→2-40, 5-2, 5-42
Telemetry
Azimuth and Elevation Limit Switches 2-34, 2-36
Azimuth Motor Current 2-7, 2-24
Azimuth Overspeed 2-31
Elevation Latch Pin 2-39
Elevation Motor Current 2-7, 2-24
Emergency Stop Command 2-33
Emergency Stop Switch 2-27, 2-33
Lift Platform Extended 2-35
Main Drive Interlock 2-36
Main Drive Power 2-37
Main Drive Power Relay 2-18, 2-20
NIR Interlock 2-36
NIR Limit Switches 2-34, 2-36
NIR Power 2-37
NIR Power Relay 2-18
Tape Switch 2-35
Telescope
Focusing 5-3
Temperature Monitoring 5-3
Telescope Control Computer/Device Control Computer 2-3
Telescope Control/Device Control Computer See TCC/DCC
TERAIRON\ Logic Signal 5-43
Tertiary Mirror 5-5→5-6
Cell 5-43
Fold Mechanism 5-33
Fold Mechanism Interface 5-15, 5-32→5-33
Position 5-15, 5-25, 5-33
Rotator Interface 5-17, 5-35→5-39
Rotator Latch Pin 5-38
Rotator Mechanism 5-25
Vacuum Support Load Cell Interface 5-15, 5-34
TERVACON\ Logic Signal 5-43
TES/ logic signal 2-33
Thermocoupler 5-3, 5-9, 5-28
Interface 5-9, 5-28
TS logic signal 2-34→2-35

U

UHL logic signal 2-34
Uninterruptable Power Supply
AC RTN (AC Return) 2-18
UP1 (120 VAC supply) 2-19→2-20
UPS Power 2-21, 2-33, 2-40, 2-42

V

Vacuum Solenoids
Secondary Mirror Mounting 5-43
Tertiary Mirror Mounting Cell 5-43
Vacuum/Air Bag Solenoid Interface 5-22→5-23, 5-43
VME Crate 2-5

W

Watchdog Timer 2-10→2-11, 2-32→2-33, 2-37, 2-40
WBCREL/ logic signal 2-42
WCCL logic signal 2-36
WCWL logic signal 2-36
WinSystem LPM-D/A-4-DC Digital-to-Analog Board - See D/A Board (OCS)
WinSystems LPM-7614 Parallel Interface Board - See Parallel Interface Board
WinSystems LPM-A/D12M Analog-to-Digital Board - See A/D 0 Board and A/D 1 Board
WinSystems LPM-COM4 Serial Communications Board - See COM-4 Board
WinSystems LPM-SBC40A Single Board Computer - See CPU Board (OCS)
WIYN
Encoder 2-41
NIR Brake Driver 2-42
NIR Servo Amplifier 2-18, 2-23
Servo Amplifier Enable Logic 2-39
WIYN NIR 5-5, 5-15, 5-17, 5-25, 5-33, 5-45

89091814319
b89091814319a